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Albanese et al.

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[54] **ADAPTIVE SIGNAL PROCESSOR FOR CLUTTER ELIMINATION**

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[73] Assignee: **Sperry Rand Corporation**, New York, N.Y.

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[21] Appl. No.: **70,194**

[52] **U.S. Cl.** ..... **343/5 R**; 343/7.7; 343/17.1 R; 343/100 CL

[51] **Int. Cl.**[2] **G01S 9/42**

[58] **Field of Search** ..... 343/5 R, 7.7, 17.1 R

[56] **References Cited**

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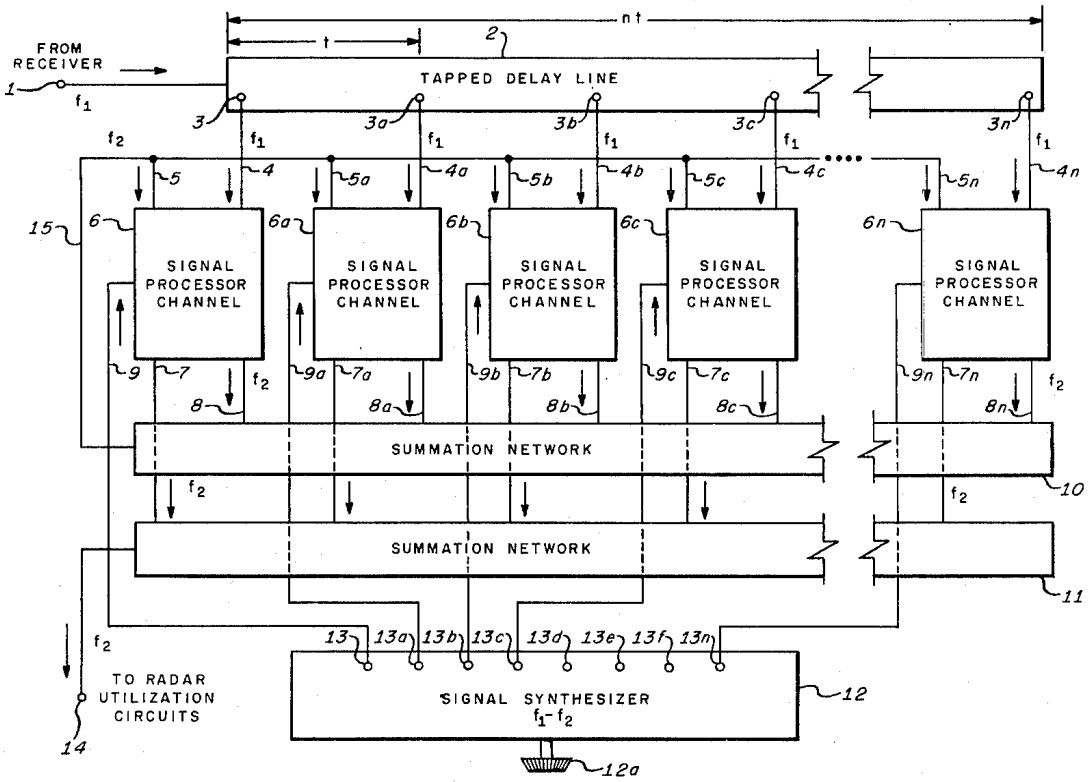
[57] **ABSTRACT**

An adaptive signal processing system for enhancing the signal-to-interference characteristics of a pulse radar system exposed to clutter signals as well as to desired target signals is disclosed. The time-extended clutter signals, along with specially generated phase reference signals are employed in a multi-element adaptive filter-correlator system to reduce the clutter presence in the radar receiver output to a minimum value for all target ranges and for both volume and surface clutter.

11 Claims, 9 Drawing Figures



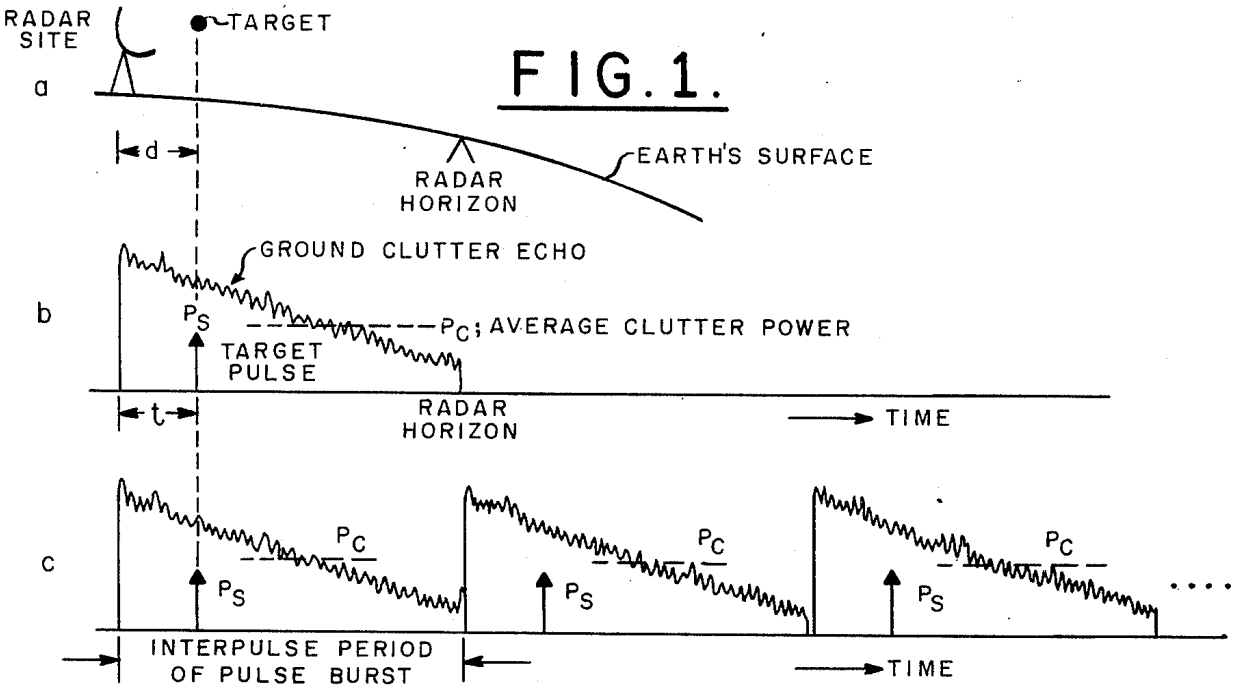


FIG. 1.

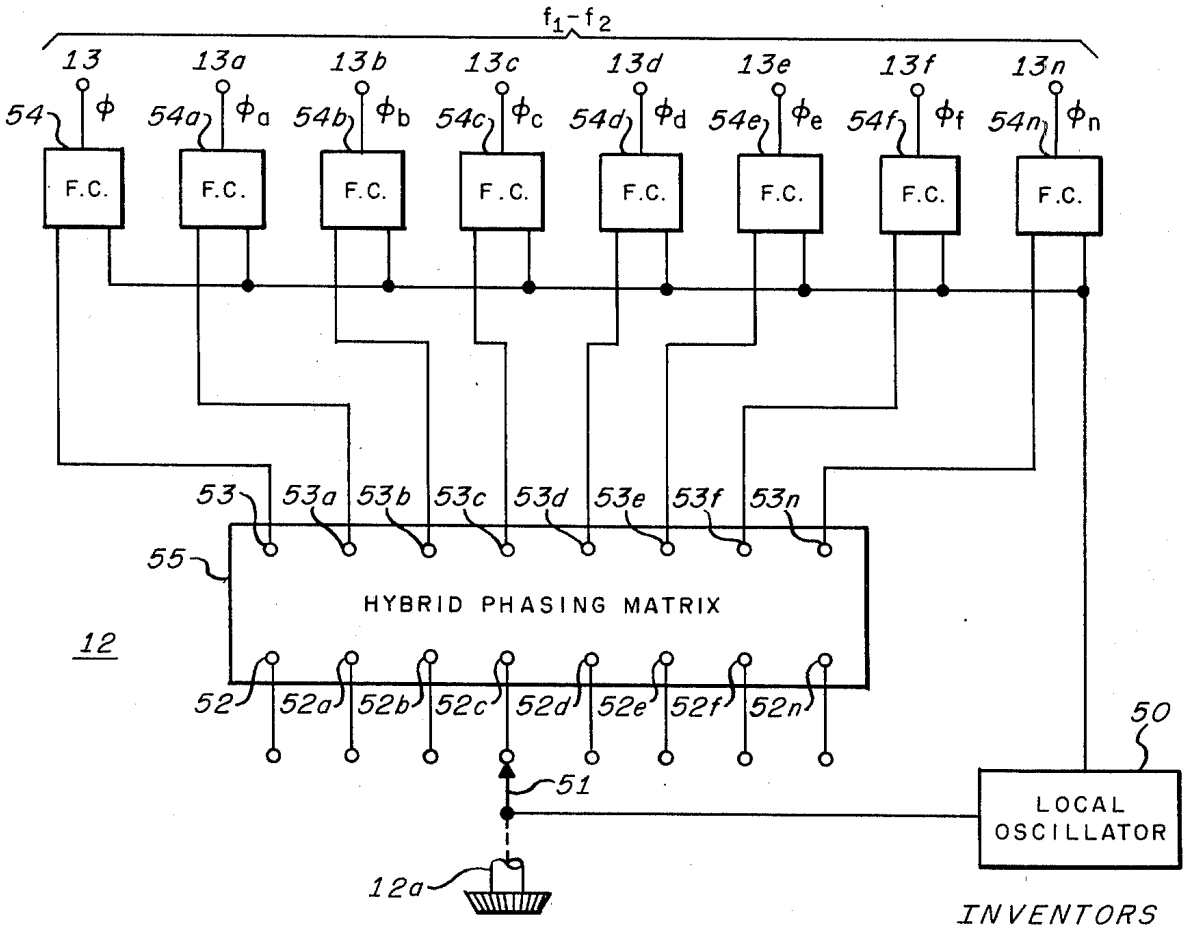


FIG. 9.

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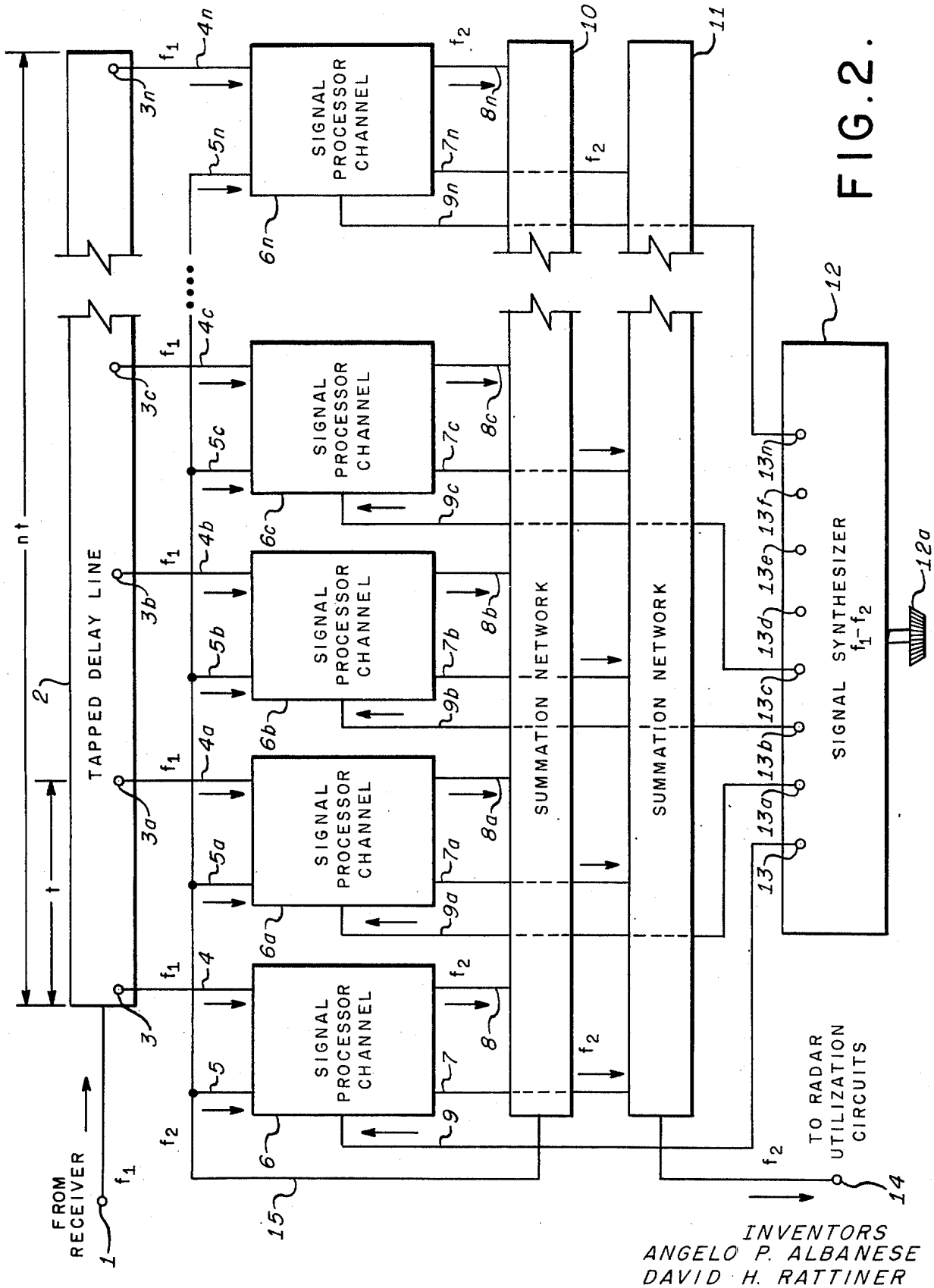

FIG. 2.

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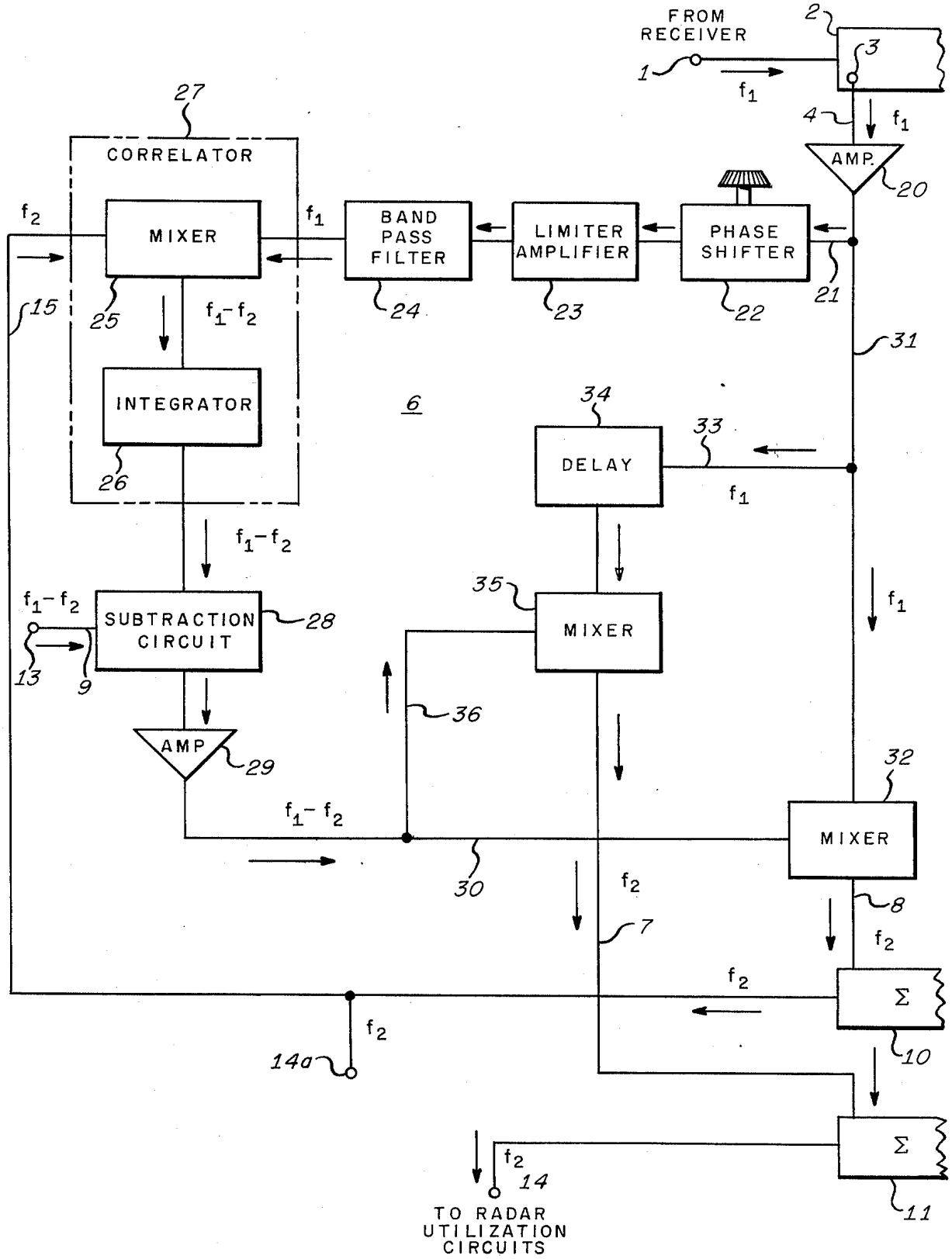

FIG. 3.

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FIG. 4.

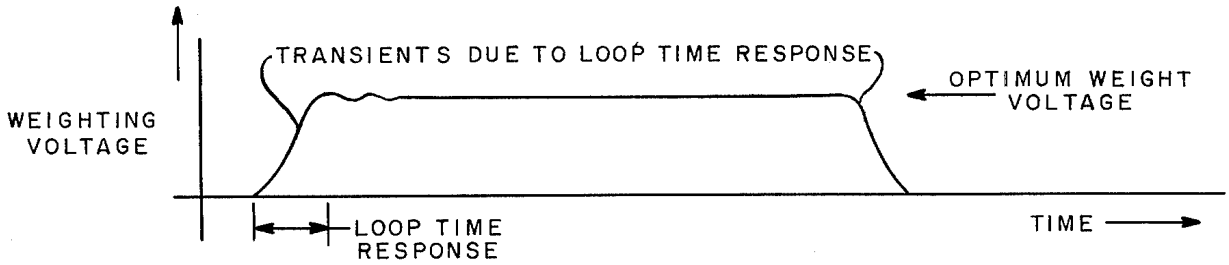

FIG. 5.

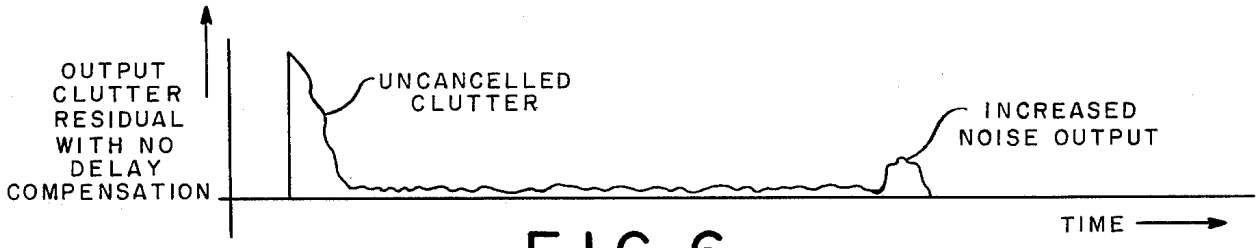

FIG. 6.

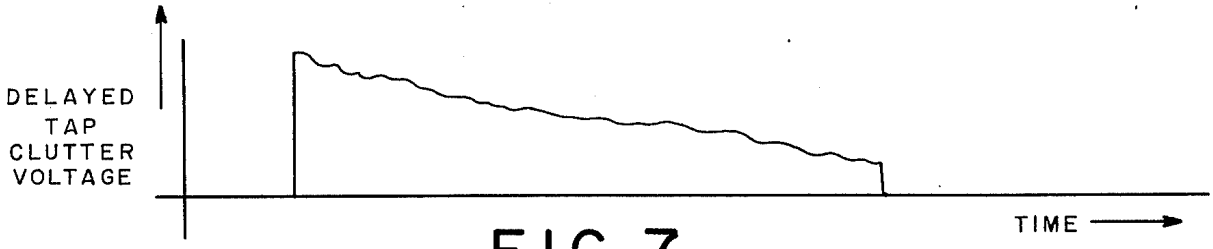

FIG. 7.

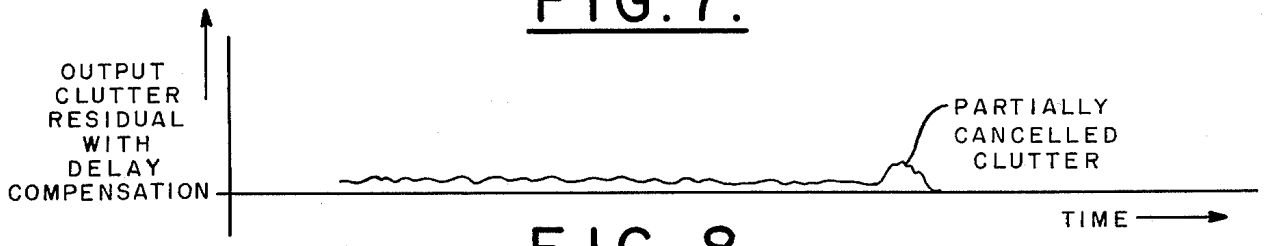

FIG. 8.

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ADAPTIVE SIGNAL PROCESSOR FOR CLUTTER ELIMINATION

CROSS REFERENCE TO RELATED APPLICATION

This document discloses apparatus used in carrying out the invention of co-pending patent application Ser. No. 70,277 for a "Radar Adaptive Signal Processor System", filed Sept. 8, 1970, and also assigned to the Sperry Rand Corporation.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention pertains to pulse radar receiver systems and more particularly to means for significant improvement of signal detection in pulse radar receivers exposed to clutter interference signals which may be of relatively high magnitude compared to desired target echoes, clutter signals such as rain, ground, and sea clutter return signals.

2. Description of the Prior Art

In prior art radar systems, various arrangements have been proposed for improving signal detectability, especially in the presence of interfering clutter signals such as ground return or rain return clutter. Moving target discriminating systems have, for instance, afforded a degree of signal-to-interference ratio improvement in efficiently diminishing the effects of clutter signals caused by stationary reflectors, such as the earth's surface. Non-adaptive radar signal processors provide acceptable clutter rejection for particular ranges and for particular types of clutter, but the performance of such systems degrades under varying clutter conditions. Further, when no interfering clutter is present, conventional non-adaptive processors are not generally optimum in the presence of ordinary electrical noise alone.

Matched filter signal processors have also been of interest for diminishing the effects of interfering clutter. However, such devices have not proven to achieve useful results under dynamically changing clutter conditions and in all range sectors. Defective results are noted particularly in matched filter operation upon the echo returns from multiple-pulse burst transmission radar systems. Matched filter processors fail to give required signal interference cancellation, for example, when the target of interest lies in particular periods of the several interpulse periods of the multi-pulse burst. Only in other particular interpulse periods may an acceptable signal-to-interference ratio be achieved. Thus, the total effect in such matched filter systems of the ultimate addition of the individual returns from a multiple-pulse burst is to yield an output having a degraded signal-to-interference ratio.

SUMMARY OF THE INVENTION

The invention is a dynamic signal processor system for effecting enhanced radar discrimination of target echoes in the presence of interfering clutter signals. The invention incorporates a time-varying filter system which adapts automatically to adjust its characteristics to optimum for each varying clutter return condition. Whether the transmitted radar impulses encounter rain or other weather clutter sources or ground clutter sources, or meet no such reflecting source, the adaptive filter system processes the received signals in an optimum manner for achieving maximum signal-to-interference performance of the radar system.

The adaptive time-variant filter system of the invention automatically alters its effective transfer function characteristic to minimize the output clutter of the radar receiver and to yield an output having a maximum signal-to-interference ratio. Appropriate variation of the filter characteristic is governed by the clutter signal input to the radar itself because of its conveniently time-extended nature. Certain control loops and correlator devices within the processor are primarily sensitive to these extended clutter signals, rather than responding to the short duration echo impulses returned from actual targets. Adaptive control is achieved by simultaneous plural measurements of the degree of correlation between the residual clutter voltage generated by the adaptive system and clutter voltage signals going into it. Any clutter remaining at the filter output generates a control voltage at the correlator outputs for modifying the filter transfer function characteristic so as to cause the residual clutter output signal to approach zero. The correlation control voltages and additional Doppler reference voltages having progressively incrementally varying phases permit processing of targets of selected target radial rates. Weighting voltages are adjusted by the presence of clutter and perform in the correlation process to maximize the final output signal-to-interference ratio. Means for overcoming unwanted clutter voltage residues because of the finite response times of the correlator processing systems within the adaptive filter are provided, as well as means for assuring the presence of correlation control and weighting voltages of adequate level.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1*a*, 1*b*, and 1*c* are graphs useful in explaining the operation of a radar system utilizing the invention.

FIG. 2 is a block diagram showing how elements of the invention cooperate.

FIG. 3 is a block diagram in greater detail of a typical portion of the apparatus of FIG. 2.

FIGS. 4 to 8 are graphs useful in explaining the operation of the invention.

FIG. 9 is a schematic block diagram showing details of part of the circuit of FIG. 2.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The invention is an adaptive signal processor apparatus for application in a radar system and which automatically adapts itself so as beneficially to process received radar signals having components representing target echoes and often other relatively large components due to the presence of clutter which adversely affect the operation of conventional radar systems. Such clutter may, for example, be generated by ground return or by rainfall in which the target is immersed. The novel adaptive processor mechanism provides rejection of the adverse effects of such types of clutter and permits the echo components truly representing a desired target to be extracted therefrom and to be used successfully for dependable radar display, control, or other purposes.

A significant feature of the novel adaptive signal processor system lies in its ability to operate as an adaptive time-varying filter that adapts automatically to present the optimum processing characteristics for time varying and other clutter conditions. For example, when the radar echoes contain patterns of interference

due to ground clutter and even to rapidly varying rainfall clutter conditions, the novel processor continues to operate upon the received signal components in an optimum way finally to yield processed target echo signals having a maximum signal-to-interference ratio.

Referring to level (a) in FIG. 1, the generalgeometry of the radar problem is illustrated so as to indicate the site of the radar system, the location of a target, and the horizon where ground clutter returns may substantially end because of the curvature of the earth's surface. At level (b) in FIG. 1, the radar return signal for the instance of the most conventional type of pulse radar system is shown. A single return target echo pulse P_s is seen at time t relative to the time of transmission of a single pulse from the radar transmitter and corresponding to the range d of the target. A typical ground clutter echo is illustrated having an average clutter power P_c on the order of the amplitude of the desired target echo pulse signal P_s. To this ground clutter, interference signals may also be added of further significance due, for example, to the presence of rain. Thus, the echo signal, when the radar transmits one pulse per repetition cycle, is composed of a narrow pulse P_s corresponding in time to the target range and a time or range-extended clutter echo composed of a random distribution of pulses. A wide variety of clutter patterns is possible, including substantially no clutter.

In a preferred form of the present invention, a radar system employing transmitter pulse bursts each comprising a multiplicity of transmitted pulses is used. Such pulse burst radar systems have been demonstrated, when used with prior art types of signal processors, to yield signal-to-interference characteristics improved in some degree. The adaptive processor of the present invention will be presented in the environment of such a pulse burst radar system.

Referring to level (c) of FIG. 1, it is assumed, for example, that n transmitted pulses, generally equally spaced apart and of substantially equal amplitude, are transmitted in each pulse burst packet, one such packet being emitted for each radar repetition cycle. A representative value of n is 8, though n may have other values, including odd values. The graph of level (c) of FIG. 1 shows only the first three parts of the consequent echo, the other $n-3$ parts being generally similar to the first three on a macroscopic basis. It is observed that the target echo P_s appears n times, still in the same time relation to each transmitted pulse comprising the pulse packet, and that the clutter interference train is similarly repeated. More complex models of the echo pattern include the case in which a relatively shorter interpulse period may produce clutter patterns actually overlapping two or more interpulse periods.

The general structure and operation of the novel radar adaptive signal processor will be understood with reference to FIG. 2. The chain of target echoes with accompanying clutter trains as seen in level (c) of FIG. 1 is prepared in conventional high frequency and intermediate frequency radar receiver circuits for application as a signal of nominal center frequency f_1 to terminal 1 of a delay line 2 having n output taps 3, 3a, 3b, . . . , 3n generally placed at equal intervals along the delay line or otherwise arranged to delay input signals by substantially equal amounts. A delay line identical to that used in the radar system transmitter for producing the transmitted burst of n pulses may be employed. Alternatively, techniques employed in digital processing systems and in radar moving target indicator apparatus may also be employed. In such an arrangement, the delay line 2 is also used on a sharing basis to determine the interpulse period of the transmitted pulses. While the specific means involved in the above function is not necessarily a part of the present invention, a single low loss, fuzed quartz ultrasonic delay line or a plurality of such delay lines may be employed to perform the function of delay line 2. In general, the signal input to delay line 2 may have a carrier frequency in the megacycle per second range and may require a 10 percent band width. Line 2 may be placed in a thermally stable oven.

The delay line taps 3, 3a, 3b, . . . , 3n are respectively coupled to form a set of first inputs on leads 4, 4a, 4b, . . . 4n to substantially identical signal processor channels 6, 6a, 6b, . . . , 6n, whose essential features will be further described with reference to FIG. 3. Each of the first set of inputs is of frequency f_1 and may contain target echoes and interference components of considerable amplitude. Each of signal processor channels 6, 6a, 6b, . . . , 6n has two additional inputs, as will be seen.

A first set of outputs of the respective processor channels appearing respectively on leads 8, 8a, 8b, . . . , 8n of processors 6, 6a, 6b, . . . , 6n is coupled by those leads to inputs of voltage summation network 10. Summation circuit 10 is typically a conventional resistance network of the kind ordinarily used coherently to add the voltages of n input signals of common phase and frequency and to supply a true sum signal on a single output, such as on feed back lead 15. Circuits employing conventional bilateral power dividers may be used. As will be seen, the sum voltage signal on lead 15 represents the residual level of the clutter signals and is coupled to the second set of inputs 5, 5a, 5b, . . . , 5n of the respective signal processor channels 6, 6a, 6b, . . . , 6n.

A third set of inputs is applied to the respective signal processor channels 6, 6a, 6b, . . . , 6n via leads 9, 9a, 9b, . . . , 9n and originates on the respective terminals 13, 13a, 13b, . . . , 13n of signal synthesizer 12, which device remains to be discussed in further detail with reference to FIG. 9. This third set of input signals constitutes fixed amplitude or reference signals of frequency f_1-f_2 and of progressively different phases as one goes from terminal 13 to terminal 13n. These reference signals, as applied to the respective processor channels 6, 6a, 6b, 6c, . . . , 6n, have a characteristic phase progression corresponding to the phase progression which whould appear at successively equal times in a selected Doppler frequency corresponding to an anticipated radial velocity of a selected target. Signal synthesizer 12 may be adjusted manually by use of manually controlled knob 12a to produce any of a different series of such equally spaced phase progressions on terminals 13, 13a, 13b, . . . , 13n, the progressions having different phase-spacings corresponding to a succession of different possible target radial velocities. By such selection, the adaptive system is, in effect, tuned to process data for a target of particular radial velocity. It will be understood that automatic positioning of adjustment 12a is within the scope of the present invention; evidently, known radar means for measurement of the Doppler velocity displacement may be used to supply a control voltage to a suitable servo for operation of adjustment 12a. Furthermore, it will be understood that selection of the appropriate reference voltage phase sequence compensates for the actual Dop-

pler phase shift of a target of interest so that coherent addition can actually be practiced in summation network **10**.

From the foregoing, it will be appreciated that the output at each tap **3**, **3***a*, **3***b*, . . . , **3***n* of delay line **2** has an associated control loop respectively comprising a signal processing channel **6**, **6***a*, **6***b*, . . . , **6***n* which modifies its respective delay line tap output for summation with all other tap outputs by voltage summation network **10**. The summation output is supplied by feed back connection **15** to each of the individual control loops via respective signal processing channels **6**, **6***a*, *b*, . . . , **6***n*.

It is understood that target echo signals and clutter return from each pulse component of the pulse burst packet are present at the respective taps **3**, **3***a*, **3***b*, . . . , **3***n* of delay line **2**. Each individual control loop adapts its characteristics to find the correlation between the individual outputs of taps **3**, **3***a*, **3***b*, . . . , **3***n* and the voltage summation output of network **10**.

In each processor **6**, **6***a*, **6***b*, . . . , **6***n*, the correlation voltage derived from an internal correlator is subtracted from the anticipated Doppler reference voltage from signal synthesizer **12**. The amplitude-difference signal is amplified and is used to form a product by amplitude multiplication with the corresponding tap clutter voltage. The effect of the control loop associated with each of the *n* signal processor loops is to adjust the amplitude and phase of the clutter voltage at each respective tap **3**, **3***a*, **3***b*, . . . , **3***n* such that the summation output of network **10** is substantially zero.

Whereas the signal processor channels **6**, **6***a*, **6***b*, . . . , **6***n* and their associated loops cause the clutter voltages to be substantially cancelled in voltage summation network **10**, the desired target echo components are coherently summed because of the action of tapped delay line **2** and because correlator devices found in signal processor channels **6**, **6***a*, **6***b*, . . . ,**6***n* do not respond to the very short target echo pulses. However, the same correlator devices respond optimally to the extended time function derived from the undesired clutter echoes.

The desired target output signals may be derived from feed back line **15** for application to the radar system displays or controls. However, for reasons yet to be explained, transient effects cause that voltage summation signal not to have fully acceptable properties. By a second manipulation of signals already provided within signal processor channels **6**, **6***a*, **6***b*, . . . , **6***n*, a more useful output with enhanced signal-to-interference characteristics is yielded. Such signals appear on a second set of output terminals associated with the *n* processors and are supplied by the respective leads **7**, **7***a*, **7***b*, . . . , **7***n* to a second voltage summation network **11**. A coherent addition is performed by network **11**, since it has characteristics similar to those of summation network **10**, and the desired echo return output appears on terminal **14** at frequency f_2, substantially free of undesired transient effects.

As noted previously, signal synthesizer **12** produces a set of reference signals of frequency f_1-f_2 having progressively incrementally different phases, which set is available on terminals **13**, **13***a*, **13***b*, . . . , **13***n* for application to the respective signal processor channels **6**, **6***a*, **6***b*, . . . , **6***n*. These reference signals each have the same amplitudes and the same intermediate frequencies, but they have a characteristic phase progression corresponding to the phase progression which would appear at successive equal times in a selected Doppler frequency signal corresponding to an anticipated radial velocity of a target. By selection of particular sets of differently spaced phase progressions at the output of signal synthesizer **12**, the adaptive system is tuned efficiently to process data for a target of particular radial velocity.

Generation by a conventional receiver master local oscillator of a reference signal of relatively stable amplitude, frequency, and phase for excitation of frequency synthesizer **12** may be accomplished by well known radar receiver techniques. Further, such a signal may be operated upon according to any of several known methods to produce simultaneously on independent output leads a set of signals having incrementally varying or shifted phase characteristics.

One available method for producing the desired incrementally phase shifted signals employs the characteristics inherent in a known bilateral hybrid phasing matrix whereby a continuous wave signal applied to any one of a first set of ports produces continuous waves at each of a second set of ports, the waves having a constantly incremented relative phase progression which will correspond to a desired Doppler frequency. If the same continuous wave signal is applied to a second of the set of input ports, a new phase progression corresponding to a new Doppler frequency is created. Such a hybrid phasing network may thus aid the function of synthesizer **12** when supplied with a multitap switch controlled by adjustment **12***a* to connect a suitable local oscillator signal to any selected one of its set of input ports. The more common of these matrices, which have been discussed at length in the literature circa 1961, have been employed with success in array antennas for developing multiple, simultaneous, radiation patterns in space and have, for example, employed fixed phase shifters and hybrid circuit elements having the 90° phase shift properties of branch-line directional couplers. The same matrices are realizable using other types of couplers or hybrids, such as sum and difference or other types of couplers. While other means of synthesis of the desired phase progression may be employed, such as a simple progression of phase shifters, the hybrid phasing network is advantageous, being passive and essentially lossless.

One method for employing the known hybrid phasing matrix for the above purpose is illustrated in FIG. **9**, wherein the receiver local oscillator system **50** produces microwave signals of carrier frequency F_1 and F_2. Signal F_1 is applied by switch **51** to a particular one of its *n* taps **52**, **52***a*, **52***b*, . . . , **52***n* by adjustment of knob **12***a*. According to the tap selected, a particular input of inputs **53**, **53***a*, **53***b*, . . . , **53***n* of hybrid matrix **55** is selected and, as previously mentioned, a particular array of microwave carrier signals having incrementally progressive phase shifts appears on terminals **53**, **53***a*, **53***b*, . . . , **53***n* of matrix **55**. This progression of signals is converted by applying a microwave carrier F_2 along with the outputs of carrier F_1 of terminals **53**, **53***a*, **53***b*, . . . , **53***n* to respective frequency converters **54**, **54***a*, **54***b*, . . . , **54***n*. The desired phase progression of signals of frequency f_1-f_2 thus appears on terminals **13**, **13***a*, **13***b*, . . . , **13***n*, carrier frequencies F_1 and F_2 being appropriately chosen for the purpose.

While the FIG. **9** apparatus employs, for example, two high frequency signals F_1 and F_2, for generation in converters **54**, **54***a*, **54***b*, . . . , **54***n* of the desired array of signals f_1-f_2 having progressively incrementally

different phases, that array of signals $f_1 - f_2$ may be generated by direct operation on an input $f_1 - f_2$ signal. An arrangement for such operation has been demonstrated by the selection of elements for hybrid phasing matrix **55** capable of operation also at relatively lower frequencies, such as at the intermediate frequency represented by $f_1 - f_2$. With such an intermediate frequency matrix, the local oscillator **50** supplies only the signal $f_1 - f_2$ to the tap **51** of switch **12***a*, the other ouput of local oscillator **50** being eliminated along with the several frequency converters **54**, **54***a*, **54***b*, . . . , **54***n*.

FIG. **3** shows in a detailed manner the structure of signal processor channel **6** of FIG. **2**; since signal processor channels **6**, **6***a*, **6***b*, . . . , **6***n* are smiliar circuits, only channel **6** and its associated connections need be discussed in detail. In FIG. **3**, parts already discussed in connection with FIG. **2** are indicated by the same reference numerals, including tapped delay line input **1**, the delay line **2** itself, tap **3**, tap lead **4**, the residual clutter output lead **15**, signal processor channel **6**, leads **7** and **8**, reference oscillator lead **9**, voltage summation networks **10** and **11**, terminal **13** of signal synchronizer **12**, and the final processor system output terminal **14**.

As mentioned above, terminal **1** of FIG. **3** is attached, for instance, to the output of a pulse burst radar system receiver adapted to receive substantially regularly spaced echo signals from a target in space illuminated by a pulse burst radar transmitter, for example, of the type emitting *n* successive generally equally and closely grouped transmitter pulses for each repetition cycle. The echo pulses applied to terminal **1** have a carrier frequency f_1 in the megacycle per second range, for example in the range between 10 and 100 megacycles per second, and are applied to the input transducer of delay line **2**. As is well known in the radar art, various noise and interference signals are simultaneously received at terminal **1** along with the desired target echo signals.

In the case of signal processor channel **6**, the first tap **3** on delay line **2** has its output supplied by lead **4** to amplifier **20**. Amplifier **20** has a moderate gain level, such as to overcome losses in delay line **2** and to contribute sufficient signals for the proper operation of the signal processor loop including channels **6** and feed back connector **15**. Amplifier **20** has a pass band centered on frequency f_1 of width, for example, about ten percent of frequency f_1. The output of amplifier **20** passes through one portion **21** of branching conductor to a trimmer phase shifter **22**. As will be seen, trimmer **22** provides means for adjustment of the phase shift within the loop so as to suppress any undesired tendency of the loop to oscillate. More important, proper adjustment of the set of such phase shifters used in processors **6**, **6***a*, **6***b*, . . . , **6***n* aids adjustment for minimum output clutter residue.

The output, still of frequency f_1, derived from phase shifter **22** is applied to limiter-amplifier or hard limiter circuit **23**, a device playing a significant role in the invention in that it processes input signals in such a way that a succeeding element in the circuit, the mixer **25** of correlator **27**, can properly function. Before being acceptable for use in mixer **25**, however, the output of limiter **23** is subjected to the action of band pass filter **24**. Because of its known inherent nature, hard limiter amplifier **23** tends to spread the spectrum of signal f_1 beyond its original band, particularly by the generation of undesired harmonic components. Band pass filter **24** beneficially brings the spectrum applied to mixer **25** back generally to the band width it orginally occupied when put into limiter-amplifier **23**.

Mixer **25** receives signal f_1 as above noted and, on feed back lead **15**, receives a signal of frequency f_2 from the output of summation circuit **10**. Mixer **25** may be a commonly used double balanced mixer of the known diode bridge type adapted to multiply the input amplitudes of signals f_1 and f_2 and to pass a signal whose frequency is the difference $f_1 - f_2$ of those frequencies to integrator circuit **26**.

Integrator **26** is a second part of what may be termed a correlator circuit which includes mixer **25**. Integrator **26** may take the form of a relatively narrow pass band, high Q, single pole filter circuit for taking the integral as a function of time of the amplitude of its input signal. As will be seen integrator **26** smooths or time-averages and filters its incoming signal and furnishes an output whose amplitude represents primarily the extent in time of clutter interference signals found in the returns received by the radar antenna. In this operation, the effect of the presence of any target return may be ignored, since such returns will be seen to contribute substantially nothing to the output of integrator **26** and correlator **27**. Correlator **27** compares the similarity between the amplitudes of its input signals f_1 and f_2. When they are totally un-alike, i. e., when the amplitude of signal f_2 on feed back lead **15** approaches zero, the correlator output is substantially zero.

The output of correlator **27** is passed as an input of frequency $f_2 - f_2$ to amplitude subtractor **28** along with a reference signal of frequency $f_1 - f_2$ derived on lead **9** from terminal **13** of the signal synthesizer **12** shown in FIG. **2**. It will be recalled that the terminal **13** signal has a particular reference phase ϕ (terminals **13** to **13***n* have progressively different reference phases ϕ to ϕ_n). Subtraction circuit **28** is a subtraction device known in the art for yielding an output signal still of frequency $f_1 - f_2$, but of diminished amplitude. A conventional passive intermediate frequency hybrid junction circuit, for example, may be used as circuit **28**.

The output of subtractor **28** is applied to mixer **32** via amplifier **29**, which amplifier may be a conventional device having relatively high gain and moderate to wide bandwidth characteristics for the purpose of minimizing loop errors. Mixer **32** is, for example, a mixer similar to mixer **25** and may be of the conventional double balanced mixer kind. It is adapted to multiply the individual amplitudes of signals input to it on leads **30** and **31**, but is connected so as to pass the sum of the input frequencies $f_1 - f_2$ and f_1, which is frequency f_2. It is seen that lead **30** supplies a weighting signal of frequency $f_1 - f_2$ from the output of amplifier **29** and that the branching conductor **31** from amplifier **20** supplies a signal of frequency f_1 to mixer **32** including target and clutter signals. The output of mixer **32** is a signal at frequency f_2 and is applied to the first of *n* inputs of the voltage summation network **10**.

It is seen from the above that signal processor channel **6** (and the similar channels **6***a* to **6***n*) is in the nature of a self-correcting adaptive correlator channel which, along with channels **6***a* to **6***n*, contributes coherent signals to voltage summation network **10** within which a residual clutter output signal is generated for application to the individual correlators **27** to **27***n* of the respective channels **6** to **6***n*.

In operation, limiter amplifier **23** is designed to have a sufficiently wide band with sufficient gain to establish a minimum level of the input interference or clutter

signals at an arbitrary value. Clutter or interference signals below that predetermined minimum value are raised to it. Since all clutter signals above that predetermined minimum level are clipped by the limiting action of limiter device **23**, relatively wide band width is necessary to provide short time constants for preventing the limiter from adversely distorting the clipped signals. Spurious signals generated in the limiting process are substantially eliminated by the band pass filter **24**. Thus, the limiter-amplifier **23** maintains the proper operating level of the signal f input to mixer **25** and enables the system comfortably to handle input signals of wide dynamic range. Since limiting will occur on substantially minimum level clutter returns, mixer **25** will always be in operation in the presence of clutter signals, assuring continual clutter cancellation of all of the input clutter and guaranteeing linear loop operation for low output clutter residues. Without the use of the limiter, only a small range of amplitudes of clutter power can be effectively cancelled because the efficiency of mixer **25** decreases as a function of decreasing clutter level. Thus, the weighting voltage supplied by amplifier **29** would not maintain the proper voltage level for optimum clutter cancellation.

The transient response of the loop including processor channel **6** and feed back lead **15** depends upon the time constant of integrator **26**, the total loop gain, and the input clutter or interference power level. Preferably, the time constant of integrator **26** is selected to obtain a desired average of extended input clutter signals and minimum response to signal returns from actual targets.

Amplifier **29** is a relatively high gain device for the purpose of reducing loop errors. So as to maintain stable loop operation, amplifier **29** is selected to have a low noise figure and a band width greater than integrator **26**. Such a band width assures that the loop stability is governed mainly by integrator **26**.

A further feature of the invention will also be explained in detail by reference to FIG. **2** and particularly to FIG. **3**. As noted previously, each signal processing channel **6** to **6*n*** is provided with a special means for provision at output terminal **14** of signals useful in conventional ways in the indicator, control and other utilization circuits of a radar system. Summation circuit **11** of FIG. **2** and its input leads **7** to **7*n*** from signal processor channels **6** to **6*n*** are additionally involved in performing such a function.

Referring to FIG. **3**, branching lead **31** supplies the signal f from amplifier **20** also to delay circuit **34** and thence to one input of mixer **35**. The second input of mixer **35** is supplied via branching lead **36** with the weighting signal voltage of frequency f f which is the output of amplifier **29**. Mixer **35** is again similar to mixer **25**, being a conventional double balanced mixer of the known diode bridge type. It is adapted to multiply the amplitudes of input signals of frequencies f and f f and to pass a signal whose frequency is the sum f of those input frequencies via lead **7** to a first input of voltage summation circuit **11**. Summation circuit **11**, like summation circuit **10**, may be any convenient resistor or other network adapted to add coherent inputs on n input terminals and to pass the sum to an output terminal, such as output terminal **14** of FIGS. **2** and **3**.

It is seen that the loop comprising processor channel **6** and feed back circuit **15** of FIG. **3** has a finite time response, so that rather broad uncancelled clutter spikes may form at the near and far ends of the clutter train processed thereby. These are formed before the loop has reached its steady state condition, the first uncancelled clutter spike due to the near edge of the clutter train being of most significant size.

The addition of delay **34** and multiplier-mixer **35** serves to suppress the undesirable transient. The delay line **34** delays the front or near edge of the clutter return until the weighting voltage output from amplifier **29** has achieved a steady state value. The clutter residues which, in the absence of elements **34, 35,** and **11** would appear at the time of the start of each clutter train, are a function of the transient response time of the control loops comprising processors **6, 6*a*, 6*b*, . . . 6*n*** and feed back connection **15**. Elimination of this transient component of the clutter residue permits the processor circuits to be otherwise adjusted for optimum performance without the imposition of conflicting design requirements.

The nature of the improvement, as will be further understood by examination of the graphs of FIGS. **4** to **8**, permits the weighting voltage appearing at the outputs **8, 8*a*, 8*b*, . . . , 8*n*** of each mixer **32, 32*a*, 32*b*, . . . , 32*n*** to be the weighting voltage truly required for substantial cancellation of the input clutter signals. FIG. **4** represents, as a function of time, the decaying form of the clutter voltage signal appearing at the respective taps of delay line **2**. With such an input wave, the adaptive system will generally create weighting voltages substantially as shown in FIG. **5**. The weighting voltage appearing, for example, on lead **30** at the output of amplifier **29** will be generally flat within the era of the clutter wave, but will have marked initial and terminal transients because of the time inherently required for the processor channels, such as channel **6**, to adjust to steady state operation. While the relatively flat era of the wave of FIG. **5** represents substantially the optimum weighting voltage, evidently the transient periods are not so representative.

As a consequence of the form of the weighting voltage, the output clutter residual on feed back line **15** would have the form shown in FIG. **6**. The wave is seen to approach zero while optimum operation obtains, but is characterized by large undesired uncancelled clutter excursions during the aforementioned transient periods. Inspection of the graphs of FIGS. **4** to **6** will indicate that the initial transient is the more troublesome of the two transients; in fact, the terminal transient will often be quite small for most types of clutter signals.

Thus, without delay compensation, the leading edge of the residual clutter signal will contain an initial uncancelled signal of large proportion enduring for the loop response time. It will seen from FIGS. **7** and **8** that the delay compensation circuit associated with the signal processor channel delay circuits such as circuit **34**, mixers such as mixer **35**, and summation network **11**, provides weighting voltages to the inputs of summation network **11** which substantially represent the true weighting voltages required for full cancellation of the significant parts of the clutter signals input from the tapped delay line **2**.

For example, FIG. **7** shows the delayed tap clutter voltage which might be derived from tap **1** of delay line **2** after passing through delay circuit **34**. The wave of FIG. **7** is zero amplitude during the initial loop transient period. When it is subjected to the amplitude multiplication operation of mixer **35**, no output can result during the loop transient period. Accordingly no initial

transient is present in the wave of FIG. **8**, which represents the output clutter voltage residual on output terminal **14** after the required delay compensation. It is, of course, within the scope of the invention to gate out a portion of the end of the clutter voltage wave of FIG. **7**, a portion again corresponding to the loop time response. A corresponding multiplication process, such as in mixer-multiplier **35**, will reduce the terminal transient uncancelled clutter seen in FIG. **8** substantially to zero. It will be understood that true target echo signals, of amplitude n times that appearing in a conventional single pulse radar system, will normally be seen (if present in the signals collected by the pulse burst radar system) in the graphs indicated in FIGS. **6** and **8** and as signals of amplitude many times the amplitude of the illustrated clutter residue signals.

While the invention has been described in its preferred embodiment, it is to be understood that the words which have been used are words of description rather than of limitation and that changes within the purview of the appended claims may be made without departure from the true scope and spirit of the invention in its broader aspects.

We claim:

1. Apparatus for improving the signal-to-interference characteristic of a composite signal comprising a pulse signal in the presence of an extended interference signal, said apparatus comprising:

means for forming a substantially constant amplitude signal for the duration of said interference signal,

first mixer-multiplier means for multiplying said substantially constant amplitude signal by a residual factor signal to produce a first product signal,

means for time integrating said first product signal,

second mixer-multiplier means for multiplying said time-integrated product signal by said composite signal to produce a product residual factor signal containing said desired signal stripped of a first substantial portion of said extended interference signal,

means for feeding back said residual factor signal to said first mixer-multiplier means,

third mixer-multiplier means for multiplying a delayed version of said composite signal by said time-integrated first product signal to form a signal containing said desired signal stripped of a second substantial portion of said extended interference signal, and

means for supplying said desired signal to utilization apparatus.

2. Apparatus as described in claim **1** wherein said means for forming a substantially constant amplitude signal for the duration of said interference signal comprises serially connected:

limiter-amplifier means, and

band pass filter means,

said band pass filter means having substantially the same pass band as the input of said limiter-amplifier means.

3. Apparatus as described in claim **1** including means directly following said time-integrating means for subtracting a constant-amplitude phase reference signal from said time integrated product signal.

4. Apparatus as described in claim **3**, wherein:

said first mixer-multiplier means is supplied with input signals of respective carrier frequencies f_1 and f_2 for producing an output signal of carrier frequency $f_1 - f_2$, and

said second mixer-multiplier means is supplied with input signals of respective carrier frequency f_1 and $f_1 - f_2$ for producing an output signal of carrier frequency f_2.

5. Apparatus as described in claim **4**, wherein:

said third mixer-multiplier means is supplied with input signals of respective carrier frequencies f_1 and $f_1 - f_2$ for producing an output signal of carrier frequency f_2.

6. Apparatus for improving the signal-to-interference characteristic of a composite signal comprising a pulse signal in the presence of an extended interference signal, said apparatus comprising:

first mixer-multiplier means having first and second input means and output means,

first circuit means for supplying said composite signal to said first input means of said first mixer-multiplier means,

second circuit means for receiving said composite signal and for supplying an output to said second input means of said first mixer-multiplier means,

said second circuit means comprising in series relation:

limiter-amplifier means,

band pass filter means,

correlator means having first and second input means and output means,

said correlator means comprising:

second mixer-multiplier means having first and second input means and output means,

integrator means having input means and output means and a characteristic settling time,

said second mixer-multiplier output means being coupled to said integrator input means,

circuit means for applying an output of said correlator output means to said second input means of said first multiplier-mixer means,

circuit feed back means for applying an output of said first mixer-multiplier means to said second input means of said correlator means,

third mixer-multiplier means having first and second input means and output means,

delay circuit means having a delay substantially equal to said integrator characteristic settling time,

circuit means for supplying said composite signal to said delay circuit means,

means for supplying said delayed signal to said first input means of said third mixer-multiplier means,

means for supplying said output of said integrator circuit to said second input means of said third mixer-multiplier means,

said third mixer-multiplier means being adapted to provide at its output means said pulse signal substantially stripped of said extended interference signal.

7. Apparatus as described in claim **6**, wherein:

said third mixer-multiplier first and second input means are supplied with input signals of respective carrier frequencies f_1 and $f_1 - f_2$ and said third mixer-multiplier means supplies an output signal of carrier frequency f_2.

8. Apparatus for improving the signal-to-interference characteristic of composite signals comprising desired pulse signals spaced at predetermined intervals, each in the presence of an extended interference signal, said apparatus comprising:

converter means, having plural output means, for placing one each of said desired pulse output means, for placing one each of said desired pulse

signals simultaneously on said converter output means,

plural signal processor means each having first, second, and third input means and first and second output means,

means coupling said converter output means to said first input means of said processor means,

first coherent signal summation means having plural input means and output means,

means coupling said first output means of said signal processor means to said plural input means of said first signal summation means,

means coupling said output means of said first summation means to said second input means of said signal processor means,

second coherent signal summation means having plural input means and output means,

means coupling said second output means of said signal processor means to said plural input means of said second summation means, and

means for coupling said output means of said second summation means to utilization apparatus.

9. Apparatus as described in claim **8** including:

hybrid matrix means having plural input means and plural output means,

local oscillator means,

means for selectively coupling said local oscillator means to said hybrid matrix means input means,

means for deriving plural incrementally-phased-shifted reference signals from said hybrid matrix means output means, and

means for coupling said reference signals to said third input means of said processor means.

10. Apparatus as described in claim **8** wherein said converter means comprises delay line means having input means and substantially equally spaced apart output means.

11. Apparatus as described in claim **8** wherein said signal processor means comprises:

first mixer-multiplier means having first and second input means and output means,

first circuit means for supplying said composite signal to said first input means of said mixer-multiplier means,

second circuit means for receiving said composite signal and for supplying an output to said second input means of said first mixer-multiplier means,

said second circuit means comprising in series relation:

limiter means,

filter means,

correlation means, and

circuit means for applying an output of said correlator means to said second input means of said first mixer-multiplier means.

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