Государственное образовательное учреждение
высшего профессионального образования
**«Томский государственный университет
систем управления и радиоэлектроники»**

ТЕМАТИЧЕСКИЙ РЕФЕРАТИВНЫЙ СБОРНИК № 50-1

“Energy Saving and Consumption Reducing”
(«Энергосбережение»)

Журнальные публикации

Источник: *Digital Library IEEEXplore*
Язык: *английский*
Глубина поиска: *2001 – 2011 гг.*
Дата формирования: *март 2011 г.*
Составитель: *В.И. Карнышев*

Томск – 2011

ТЕМАТИЧЕСКИЙ РЕФЕРАТИВНЫЙ СБОРНИК № 50-1

"Energy Saving and Consumption Reducing"
(«Энергосбережение»)

Журнальные публикации

"A Message-Scheduling Scheme for Energy Conservation in Multimedia Wireless Systems"

Reducing power consumption of wireless networks has become a major goal in designing modern multimedia wireless systems. In an effort to reduce power consumption, this paper addresses the issue of scheduling real-time messages in multimedia wireless networks subject to both timing and power constraints. A power-consumption model is introduced to calculate power-consumption rates in accordance with message-transmission rates. Next, a new message-scheduling scheme called Power-aware Real-time Message (PARM) is developed to generate message-transmission schedules that minimize power consumption of multimedia wireless-network interfaces and the probability of missing deadlines for real-time messages. With a power-aware scheduling policy in place, the proposed PARM scheme is very energy-efficient. Experimental results based on a wide variety of synthetic workloads and eight real-world applications show that PARM significantly reduces energy dissipation while maintaining low missed rates. PARM reduces power consumption of data transmissions by up to 99.4% (with an average of 86.7%) for synthetic network traffic and saves energy by up to 60.0% (with an average of 34.1%) in the eight real-world applications. [J1]

"Energy-Saving Cooperative Spectrum Sensing Processor for Cognitive Radio System"

Cooperative spectrum sensing has recently become an important research topic for cognitive radio systems because it solves the hidden terminal problem in single-user spectrum sensing. However, idle cognitive users must consume massive spectrum sensing energy for one operating cognitive user. This characteristic reduces the attraction of the cooperative spectrum sensing technique in practical cognitive radio systems. Therefore, this paper develops a partial spectrum sensing algorithm with decision result prediction (DRP) and decision result modification (DRM) techniques to reduce the cooperative spectrum sensing energy. This study also designs and implements an energy-saving spectrum sensing processor for cognitive radio systems. The proposed cooperative spectrum sensing chip reduces energy consumption by about 64% for one fast Fourier transform (FFT) spectrum sensing calculation. For any given specified spectrum detection time, the proposed chip could also improve the detection performance compared to the traditional FFT spectrum sensing. [J2]

"IP Over WDM Networks Employing Renewable Energy Sources"

With network expansion, the energy consumption and CO2emissions associated with networks are increasing rapidly. In this paper we propose an approach for energy minimization in IP over WDM networks and furthermore propose the use of renewable energy to further reduce the CO2emissions at a given energy consumption level. We develop a Linear Programming (LP) model for energy minimization in the network when renewable energy is used and propose a novel heuristic for improving renewable energy utilization. Compared with routing in the electronic layer, routing in the optical layer coupled with renewable energy nodes significantly reduces the CO2emission of the IP over WDM network considered by 47% to 52%, and the new heuristic introduced hardly affects the QoS. In order to identify the impact of the number and the location of nodes that employ renewable energy on the non-renewable energy consumption of whole network, we also constructed another LP model. The results show that the nodes at the center of the network have more impact than other nodes if they use renewable energy sources. We have also investigated the additional energy savings that can be gained through Adaptive Link Rate (ALR) techniques where different load dependent energy consumption profiles are considered. Our optimized REO-hop routing algorithm with renewable energy and ALR results in a maximum energy saving of 85% (average of 65%) compared to a current network design where all nodes are statically dimensioned for the maximum traffic in terms of IP ports and optical layer and hence consume power accordingly. Furthermore, when all the nodes have access to typical levels of renewable power we show that the associated reduction in non-renewable energy consumption reduces the network's CO2emissions by 97% peak, 78% average. [J3]

"Power-Efficient Explicit-Pulsed Dual-Edge Triggered Sense-Amplifier Flip-Flops"

A novel explicit-pulsed dual-edge triggered sense-amplifier flip-flop (DET-SAFF) for low-power and high-performance applications is presented in this paper. By incorporating the dual-edge triggering mechanism in the new fast latch and employing conditional precharging, the DET-SAFF is able to achieve low-power consumption that has small delay. To further reduce the power consumption at low switching activities, a clock-gated sense-amplifier (CG-SAFF) is engaged. Extensive post-layout simulations proved that the proposed DET-SAFF exhibits both the low-power and high-speed properties, with delay and power reduction of up to 43.3% and 33.5% of those of the prior art, respectively. When the switching activity is less than 0.5, the proposed CG-SAFF demonstrates its superiority in terms of power reduction. During zero input switching activity, CG-SAFF can realize up to 86% in power saving. Lastly, a modification to the proposed circuit has led to an improved common-mode rejection ratio (CMRR) DET-SAFF. [J4]

"EAD and PEBD: Two Energy-Aware Duplication Scheduling Algorithms for Parallel Tasks on Homogeneous Clusters"

High-performance clusters have been widely deployed to solve challenging and rigorous scientific and engineering tasks. On one hand, high performance is certainly an important consideration in designing clusters to run parallel applications. On the other hand, the ever increasing energy cost requires us to effectively conserve energy in clusters. To achieve the goal of optimizing both performance and energy efficiency in clusters, in this paper, we propose two energy-efficient duplication-based scheduling algorithms-Energy-Aware Duplication (EAD) scheduling and Performance-Energy Balanced Duplication (PEBD) scheduling. Existing duplication-based scheduling algorithms replicate all possible tasks to shorten schedule length without reducing energy consumption caused by duplication. Our algorithms, in contrast, strive to balance schedule lengths and energy savings by judiciously replicating predecessors of a task if the duplication can aid in performance without degrading energy efficiency. To illustrate the effectiveness of EAD and PEBD, we compare them with a nonduplication algorithm, a traditional duplication-based algorithm, and the dynamic voltage scaling (DVS) algorithm. Extensive experimental results using both synthetic benchmarks and real-world applications demonstrate that our algorithms can effectively save energy with marginal performance degradation. [J5]

"A Robust Edge Encoding Technique for Energy-Efficient Multi-Cycle Interconnect"

In this paper, we propose a new circuit technique for on-chip communication, the edge encoding technique, to reduce the energy consumption in multi-cycle interconnects. Both average and worst-case energy are reduced by desynchronizing the edges of rising and falling transitions. In a 1.2 V 65-nm CMOS technology, the proposed approach achieves up to 34% energy reduction with no latency overhead over optimally designed conventional busses due to coupling capacitance reductions. The technique further reduces energy consumption by 39% with iso-throughput at the expense of one-cycle latency. Energy savings are shown to be both larger and more robust to process, voltage, and temperature variations than previous techniques. [J6]

"Quasi-Static Voltage Scaling for Energy Minimization With Time Constraints"

Supply voltage scaling and adaptive body biasing (ABB) are important techniques that help to reduce the energy dissipation of embedded systems. This is achieved by dynamically adjusting the voltage and performance settings according to the application needs. In order to take full advantage of slack that arises from variations in the execution time, it is important to recalculate the voltage (performance) settings during runtime, i.e., online. However, optimal voltage scaling algorithms are computationally expensive, and thus, if used online, significantly hamper the possible energy savings. To overcome the online complexity, we propose a quasi-static voltage scaling (QSVS) scheme, with a constant online time complexity O(1). This allows to increase the exploitable slack as well as to avoid the energy dissipated due to online recalculation of the voltage settings. [J7]

"Domesticating Energy-Monitoring Systems: Challenges and Design Concerns"

Domestic energy consumption contributes approximately 30 percent to the UK's total C02 output. Although simple energy-saving steps can reduce the national carbon emission level by 10 percent, energy demand in housing and domestic appliances is rapidly increasing. The Digital Home Energy Management System assesses user experiences and preferences to provide appropriate feedback to domestic energy consumers and effect positive behavior change. [J8]

"Power-Efficient and Cost-Effective 2-D Symmetry Filter Architectures"

This paper presents two-dimensional (2-D) VLSI digital filter structures possessing various symmetries in the filter magnitude response. For this purpose, four Type-1 and four Type-2 power-efficient and cost-effective 2-D magnitude symmetry filter architectures possessing diagonal, fourfold rotational, quadrantal, and octagonal symmetries with reduced number of multipliers and one power-efficient and cost-effective multimode 2-D

symmetry filter are given. By combining the identities of the four Type-1 symmetry filter structures, the proposed multimode 2-D symmetry filter is capable of providing four different operation modes: diagonal symmetry mode (DSM), fourfold rotational symmetry mode (FRSM), quadrantal symmetry mode (QSM), and octagonal symmetry mode (OSM). The proposed diagonal, fourfold rotational, quadrantal, and octagonal symmetry filter structures can attain power savings of 16.77%, 36.30%, 22.90%, and 37.73% with respect to that of the conventional 2-D filter design without symmetry. On the other hand, the proposed DSM, FRSM, QSM, and OSM modes can reduce power consumption by 11.01%, 31.42%, 17.53%, and 35.26% compared with that of the conventional 2-D filter design. The proposed multimode filter can result in a 63.25% area reduction compared with the sum of the areas of the four individual Type-1 symmetry filter structures. [J9]

"Using Lossless Data Compression in Data Storage Systems: Not for Saving Space"

Lossless data compression for data storage has become less popular as mass data storage systems are becoming increasingly cheap. This leaves many files stored on mass data storage media uncompressed although they are losslessly compressible. This paper proposes to exploit the lossless compressibility of those files to improve the underlying storage system performance metrics such as energy efficiency and access speed, other than saving storage space as in conventional practice. The key idea is to apply runtime lossless data compression to enable an opportunistic use of a stronger error correction code (ECC) with more coding redundancy in data storage systems, and trade such opportunistic extra error correction capability to improve other system performance metrics in the runtime. Since data storage is typically realized in the unit of equal-sized sectors (e.g., 512 B or 4 KB user data per sector), we only apply this strategy to each individual sector independently in order to be completely transparent to the firmware, operating systems, and users. Using low-density parity check (LDPC) code as ECC in storage systems, this paper quantitatively studies the effectiveness of this design strategy in both hard disk drives and NAND flash memories. For hard disk drives, we use this design strategy to reduce average hard disk drive read channel signal processing energy consumption, and results show that up to 38 percent read channel energy saving can be achieved. For NAND flash memories, we use this design strategy to improve average NAND flash memory write speed, and results show that up to 36 percent write speed improvement can be achieved for 2 bits/cell NAND flash memories. [J10]

"Energy Reduction in Consolidated Servers through Memory-Aware Virtual Machine Scheduling"

Increasing energy consumption in server consolidation environments leads to high maintenance costs for data centers. Main memory, no less than processor, is a major energy consumer in this environment. This paper proposes a technique for reducing memory energy consumption using virtual machine scheduling in multicore systems. We devise several heuristic scheduling algorithms by using a memory power simulator, which we designed and implemented. We also implement the biggest cover set first (BCSF) scheduling algorithm in the working server system. Through extensive simulation and implementation experiments, we observe the effectiveness of the memory-aware virtual machine scheduling in saving memory energy. In addition, we find out that power-aware memory management is essential to reduce the memory energy consumption. [J11]

"Processing Continuous Range Queries with Spatiotemporal Tolerance"

Continuous queries are often employed to monitor the locations of mobile objects (MOs), which are determined by sensing devices like GPS receivers. In this paper, we tackle two challenges in processing continuous range queries (CRQs): coping with data uncertainty inherently associated with location data, and reducing the energy consumption of battery-powered MOs. We propose the concept of spatiotemporal tolerance for CRQ to relax a query's accuracy requirements in terms of a maximal acceptable error. Unlike previous works, our definition considers tolerance in both the spatial and temporal dimensions, which offers applications more flexibility in specifying their individual accuracy requirements. As we will show, these tolerance bounds can provide well-defined query semantics in spite of different sources of data uncertainty. In addition, we present efficient algorithms that carefully control when an MO should sense or report a location, while satisfying these tolerances. Thereby, we particularly reduce the number of position sensing operations substantially, which constitute a considerable source of energy consumption. Extensive simulations confirm that the proposed algorithms result in large energy savings compared to nontolerant query processing. [J12]

"Energy-Efficient Multicasting of Scalable Video Streams Over WiMAX Networks"

The Multicast/Broadcast Service (MBS) feature of mobile WiMAX network is a promising technology for providing wireless multimedia, because it allows the delivery of multimedia content to large-scale user communities in a cost-efficient manner. In this paper, we consider WiMAX networks that transmit multiple video streams encoded in scalable manner to mobile receivers using the MBS feature. We focus on two research problems in such networks: 1) maximizing the video quality and 2) minimizing energy consumption for mobile receivers. We

formulate and solve the substream selection problem to maximize the video quality, which arises when multiple scalable video streams are broadcast to mobile receivers with limited resources. We show that this problem is NP-Complete, and design a polynomial time approximation algorithm to solve it. We prove that the solutions computed by our algorithm are always within a small constant factor from the optimal solutions. In addition, we extend our algorithm to reduce the energy consumption of mobile receivers. This is done by transmitting the selected substreams in bursts, which allows mobile receivers to turn off their wireless interfaces to save energy. We show how our algorithm constructs burst transmission schedules that reduce energy consumption without sacrificing the video quality. Using extensive simulation and mathematical analysis, we show that the proposed algorithm: 1) is efficient in terms of execution time, 2) achieves high radio resource utilization, 3) maximizes the received video quality, and 4) minimizes the energy consumption for mobile receivers. [J13]

"A 2.4-GHz Energy-Efficient Transmitter for Wireless Medical Applications"

A 2.4-GHz energy-efficient transmitter (TX) for wireless medical applications is presented in this paper. It consists of four blocks: a phase-locked loop (PLL) synthesizer with a direct frequency presetting technique, a class-B power amplifier, a digital processor, and nonvolatile memory (NVM). The frequency presetting technique can accurately preset the carrier frequency of the voltage-controlled oscillator and reduce the lock-in time of the PLL synthesizer, further increasing the data rate of communication with low power consumption. The digital processor automatically compensates preset frequency variation with process, voltage, and temperature. The NVM stores the presetting signals and calibration data so that the TX can avoid the repetitive calibration process and save the energy in practical applications. The design is implemented in 0.18- μm radio-frequency complementary metal-oxide semiconductor process and the active area is 1.3 mm 2. The TX achieves 0-dBm output power with a maximum data rate of 4 Mb/s/2 Mb/s and dissipates 2.7-mA/5.4-mA current from a 1.8-V power supply for on-off keying/frequency-shift keying modulation, respectively. The corresponding energy efficiency is 1.2 nJ/b·mW and 4.8 nJ/b· mW when normalized to the transmitting power. [J14]

"A Cooperative Clustering Protocol for Energy Saving of Mobile Devices with WLAN and Bluetooth Interfaces"

One of the most widely used wireless communication standards is a Wireless Local Area Network (WLAN) (IEEE 802.11). However, WLAN has a serious power consumption problem. In this paper, we propose a novel energy saving approach that exploits the multiradio feature of recent mobile devices equipped with WLAN and Bluetooth interfaces. Unlike previous approaches, our work is based on clustering. In our work, a cluster is a Bluetooth Personal Area Network (PAN), which consists of one cluster head and several regular nodes. The cluster head acts as a gateway between the PAN and the WLAN, enabling the regular nodes to access the WLAN infrastructure via low-power Bluetooth. We present a distributed clustering protocol, Cooperative Networking protocol (CONET), which dynamically reforms clusters according to each node's bandwidth requirement, energy use, and application type. CONET does not require modifications of existing wireless infrastructures because clustering is performed independently of WLAN access points. We implemented the CONET prototype with four wearable computing devices to evaluate the performance on real hardware. We also simulated CONET for large networks of more than 100 mobile nodes. Both results demonstrate that our approach is effective in reducing the power consumption of WLAN. [J15]

"Hybrid timing-address oriented load-store queue filtering for an x86 architecture"

In the last few years, many researchers have focused their efforts on the field of low-power processor design. Several jobs in this area have dealt with the logic that enforces correct memory-based dependences-the load-store queue-(LSQ) a pretty energy-consuming structure since many accesses are performed in an associative fashion. Among these proposals, some of them manage to reduce this resource's energy consumption by avoiding unnecessary lookups. In this context, the authors introduce a straightforward filtering mechanism, which results in a more energy-efficient design than past techniques, using less and simpler hardware. Besides, both the new scheme and some previous approaches are tested in the widespread x86 architecture. This microarchitectural model provides new opportunities for extra types of filtering, which lead to higher energy savings. On average, the authors proposal filters up to 75% of the associative accesses to the load queue, 56% to the store queue and 42% to the dependence predictor with a reduced amount of hardware-less than 100 bytes. According to their energy model, this means a dynamic energy saving of more than 39% over a conventional LSQ. [J16]

"Design and implementation of a home embedded surveillance system with ultra-low alert power"

In this paper we design and implement a home embedded surveillance system with ultra-low alert power. Traditional surveillance systems suffer from an unnecessary waste of power and the shortcomings of memory

conditions in the absence of invasion. In this design we use Pyroelectric Infrared sensors (PIR) and pressure sensors as the alert group in windows and doors where an intruder must pass through. These low-power alert sensors wake up the MCU (Micro Controller Unit) which has power management for the ultrasonic sensors and PIR sensors indoors. This state transition method saves a large number of sensors required for the alert power. We also use the Majority Voting Mechanism (MVM) to manage the sensor groups to enhance the probability of multiple sensors sensing. After the MCU sends the sensor signals to the embedded system, the program starts the Web camera. Our sensing experiment shows that we reduce the system's power consumption. [J17]

"Evaluation of ONU power saving modes for gigabit-capable passive optical networks"

Energy efficiency has become an increasingly important aspect of designing access networks, due to both increased concerns for global warming and increased network costs related to energy consumption. Comparing access, metro, and core, the access constitutes a substantial part of the per subscriber network energy consumption and is regarded as the bottleneck for increased network energy efficiency. One of the main opportunities for reducing network energy consumption lies in efficiency improvements of the customer premises equipment. Access networks in general are designed for low utilization while supporting high peak access rates. The combination of large contribution to overall network power consumption and low utilization implies large potential for CPE power saving modes where functionality is powered off during periods of idleness. [J18]

"More efficient home energy management system based on ZigBee communication and infrared remote controls"

This paper describes more efficient home energy management system to reduce power consumption in home area. We consider the room easily controllable with an IR remote control of a home device. The room has automatic standby power cut-off outlets, a light, and a ZigBee hub. The ZigBee hub has an IR code learning function and educates the IR remote control signal of a home device connected to the power outlet. Then the power outlets and the light in the room can be controlled with an IR remote control. A typical automatic standby power cut-off outlet has a waiting time before cutting off the electric power. It consumes standby power during that time. To eliminate the waiting time, we turn off the home device and the power outlet simultaneously with an IR remote control through the ZigBee hub. This method actively reduces the standby power. The proposed HEMS provides easy way to add, delete, and move home devices to other power outlets. When a home device is moved to the different outlet, the energy information of the home device is kept consistently and seamlessly regardless of location change. The proposed architecture gives more efficient energy-saving HEMS. [J19]

"Rethinking energy efficiency models of cellular networks with embodied energy"

The continuous increase in energy consumption by cellular networks requires rethinking their energy efficiency. Current research indicates that one third of operating energy could be saved by reducing the transmission power of base stations. However, this approach requires the introduction of a range of additional equipment containing more embodied energy ?? consumed by all processes associated with the production of equipment. This problem is addressed first in this article. Furthermore, a new cellular network energy efficiency model with embodied energy is proposed, and optimization between the number of cells and their coverage is investigated. Contrary to previous works, we have found that embodied energy accounts for a significant proportion of total energy consumption and cannot be neglected. The simulation results confirm an important trade-off between operating and embodied energies, which can provide some practical guidelines for designing energy-efficient cellular access networks. The new model considering embodied energy is not limited to just cellular networks, but to other telecommunications, such as wireless local area networks and wired networks. [J20]

"Mixed bio-signal lossless data compressor for portable brain-heart monitoring systems"

This paper presents a highly integrated VLSI implementation of a mixed bio-signal lossless data compressor capable of handling multichannel electroencephalogram (EEG), electrocardiogram (ECG) and diffuse optical tomography (DOT) bio-signal data for reduced storage and communication bandwidth requirements in portable, wireless brain-heart monitoring systems used in hospital or home care settings. The compressor integrated in a multiprocessor brain-heart monitoring IC comprises 15k gates and 12kbits of RAM, occupying a total area of 58k μm2in 65nm CMOS technology. Results demonstrate an average compression ratio (CR) of 2.05, and a simulated power consumption of 170μW at an operating condition of 24MHz clock and 1.0V core voltage. Nominal power savings of 43% and 47% at the transmitter can be achieved when employing Bluetooth and Zigbee transceivers, respectively. [J21]

"Optimal Selective Forwarding for Energy Saving in Wireless Sensor Networks"

Scenarios where nodes have limited energy and forward messages of different importances (priorities) are

frequent in the context of wireless sensor networks. Tailored to those scenarios, this paper relies on stochastic tools to develop selective message forwarding schemes. The schemes will depend on parameters such as the available battery at the node, the energy cost of retransmitting a message, or the importance of messages. The forwarding schemes are designed for three different cases: 1) when sensors maximize the importance of their own transmitted messages; 2) when sensors maximize the importance of messages that have been successfully retransmitted by at least one of its neighbors; and 3) when sensors maximize the importance of messages that successfully arrive to the sink. More sophisticated schemes will achieve better importance performance, but will also require information from other sensors. The results contribute to identify the variables that, when made available to other nodes, have a greater impact on the overall network performance. Suboptimal schemes that rely on local estimation algorithms and entail reduced computational cost are also designed. [J22]

"Energy Optimization for Many-Core Platforms: Communication and PVT Aware Voltage-Island Formation and Voltage Selection Algorithm"

In this paper, we propose a novel approach to voltage-island formation, for the energy optimization of many-core architectures, which mitigates the impact of process, voltage, and temperature (PVT) variations. The islands are created by balancing their shape constraints imposed by intra and inter-island communication with the desire to limit the spatial extent of each island to minimize PVT impact. In addition, to reduce the number of voltage levels in the design, we propose an efficient voltage selection approach that provides near optimal results, for a set of 33 examined cases, with more than a ten times speedup compared to the best-known previous methods. This run-time improvement is important, especially for large many-core platforms. Finally, we present an evaluation platform considering pre-fabrication and post-fabrication PVT scenarios where multiple applications with hundreds to thousands of tasks are mapped onto many-core platforms with hundreds to thousands of cores to evaluate the proposed techniques. Results show that the average energy savings for 33 test cases using the proposed methods are 37% compared to 16% obtained using previous methods. [J23]

"MAC Essentials for Wireless Sensor Networks"

The wireless medium being inherently broadcast in nature and hence prone to interferences requires highly optimized medium access control (MAC) protocols. This holds particularly true for wireless sensor networks (WSNs) consisting of a large amount of miniaturized battery-powered wireless networked sensors required to operate for years with no human intervention. There has hence been a growing interest on understanding and optimizing WSN MAC protocols in recent years, where the limited and constrained resources have driven research towards primarily reducing energy consumption of MAC functionalities. In this paper, we provide a comprehensive state-of-the-art study in which we thoroughly expose the prime focus of WSN MAC protocols, design guidelines that inspired these protocols, as well as drawbacks and shortcomings of the existing solutions and how existing and emerging technology will influence future solutions. In contrast to previous surveys that focused on classifying MAC protocols according to the technique being used, we provide a thematic taxonomy in which protocols are classified according to the problems dealt with. We also show that a key element in selecting a suitable solution for a particular situation is mainly driven by the statistical properties of the generated traffic. [J24]

"Hardware-Based Load Balancing for Massive Multicore Architectures Implementing Power Gating"

Many-core architectures provide a computation platform with high execution throughput, enabling them to efficiently execute workloads with a significant degree of thread-level parallelism. The burstlike nature of these workloads allows large power savings by power gating the idle cores. In addition, the load balancing of threads to cores also impacts the power and thermal behavior of the processor. Processor implementations of many-core architectures may choose to group several cores into clusters sharing the area overhead, so that the whole cluster is power gated as opposed to the individual cores. However, the potential for power savings is reduced due to the coarser level of power gating. In this paper, several hardware-based stateless load-balancing schemes are evaluated for these clustered homogeneous multicore architectures in terms of their power and thermal behavior. All these methods can be unified into a parameterized technique that dynamically adjusts to obtain the desired goal (lower power, higher performance, and lower hotspot temperature). [J25]

"Color Filter-Less LCDs in Achieving High Contrast and Low Power Consumption by Stencil Field-Sequential-Color Method"

The field-sequential-color liquid crystal display (FSC-LCD) without a color filter enables high light efficiency, wide color gamut, and low material cost. However, the visual defect of color breakup (CBU) is perceived when relative velocities exist between the screen image and the human eye. We proposed the Stencil-FSC method with a 240-Hz field rate to make CBU imperceptible. Given the Stencil-FSC method, the hardware parameters were

optimized to reduce hardware complexity while maintaining sufficient suppression of CBU. After implementing Stencil-FSC on a 32-in FSC-LCD, the image contrast ratio was shown to be ten times more than that of a conventional CCFL LCD, and the average power consumption was reduced to less than 35 W-a 67% savings in power consumption. [J26]

"Building a Green Wireless-Optical Broadband Access Network (WOBAN)"

Access networks consume a significant portion of overall Internet energy consumption. With the increase of bit-rate requirements in access networks, future-proof access technologies should be energy efficient. In this paper, we show how we can build a very high-throughput "green" hybrid wireless-optical broadband access network (WOBAN). We devise novel energy-saving techniques for WOBAN to improve its energy efficiency and network utilization. We present a mixed integer linear program (MILP) model, which acts as a benchmark for evaluating our techniques. We analyze the impact of energy-aware design and protocols on the performance of WOBAN over dynamic traffic profiles. Illustrative numerical examples show that, with suitable design parameters, we can efficiently reduce energy consumption in WOBAN without significantly impacting the network performance. [J27]

"VEBEK: Virtual Energy-Based Encryption and Keying for Wireless Sensor Networks"

Designing cost-efficient, secure network protocols for Wireless Sensor Networks (WSNs) is a challenging problem because sensors are resource-limited wireless devices. Since the communication cost is the most dominant factor in a sensor's energy consumption, we introduce an energy-efficient Virtual Energy-Based Encryption and Keying (VEBEK) scheme for WSNs that significantly reduces the number of transmissions needed for rekeying to avoid stale keys. In addition to the goal of saving energy, minimal transmission is imperative for some military applications of WSNs where an adversary could be monitoring the wireless spectrum. VEBEK is a secure communication framework where sensed data is encoded using a scheme based on a permutation code generated via the RC4 encryption mechanism. The key to the RC4 encryption mechanism dynamically changes as a function of the residual virtual energy of the sensor. Thus, a one-time dynamic key is employed for one packet only and different keys are used for the successive packets of the stream. The intermediate nodes along the path to the sink are able to verify the authenticity and integrity of the incoming packets using a predicted value of the key generated by the sender's virtual energy, thus requiring no need for specific rekeying messages. VEBEK is able to efficiently detect and filter false data injected into the network by malicious outsiders. The VEBEK framework consists of two operational modes (VEBEK-I and VEBEK-II), each of which is optimal for different scenarios. In VEBEK-I, each node monitors its one-hop neighbors where VEBEK-II statistically monitors downstream nodes. We have evaluated VEBEK's feasibility and performance analytically and through simulations. Our results show that VEBEK, without incurring transmission overhead (increasing packet size or sending control messages for rekeying), is able to eliminate malicious data from the network in an energy-efficient manner. We also show that our framework performs be--tter than other comparable schemes in the literature with an overall 60-100 percent improvement in energy savings without the assumption of a reliable medium access control layer. [J28]

"Reducing Power Consumption with QoS Constraints in IEEE 802.16e Wireless Networks"

Mobile Broadband Wireless Access (BWA) networks will offer in the forthcoming years multiple and differentiated services to users with high mobility requirements, connecting via portable or wearable devices which rely on the use of batteries by necessity. Since a relatively large fraction of energy is consumed by such devices for transmitting/receiving data over-the-air, mechanisms are needed to reduce power consumption, in order to increase the lifetime of devices, and hence, improve user's satisfaction. The IEEE 802.16, which supports mobile BWA since its "e" amendment in 2005, defined power saving functions at the Medium Access Control (MAC) layer, which are designed to be operated during open traffic sessions for the greatest energy consumption reduction. However, enabling power saving usually increases the transmission latency, which can negatively affect the Quality of Service (QoS) experienced by users. On the other hand, imposing stringent QoS requirements may limit the amount of energy that can be saved. In this paper, an extensive study of the mutual interaction between power saving mechanisms and QoS support is carried out in the context of the IEEE 802.16e. In particular, two types of delay-constrained applications with different requirements are considered, i.e., Web and Voice over IP (VoIP) for which the IEEE 802.16e standard specifies two different power saving classes. The performance is assessed via detailed packet-level simulation, with respect to several system parameters. To capture the relative contribution of all the factors on the energy- and QoS-related metrics, part of the evaluation is carried out by means of 2k?? ??! analysis. [J29]

"Energy efficient multi-function home gateway in always-on home environment"

To provide digital home services without their suspension or any user's waiting, HG(Home Gateway) is to be

always in operating state because these home services can be started at any time, by any device and from any network (external or internal home network). Furthermore, some home network devices including HG are required to be ready to operate at any time in digital home environment. We call this characterized digital home network devices as 'Always-On' home network devices. The characteristic of always-on in home network environment gives rise to consuming more electrical power to activate these home network devices. In this paper, we propose a novel power control scheme to reduce effectively the power consumed by a HG. The proposed HG is composed of several function blocks which are controlled with separated power. In the proposed HG, we can power down all function blocks except for NPA(Network Protocol Agent) to maintain network connectivity and to monitor any service interrupt from any interior and exterior environments. With the proposed scheme, we can reduce the power consumed excessively by HG characterized with 'Always-On'. [J30]

"Multivoltage Floorplan Design"

Energy efficiency has become a very important issue to be addressed in today's system-on-a-chip (SoC) designs. One way to lower power consumption is to reduce the supply voltage. Multisupply voltage (MSV) is thus introduced to provide flexibility in controlling the power and performance tradeoff. In region-based MSV, circuits are partitioned into Г‚Вїvoltage islandsГ‚Вї where each island occupies a contiguous physical space and operates at one voltage level. These tasks of island partitioning and voltage level assignment should be done simultaneously in the floorplanning process in order to take those important physical information into consideration. In this paper, we consider this core-based voltage island driven floorplanning problem including islands with power down mode, and propose a method to solve it. Given a candidate floorplan solution represented by a normalized Polish expression, we are able to obtain optimal voltage assignment and island partitioning (including islands with power down mode) simultaneously to minimize the total power consumption. Simulated annealing is used as the basic searching engine. By using this approach, we can achieve significant power saving (up to 50%) for all datasets, without any significant increase in area and wire length. We compared our approach with the most updated previous work on the same problem, and results show that our approach is much more efficient and is able to save more power in most cases. We have also studied two other approaches to solve the same problem, a simple dynamic programming approach and a lowest possible power consumption approach. Experimental results show that ours can perform the best among these three approaches. Our floorplanner can also be extended to minimize the number of level shifters, to address a minVdd version of the problem and to simplify the power routing step by placing islands close to their corresponding power pins. [J31]

"Energy efficiency via thread fusion and value reuse"

Energy consumption has become the dominant metric when it comes to designing high-performance simultaneous multi-threaded (SMT) microprocessors. The authors propose a fusion of threads to help reduce energy consumption for these future SMT microprocessors. Threads are fused by merging two dynamic instances of the same static instruction into a single instruction thereby reducing unnecessary redundant computation in the front-end of the processor. The result is that power consumption is reduced in the pipeline until the execution stage. The authors have performed full system simulation, and our simulation results show average energy reduction of 10% with little impact on performance (less than 1%). They also extend thread fusion by proposing mechanisms to reduce the number of register file accesses and functional unit activity by reusing computations when the input values of the two dynamic instances of a fused instruction are the same. Our experiments show 5% energy savings in the integer register file and 10% in the integer functional units using this technique. [J32]

"Burst Transmission for Energy-Efficient Ethernet"

The proposed Energy-Efficient Ethernet (EEE) standard reduces energy consumption by defining two operation modes for transmitters and receivers: active and low power. Burst transmission can provide additional energy savings when EEE is used. Collecting data frames into large-sized data bursts for back-to-back transmission maximizes the time an EEE device spends in low power, thus making its consumption nearly proportional to its traffic load. An initial evaluation shows that the additional savings in the scenarios considered range from 5 to 70 percent for conventional users and approximately 50 percent for large data centers. [J33]

"A clipping reduction algorithm using backlight luminance compensation for local dimming liquid crystal displays"

Local dimming techniques cause clipping artifacts in liquid crystal displays. To overcome the problems associated with the artifacts, the backlight luminance should be adjusted, but this process increases power consumption. In this paper we propose a novel backlight luminance compensation algorithm to reduce clipping artifacts by minimizing the increment of backlight luminance. [J34]

"Enhanced power saving through increasing unavailability interval in the IEEE 802.16e systems"

The power saving mechanisms of the current IEEE 802.16e system are designed to take no consideration of the harmonization between power saving classes (PSCs) I and II. Using the IEEE 802.16e standard as a basis, we propose a dynamic power saving mechanism that increases unavailability interval when a mobile station (MS) uses PSCs. The proposed mechanism adjusts the timing of the sleep window of PSC I to maximize the unavailability interval of the MSs. As a result, the proposed scheme achieves power saving of the MSs. Through numerical analysis and simulations, we show that the proposed mechanism can reduce the power consumption of the MSs considerably compared with conventional mechanisms. [J35]

"Energy-Efficient VoIP over Wireless LANs"

Emerging dual-mode phones incorporate a wireless LAN (WLAN) interface along with the traditional cellular interface. The additional benefits of the WLAN interface are, however, likely to be outweighed by its greater rate of energy consumption. This is especially of concern when real-time applications, that result in continuous traffic, are involved. WLAN radios typically conserve energy by staying in sleep mode. With real-time applications like voice over Internet Protocol (VoIP), this can be challenging since packets delayed above a threshold are lost. Moreover, the continuous nature of traffic makes it difficult for the radio to stay in the lower power sleep mode enough to reduce energy consumption significantly. In this work, we propose the GreenCall algorithm to derive sleep/wake-up schedules for the WLAN radio to save energy during VoIP calls while ensuring that application quality is preserved within acceptable levels of users. We evaluate GreenCall on commodity hardware and study its performance over diverse network paths and describe our experiences in the process. We further extensively investigate the effect of different application parameters on possible energy savings through trace-based simulations. We show that, in spite of the interactive, real-time nature of voice, energy consumption during calls can be reduced by close to 80 percent in most instances. [J36]

"Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits"

Power has become the primary design constraint for chip designers today. While Moore's law continues to provide additional transistors, power budgets have begun to prohibit those devices from actually being used. To reduce energy consumption, voltage scaling techniques have proved a popular technique with subthreshold design representing the endpoint of voltage scaling. Although it is extremely energy efficient, subthreshold design has been relegated to niche markets due to its major performance penalties. This paper defines and explores near-threshold computing (NTC), a design space where the supply voltage is approximately equal to the threshold voltage of the transistors. This region retains much of the energy savings of subthreshold operation with more favorable performance and variability characteristics. This makes it applicable to a broad range of power-constrained computing segments from sensors to high performance servers. This paper explores the barriers to the widespread adoption of NTC and describes current work aimed at overcoming these obstacles. [J37]

"Using Embedded Dynamic Random Access Memory to Reduce Energy Consumption of Magnetic Recording Read Channel"

Although the performance of a magnetic recording read channel can be improved by employing advanced iterative signal detection and coding techniques, the method nevertheless tends to incur significant silicon area and energy consumption overhead. Motivated by recent significant improvement of high-density embedded dynamic random access memory (eDRAM) towards high manufacturability at low cost, we explored the potential of integrating eDRAM in read channel integrated circuits (IC) to minimize the silicon area and energy consumption cost incurred by iterative signal detection and coding. As a result of the memory-intensive nature of iterative signal detection and coding algorithms, the silicon cost can be reduced in a straightforward manner by directly replacing conventional SRAM with eDRAM. However, reducing the energy consumption may not be trivial. In this paper, we present two techniques that trade eDRAM storage capacity to reduce the energy consumption of iterative signal detection and coding datapath. We have demonstrated dDRAM's energy saving potential by designing a representative iterative read channel at the 65 nm technology node. Simulation shows that we can eliminate over 99.99% of post-processing computation for dominant error events detection, and achieve up to a 67% reduction of decoding energy consumption. [J38]

"Register File Partitioning and Compiler Support for Reducing Embedded Processor Power Consumption"

Register file (RF) in modern embedded processors contributes a substantial budget in the energy consumption due to its large switching capacitance and long working time. For embedded processors, on average 25% of

registers count for 83% of RF accessing time. This motivates us to partition the RF into hot and cold regions, with the most frequently used registers placed in the hot region, and the rarely accessed ones in the cold region. We employ the techniques of bit-line splitting and drowsy register cell to reduce the overall accessing power of RF. We propose a novel approach to partition the RF in a way that can achieve the largest power saving. We formulate the RF partitioning process into a graph partitioning problem, and apply an effective algorithm to obtain the optimal result. We evaluate our algorithm on MiBench and SPEC2000 applications, and an average saving of 58.3% and 54.4% over the non-partitioned RF accessing power is achieved for the SimpleScalar PISA system, respectively. The area overhead is negligible, and the execution time overhead is acceptable. [J39]

"The Power-Saving Mechanism With Periodic Traffic Indications in the IEEE 802.16e/m"

In IEEE Standards 802.16e (air interface standard for MWiMAX) and 802.16m (evolution of MWiMAX for IMT-Advanced), power saving is one of the important issues for battery-powered mobile stations (MSs) due to mobility. According to the IEEE 802.16e standard, when an MS switches from awake mode to sleep mode, the MS is required to send a sleep request (MOB-SLP-REQ) message and to receive a sleep response (MOB-SLP-RSP) message. In this paper, we propose a new sleep mode scheme called the power-saving mechanism with periodic traffic indications, where the MOB-SLP-REQ/RSP messages are omitted, and a traffic indication (TRF-IND) message is periodicallysent at the beginning of every constant TRF-IND interval. The merits of the proposed scheme are simple implementation, reduction of energy consumption, and saving of the resource compared with the sleep mode in the IEEE 802.16e standard. The proposed scheme in this paper is well aligned with the design policy of sleep mode in discussion at IEEE 802.16m in the sense that it tries to minimize the state transition overhead between the awake and sleep modes, and hence, it can reduce the delay for state transition and enhance the power-saving efficiency. We investigate the performance of the proposed scheme in two ways: simulation and analytical methods. Using the performance evaluation, we find the optimal TRF-IND interval, which minimizes the average power consumption of the MS while satisfying the quality of service (QoS) on the mean delay. Numerical results show that the proposed scheme has 20%-50% reduction of the energy compared with the power-saving class (PSC) of type I, which is one of three operations for sleep mode in IEEE 802.16e. [J40]

"Schedule Adaptation of Low-Power-Listening Protocols for Wireless Sensor Networks"

Many recent advances in MAC protocols for wireless sensor networks have been proposed to reduce idle listening, an energy wasteful state of the radio. Low-Power-Listening (LPL) protocols transmit packets for U s (the "interlistening interval"), thereby, allowing nodes to sleep for long periods of time between channel probes. The interlistening interval as well as the particular type of LPL protocol should be well matched to the network conditions. In this paper, we propose network-aware adaptation of the specific succession of repeated packets over the U interval (the "MAC schedule"), which yields significant energy savings. Moreover, some LPL protocols interrupt communication between the sender and the receiver after the data packet has been successfully received. We propose a new and simple adaptation of the "transmit/receive schedule" to synchronize nodes on a slowly changing path so that energy consumption and delay are further reduced, at no cost of overhead in most cases. Our results show that using network-aware adaptation of the MAC schedule provides up to 30 percent increase in lifetime for different traffic scenarios. Additional adaptation of the transmit/receive schedule to automatically synchronize the nodes can reduce packet delivery delays by up to 50 percent, providing an additional decrease in energy consumption of 18 percent. [J41]

"A 4 GHz Non-Resonant Clock Driver With Inductor-Assisted Energy Return to Power Grid"

Power consumption of a multi-GHz local clock driver is reduced by returning energy stored in the clock-tree load capacitance back to the on-chip power-distribution grid. We call this type of return energy recycling. To achieve a nearly square clock waveform, the energy is transferred in a non-resonant way using an on-chip inductor in a configuration resembling a full-bridge DC-DC converter. A zero-voltage switching technique is implemented in the clock driver to reduce dynamic power loss associated with the high switching frequencies. A prototype implemented in 90 nm CMOS shows a power savings of 35% at 4 GHz. The area needed for the inductor in this new clock driver is about 6% of a local clock region. [J42]

"Exploring Asynchronous Design Techniques for Process-Tolerant and Energy-Efficient Subthreshold Operation"

Supply voltage scaling is one of the easiest ways to reduce energy dissipation. Therefore, researchers have considered subthreshold logic as a promising option to achieve ultra low energy dissipation. However, circuit propagation delay is extremely sensitive to PVT variations under subthreshold operation. Hence, large delay

margin is required for successful operation of conventional synchronous designs. Since leakage energy contributes to a substantial portion of total energy dissipation in subthreshold operation, the leakage energy dissipated for the required delay margin degrades energy efficiency significantly. In addition, even small intra-die variations result in large clock skew and hence, it is difficult to efficiently handle timing issues such as the setup and the hold time violations. In this work, we explore asynchronous design approach to address these challenges in subthreshold operation. We employ critical-path replica to generate completion signals of combinational logic blocks and use classical four-phase handshaking for communication between pipeline flip-flops. Since the proposed design approach uses only local clock buffers, it is easier to handle timing problems compared to synchronous designs. We compared iso-yield minimum energy dissipation of two design approaches (synchronous and asynchronous) in an inverter chain. Despite leakage overhead due to pad delay of critical-path delay line and ?return-to-zero? time of four-phase handshaking, the proposed asynchronous design shows 71% energy savings compared to its synchronous counterpart. To demonstrate subthreshold operation of the proposed design approach, we fabricated an 8-tap FIR filter in 90 nm CMOS. Measured oscilloscope plots of handshaking and output bus signals show that the design operates successfully below 300 mV. We also measured energy consumption of the FIR filter from 19 test chips-the average was 4.64 pJ and the standard deviation was 0.3526 pJ. [J43]

"A 116 fps/74 mW Heterogeneous 3D-Media Processor for 3-D Display Applications"

In this paper, a heterogeneous 3D-media processor is presented, which supports all 3-D display applications by combining a 3-D display IP with a 3-D graphics IP and a stereo video decoder. For mobile environments, adaptive power management scheme is proposed, which saves power consumption up to 186 mW by turning off idle functional blocks based on a target application, a target performance, and the run-time ratio between different IPs. As a result, the minimum power consumption of the processor is only 15 mW, while the overall power consumption is 201 mW. As well as the reduction of power consumption, this work shows impressive performance improvement. The proposed fast modulo operators and adopted division-free algorithm reduces the critical latencies of 3-D display image processing. The proposed fast datapath with parallel architecture increase synthesis rate up to 116 fps which is 17 times faster than a previous work. In addition, reordered operation sequence fixes memory bandwidth regardless of the number of images to be produced. In the 3-D graphics IP and the decoding IP, redundant datapath are merged using an IEEE 754 compliant floating-point vector unit to save both chip area and power consumption, which even reduces the critical latency by 30%. [J44]

"Design of Power-Efficient Configurable Booth Multiplier"

In this paper, a power-efficient 16times16 configurable Booth multiplier (CBM) that supports single 16-b, single 8-b, or twin parallel 8-b multiplication operations is proposed. To efficiently reduce power consumption, a novel dynamic-range detector is developed to dynamically detect the effective dynamic ranges of two input operands. The detection result is used to not only pick the operand with smaller dynamic range for Booth encoding to increase the probability of partial products becoming zero but also deactivate the redundant switching activities in ineffective ranges as much as possible. Moreover, the output product of the proposed multiplier can be truncated to further decrease power consumption by sacrificing a bit of output precision. To efficiently and correctly combine these techniques, some additional components, including a correcting-vector generator, an adjustor, a sign-bit generator, a modified error compensation circuit, etc., are also developed. Finally, three real-life applications are adopted to evaluate the power efficiency and error performance of the proposed multiplier. The results show that the proposed multiplier is more complex than non-CBMs, but significant power and energy savings can be achieved. Furthermore, the proposed multiplier maintains an acceptable output quality for these applications when truncation is performed. [J45]

"Dynamic Bit-Width Adaptation in DCT: An Approach to Trade Off Image Quality and Computation Energy"

This paper presents a dynamic bit-width adaptation scheme for applications using discrete cosine transform (DCT). The technique can efficiently trade off image quality and computation energy. Based on sensitivity differences of 64 DCT coefficients, separate operand bit-widths are used for different frequency components to reduce computation energy. To select the appropriate operand bit-widths that achieve significant reduction of power consumption with minimum image quality degradation, we also propose a bit-width selection algorithm. The proposed variable bit precision DCT algorithm can be efficiently implemented using carry save adder trees. The reconfigurable DCT architecture can achieve power savings ranging from 36% to 75% compared to normal operation at the expense of minor image quality degradation. [J46]

"Computation Error Analysis in Digital Signal Processing Systems With Overscaled Supply Voltage"

It has been recently demonstrated that digital signal processing systems may possibly leverage unconventional voltage overscaling (VOS) to reduce energy consumption while maintaining satisfactory signal processing performance. Due to the computation-intensive nature of most signal processing algorithms, the energy saving potential largely depends on the behavior of computer arithmetic units in response to overscaled supply voltage. This paper shows that different hardware implementations of the same computer arithmetic function may respond to VOS very differently and result in different energy saving potentials. Therefore, the selection of appropriate computer arithmetic architecture is an important issue in voltage-overscaled signal processing system design. This paper presents an analytical method to estimate the statistics of computer arithmetic computation errors due to supply voltage overscaling. Compared with computation-intensive circuit simulations, this analytical approach can be several orders of magnitude faster and can achieve a reasonable accuracy. This approach can be used to choose the appropriate computer arithmetic architecture in voltage-overscaled signal processing systems. Finally, we carry out case studies on a coordinate rotation digital computer processor and a finite-impulse-response filter to further demonstrate the importance of choosing proper computer arithmetic implementations. [J47]

"Energy-Aware Tag Anticollision Protocols for RFID Systems"

Energy consumption of portable RFID readers is becoming an important issue as applications of RFID systems pervade many aspects of our lives. Surprisingly, however, these systems are not energy-aware with the focus till date being on reducing the time to read all tags by the reader. In this work, we consider the problem of tag arbitration in RFID systems with the aim of designing energy-aware anticollision protocols. We explore the effectiveness of using multiple time slots per node of a binary search tree through three anticollision protocols. We further develop an analytical framework to predict the performance of our protocols and enable protocol parameter selection. We demonstrate that all three protocols provide significant energy savings both at the reader and tags (if they are active tags) compared to the existing Query Tree protocol, while sharing the deterministic property of the latter. Further, we show that our protocols provide similar benefits even with correlated tag IDs. [J48]

"Behavior Modification"

This article describes how retail electricity demand can be made price-responsive through either dynamic, time-based retail pricing or DR programs offered by utilities and/or regional ISOs. PRD can provide the crucial link between wholesale and retail electricity markets that is missing under traditional fixed retail rates. Parties generally agree on the need for greater PRD to improve the efficiency of wholesale power markets. There is no mechanical formula for determining how much consumers will alter their usage patterns for any given event. Price response varies considerably across customers and it tends to be greater for customers with relatively high usage levels. Consumers can choose to save money by reducing consumption during periods of high prices or "buy through" at prices that reflect wholesale market conditions. [J49]

"Concurrent simulation platform for energy-aware smart metering systems"

We propose a simulation framework that can model a house equipped with various home appliances and next-generation smart metering devices. This simulator can predict the power dissipation profiles of individual appliances as well as the cumulative energy consumption of the house in a realistic manner. We utilize SystemC, a concurrent system-modeling methodology originally developed and populated in the design automation community. According to our experiments with various consumer electronics devices, the simulated and measured power profiles match very closely, producing the average correlation of 0.973. The deviation of simulated energy consumption from the measurement was also negligible. Using the proposed simulation platform, any electricity consumer interested in energy saving as well as the designer of a new smart metering system will be able to simulate and test their system from energy perspectives. As a case study, we show how the size of the accumulative power peak of a house can be reduced significantly by using the information provided by the proposed simulator. [J50]

"Boomerang: Reducing Power Consumption of Response Packets in NoCs with Minimal Performance Impact"

Most power reduction mechanisms for NoC channel buffers rely on on-demand wakeup to transition from a low-power state to the active state. Two drawbacks of on-demand wakeup limit its effectiveness: 1) performance impact caused by wakeup delays, and 2) energy and area cost of sleep circuitry itself. What makes the problem harder to solve is that solutions to either problem tend to exacerbate the other. For example, faster wakeup from a power-gated state requires greater charge/discharge current for the sleep transistors while using nimbler sleep transistors implies long wakeup delays. As a result, power downs have to be conservatively prescribed, missing

many power-saving opportunities. We propose Boomerang, a novel power-saving method that overcomes the above drawbacks. Specifically, based on the observation that a response is always preceded by a request, we let the request trigger wakeup of the buffer that is to be used by its response in the (near) future, instead of using on-demand wakeups. Hiding the wakeup delay completely, Boomerang allows us to employ aggressive sleep policies and use low-cost power gating circuits on response buffers. [J51]

"IEEE 802.3az: the road to energy efficient ethernet"

Ethernet is the dominant wireline communications technology for LANs with over 1 billion interfaces installed in the U.S. and over 3 billion worldwide. In 2006 the IEEE 802.3 Working Group started an effort to improve the energy efficiency of Ethernet. This effort became IEEE P802.3az Energy Efficient Ethernet (EEE) resulting in IEEE Std 802.3az-2010, which was approved September 30, 2010. EEE uses a Low Power Idle mode to reduce the energy consumption of a link when no packets are being sent. In this article, we describe the development of the EEE standard and how energy savings resulting from the adoption of EEE may exceed $400 million per year in the U.S. alone (and over $1 billion worldwide). We also present results from a simulation-based performance evaluation showing how packet coalescing can be used to improve the energy efficiency of EEE. Our results show that packet coalescing can significantly improve energy efficiency while keeping absolute packet delays to tolerable bounds. We are aware that coalescing may cause packet loss in downstream buffers, especially when using TCP/IP. We explore the effects of coalescing on TCP/IP flows with an ns-2 simulation, note that coalescing is already used to reduce packet processing load on the system CPU, and suggest open questions for future work. This article will help clarify what can be expected when EEE is deployed. [J52]

"A reconfigurable IDCT architecture for universal video decoders"

Nowadays, the reconfigurable architecture has become more and more popular. It not only decreases the time of research and development but also saves fabrication cost. Moreover, the proposed reconfigurable inverse discrete cosine transform (IDCT) architecture can support various video standards such as VC-1, MPEG-1/2/4 and H.264 AVC. It can sustain four transform types, 8 Ч 8, 8 Ч 4, 4 Ч 8, and 4 Ч 4 transform. The advantages of the proposed architecture are that this architecture does not require multipliers and ROM. It only needs adders and shifters. In digital circuits, the area of the multipliers and ROM are larger than adders and shifters. In order to reduce power consumption, we implement this reconfigurable architecture by using 90nm process technology to accomplish our chip design. The simulation result shows that the power consumption is only 3.4mW at 100MHz. The processor can perform HDTV 720p and HDTV 1080p in real-time. Briefly, the proposed architecture is regular, low power and reconfigurable. Therefore, it can be applied in universal video decoders. [J53]

"DRX-Aware Scheduling Method for Delay-Sensitive Traffic"

The Long Term Evolution (LTE) system adopts Discontinuous Reception (DRX) in the link level for power saving to extend the battery life of the User Equipment (UE). A novel real-time DRX-aware scheduling method is proposed for delay-sensitive services in wireless downlink systems. In the scheme, DRX parameters are introduced into the scheduling determinants, so as to reduce packet loss caused by the sleeping process during DRX. Simulation results show that, significant performance gain in terms of packet loss rate and power consumption, can be achieved by the proposed scheme compared with traditional schemes. [J54]

"Home energy management system based on power line communication"

This paper describes a home energy management system (HEMS) based on power line communication. Smart metering and power line communication can provide detailed information of energy consumption patterns and intelligent controlling to appliances at home. We propose a HEMS that can provide easy-to-access information on home energy consumption in real time, intelligent planning for controlling appliances, and optimization of power consumption at home. The HEMS consists of three modules: an advanced power control planning engine, a device control module, and a power resource management server. Our prototype system reduces the cost of power consumption by about 10%. [J55]

"Energy consumption minimization for mobile and wireless devices-a cognitive approach"

Energy consumption for mobile and wireless communication device, such as cell phones, has long been an important aspect for both designers and customers. This paper shows how a cognitive radio (CR) framework can help to reduce system energy consumption of a mobile and wireless communication device based on the application quality of service requirement, the channel condition, and the radio capabilities and characteristics. The CR framework enables not only adaptation of modulation, coding rate, coding gain, and radiated power as conventional adaptive modulation (AM) scheme, but also joint adjustment of radio component characteristics

(e.g., power amplifier (PA) characteristics) to achieve high energy efficiency. A unified PA efficiency model characterizing theoretical Class A, Class B, and practical PAs is adopted and enables the analysis of the impact of different radio configurations and channel conditions on energy efficiency. Significant energy savings (up to 90%) using the proposed CR framework for systems with theoretical PAs and with a realistic PA can be achieved compared with the conventional AM approach in simulation. This framework can also be used to manage other radio resources. [J56]

"A wireless sensor node SoC with a profiled power management unit for IR controllable digital consumer devices"

Network enabled digital technology increases the connectivity of consumer devices within the home for the purpose of remote control and monitoring of network enabled devices. Such dynamic control scheme for multiple legacy IR controllable digital consumer electronics appliances increases power consumption and system complexity. In this paper, we present a wireless sensor node SoC with a profiled power management unit for reducing active power consumption of a battery operated interactive home remote controller. The profiled power management unit decides the behavior of the power management service and the classes of operating hardware blocks which is used to control power state and hardware reset management for a wireless sensor node SoC. A profile includes the consumer devices classes, activity property values, and methods for changing a pending power state and an immediate power state. Proposed wireless sensor node SoC consists of an 8- bit embedded microcontroller with 64 Kbytes in-system programmable flash memory, hardwired media access control (MAC), RF transceiver and digital baseband. We fabricate a wireless sensor node SoC using 0.18 um CMOS technology and organize a wireless sensor network for home automation. These results show that it reduces active power consumption about 18% and it can be successfully applied in wireless sensor networks for further interactive home automation system. [J57]

"Design and implementation of a disk energy saving scheme for media players which use hybrid disks"

A hybrid hard disk drive that uses non-volatile memory as a cache is gaining popularity because of its improved reliability and performance. We present the design and implementation of a data prefetching scheme that makes use of flash memory to reduce disk energy consumption in media players. Based on the estimated time taken to prefetch data into flash memory, we selectively determine when to spin up or down the disk in a timely manner with the aim of reducing disk energy consumption while providing real-time video playback. We implemented our scheme in MPlayer running on the Linux 2.6. Experimental results show that the disk energy consumption can be reduced between 35% and 63%, if we add a reasonable amount of flash memory to a small DRAM. [J58]

"A color compensation algorithm to avoid color distortion in active dimming liquid crystal displays"

In LCD applications, various low power techniques, such as low voltage driving LEDs, high efficiency DC-DC converter circuitries, active backlight control schemes and the likes, have been applied to a backlight, which occupies the huge portion of total power consumption. Especially, it is a well-known fact that active dimming methods have accomplished considerable power reduction by as much as 20% up to 50% compared to the constant backlight method. However, the former technique may involve several artifacts such as color distortion, clipping, and so on. In this paper, color distortion in an active dimming LCD system caused by the mismatch between gamma values of pixel compensation algorithm and RGB sub-pixels, is analyzed and lowered by the proposed color compensation algorithm. This color compensation algorithm achieves the dramatic reduction on the color distortion without any loss of power saving performances. The maximum color difference ΔEabmaxhas been measured for each test image with the previous pixel compensation approaches (method-1 and method-2), and the average value of ΔEabmaxhas been obtained over 24 KODAK images. The resultant average value of a color compensated active dimming algorithm has been reduced to 0.413 and 0.478, compared to 24.595 and 9.527 of the conventional active dimming algorithms for method-1 and method-2, respectively. [J59]

"A local dimming algorithm for low power LCD TVs using edge-type LED backlight"

A local dimming algorithm is proposed to reduce the power consumption of LCD TVs using edge-type LED backlight. The proposed local dimming algorithm is implemented by matrix driving of orthogonally located LEDs at the edge of the backlight. The dimming rate of LED string is determined according to target luminance of local blocks and modified to reduce image distortion. The backlight power saving ratios of four typical images are 23.2-53.2 % and 30.2- 54.3% by using proposed division and rate algorithms, respectively. PSNR is greater than 48 dB using proposed local dimming algorithms. [J60]

"Challenges and enabling technologies for energy aware mobile radio networks"

Mobile communications are increasingly contributing to global energy consumption. In this article, a holistic approach for energy efficient mobile radio networks is presented. The matter of having appropriate metrics and evaluation methods that allow assessing the energy efficiency of the entire system is discussed. The mutual supplementary saving concepts comprise component, link and network levels. At the component level the power amplifier complemented by a transceiver and a digital platform supporting advanced power management are key to efficient radio implementations. Discontinuous transmission by base stations, where hardware components are switched off, facilitate energy efficient operation at the link level. At the network level, the potential for reducing energy consumption is in the layout of networks and their management, that take into account slowly changing daily load patterns, as well as highly dynamic traffic fluctuations. Moreover, research has to analyze new disruptive architectural approaches, including multi-hop transmission, ad-hoc meshed networks, terminal-to-terminal communications, and cooperative multipoint architectures. [J61]

"Cell zooming for cost-efficient green cellular networks"

Cell size in cellular networks is in general fixed based on the estimated traffic load. However, the traffic load can have significant spatial and temporal fluctuations, which bring both challenges and opportunities to the planning and operating of cellular networks. This article introduces a concept of cell zooming, which adaptively adjusts the cell size according to traffic load, user requirements and channel conditions. The implementation issues of cell zooming are then presented. Finally a usage case of cell zooming for energy saving is investigated. Centralized and distributed cell zooming algorithms are developed, and simulation results show that the proposed algorithms can greatly reduce the energy consumption, which leads to green cellular networks. [J62]

"Money for Research, Not Energy Bills: Finding Energy and Cost Savings in High-Performance Computer Facility Designs"

High-performance computing facilities in the US consume enormous amounts of electricity,, cutting into research budgets and challenging efforts to reduce energy consumption and meet environmental goals. Facility designs that target efficiency greatly reduce energy demand. This case study describes strategies and technologies to achieve facility energy reductions through thoughtful design. [J63]

"Study and Demonstration of Sleep and Adaptive Link Rate Control Mechanisms for Energy Efficient 10G-EPON"

This paper describes sleep and adaptive link rate (ALR) control functions to reduce the power consumption of optical network units (ONUs) in 10 Gb/s Ethernet passive optical network (10G-EPON) systems. A hybrid mechanism that includes both sleep and ALR control functions is proposed with a view to further improving the power-saving performance. The sleep control function switches the ONU mode, i.e., active or sleep, depending on the presence or absence of traffic. The ALR control function switches the downlink rates between an optical line terminal (OLT) and an ONU, i.e., 1 Gb/s or 10 Gb/s, depending on the quantity of traffic. The proposed hybrid mechanism offers effective power management of ONUs on the basis of the traffic conditions. The proposed hybrid mechanism is validated by a numerical simulation and an experiment. [J64]

"Performance enhancement and analysis for IEEE 802.16e/m sleep mode operations with unsolicited grant service/real-time variable-rate connections"

The power saving class of type II (PSC II), one of the sleep mode operations in the IEEE 802.16e standard, is designed to reduce power consumption for unsolicited grant service (UGS) and real-time variable-rate (RT-VR) connections. However, the configuration of fixed-length listening windows in the PSC II incurs unnecessary energy consumption or packet loss for these types of connections. In order to enhance the performance of sleep mode operations, an approach with adaptive listening window (ALW) is proposed. The ALW scheme dynamically adjusts the length of each listening window based on the number of both arrival and retransmission packets as well as the delay constraint. Numerical analysis and simulation results show that the proposed ALW approach can effectively reduce the packet loss rate for UGS connections, whereas better energy conservation with reduced packet loss rate is achieved for RT-VR connections. [J65]

"Efficient sensor for robust low-power design in nano-CMOS technologies"

Conventional design methods add pessimistic safety margins to mitigate increased variability in scaled technologies that incur high power and performance losses. An efficient sensor design is presented that can significantly reduce design margins yet provide robust circuit operation. The proposed design uses the delay of the master latch of a conventional flip-flop to predetect timing failures and enable low-power error-free operation. HSPICE simulation of a 45 nm 16 ГґВ— 16 carry save multiplier indicates a 37% reduction in the total power

consumption for the proposed design compared to a conventional worst case design when subjected to high statistical variability. Similarly, gate level simulations show a 26% reduction in the total power consumption of a 32 nm 32-bit carry select adder when subjected to temperature variations. [J66]

"Duty Cycle Control for Low-Power-Listening MAC Protocols"

Energy efficiency is of the utmost importance in wireless sensor networks. The family of Low-Power-Listening MAC protocols was proposed to reduce one form of energy dissipation-idle listening, a radio state for which the energy consumption cannot be neglected. Low-Power-Listening MAC protocols are characterized by a duty cycle: a node probes the channel every t_i {rm s} of sleep. A low duty cycle favors receiving nodes because they may sleep for longer periods of time, but at the same time, contention may increase locally, thereby reducing the number of packets that can be sent. We propose two new approaches to control the duty cycle so that the target rate of transmitted packets is reached, while the consumed energy is minimized. The first approach, called asymmetric additive duty cycle control (AADCC), employs a linear increase/linear decrease in the t_i value based on the number of successfully received packets. This approach is easy to implement, but it cannot provide an ideal solution. The second approach, called dynamic duty cycle control (DDCC) utilizes control theory to strike a near-optimal balance between energy consumption and packet delivery successes. We generalize both approaches to multihop networks. Results show that both approaches can appropriately adjust t_i to the current network conditions, although the dynamic controller (DDCC) yields results closer to the ideal solution. Thus, the network can use an energy saving low duty cycle, while delivering up to four times more packets in a timely manner when the offered load increases. [J67]

"Energy-Optimal Dynamic Thermal Management: Computation and Cooling Power Co-Optimization"

Conventional dynamic thermal management (DTM) assumes that the thermal resistance of a heat-sink is a given constant determined at design time. However, the thermal resistance of a common forced-convection heat sink is inversely proportional to the flow rate of the air or coolant at the expense of the cooling power consumption. The die temperature of the silicon devices strongly affects its leakage power consumption and reliability, and it can be changed by adjusting the thermal resistance of the cooling devices. Different from conventional DTM which aims to avoid the thermal emergency, our proposed DTM regards the thermal resistance of a forced-convection heat sink as a control variable, and minimize the total power consumption both for computation and cooling. We control the cooling power consumption together with the microprocessor clock frequency and supply voltage, and track the energy-optimal die temperature. Consequently, we reduce a significant amount of the temperature-dependent leakage power consumption of the microprocessor while spending a bit higher cooling power than conventional DTM, and eventually consume less total power. Experimental results show the proposed DTM saves up to 8.2% of the total energy compared with a baseline DTM approach. Our proposed DTM also enhances the Failures in Time (FIT) up to 80% in terms of the electromigration lifetime reliability. [J68]

"Leveraging Unused Cache Block Words to Reduce Power in CMP Interconnect"

Power is of paramount importance in modern computer system design. In particular, the cache interconnect in future CMP designs is projected to consume up to half of the system power for cache fills and spills. Despite the power consumed by spills and fills, a significant percentage of each cache line is unused prior to eviction from the cache. If unused cache block words can be identified, this information can be used to improve CMP interconnect power and energy consumption. We propose a new method of CMP interconnect packet composition, leveraging unused data to reduce power. These methods are well suited to interconnection networks with high-bandwidth wires, and do not require expensive multi-ported memory systems. Assuming perfect prediction, our technique achieves an average of 37% savings in total dynamic link power consumption. With our current best prediction mechanism, our techniques reduce dynamic power consumption by 23% on average. [J69]

"Chasing the Negawatt: Visualization for Sustainable Living"

Energy and resource management is an important and growing research area at the intersection of conservation, sustainable design, alternative energy production, and social behavior. Energy consumption can be significantly reduced by simply changing how occupants inhabit and use buildings, with little or no additional costs. Reflecting this fact, an emerging measure of grid energy capacity is the negawatt: a unit of power saved by increasing efficiency or reducing consumption.Visualization clearly has an important role in enabling residents to understand and manage their energy use. This role is tied to providing real-time feedback of energy use, which encourages people to conserve energy.The challenge is to understand not only what kinds of visualizations are most effective but also where and how they fit into a larger information system to help residents make informed

decisions. In this article, we also examine the effective display of home energy-use data using a net-zero solar-powered home (North House) and the Adaptive Living Interface System (ALIS), North House's information backbone. [J70]

"Multisize Sliding Window in Workload Estimation for Dynamic Power Management"

Energy efficiency has become one of the key challenges for a large class of electronic systems. Longer time between battery recharges is highly desirable for battery-powered devices such as mobile phones, digital cameras, Internet tablets, and electronic organizers. Energy efficiency is also important for electronic systems powered from the electric grid since it may reduce power consumption and the cooling requirements. Power savings are possible because electronic systems generally have an idle state, when, for example, the processor can run in a low-power state. Thus, the correct estimation of the workload model plays an essential role in the decision of which and when a power state transition should be performed by the electronic system. This paper introduces a multisize sliding window workload estimation technique for dynamic power management (DPM) in nonstationary environments. This technique reduces both the effects of identification delay and sampling error present in the previous fixed-size sliding window approach. The system is modeled by discrete-time Markov chains and the model offers a rigorous mathematical formulation of the problem and allows one to obtain an excellent trade-off between performance and power consumption. [J71]

"Energy-Recycling (ER) Technique for a Direct-Lit Intelligent Power Management Backlight Unit (BLU)"

A field-sequential-color (FSC) liquid crystal display (LCD) technique with a direct-lit red, green, and blue LED backlight driver is proposed to achieve low weight, thin, perfect image quality, and low-power consumption of LCD television. The FSC technique performs a pseudorandom color sequence in the spatial and temporal domains to reduce color-breakup and motion-blur effects. The direct-lit RGB-LED backlight driver increases brightness, contrast, and uniformity due to the removal of a color filter. In this paper, the proposed FCS-LCD controller uses a single LED driver to switch the driving voltage alternatively between 36 V for driving 12-series G- or B-LEDs and 24 V for 12-series R-LEDs. The proposed energy-recycling technique can harvest the extra energy when the driving voltage switches from 36 to 24 V. Experimental results show that energy saving is higher than 17% of the conventional driving method. [J72]

"Electrostatic Precipitator Control Systems"

Enhancing precipitation efficiency using conventional and fuzzy logic control. Modern high-voltage (HV) power supplies based on fast switching devices such as insulated-gate bipolar transistors (IGBTs) increases the performance of the corona power of electrostatic precipitators (ESPs), resulting in improved gas cleaning and higher performance of the ESP. Unfortunately, increased energy consumption of the precipitator requires a higher amount of electricity to be generated the power station, which results in higher CO2emissions, With both centralized and decentralized control algorithms, the total energy consumption of an ESP can be significantly reduced while achieving low dust-emission values. The control system operates with a few input signals only and has been linked and extended to the plate-rapping system. Power savings depend on the operating conditions, and experiments have shown an average savings in the range of 30-60% within a longer period of operation. [J73]

"System-Level Energy Optimization for Error-Tolerant Image Compression"

Based on the natural error tolerance of image and multimedia processing, aggressive voltage scaling has been considered for energy savings by trading off accuracy. However, aggressive voltage scaling in image compression may not reduce overall system energy consumption because of the reduction in the compression ratio. Based on the system-level analysis, we present an adaptive pixel and coefficient truncation technique to successfully reduce error rates so that we can achieve great energy savings without significant quality degradation. Our experimental results show that average energy savings of up to 40% can be realized at a trivial implementation cost. [J74]

"Efficient Power Management for Infrastructure IEEE 802.11 WLANs"

To achieve a long run-time for battery-operated portable electronic devices that incorporate wireless transceivers, efficient power management of the radio is a critical requirement. The power management function of IEEE 802.11 wireless local area networks (WLANs) allows stations (STAs) to operate in the doze mode so that their power consumption is significantly reduced. Hence, efficient algorithms to manage when and how often a STA enters and exits doze mode are crucial to battery-operated STAs. We address this problem by developing a novel model for stochastic analysis of timer-based power management in infrastructure IEEE 802.11 WLANs.

Based on this model, the probabilities that a STA is active, idle, or dozing are derived, and the power consumption of the STA, number of frames buffered, and average delay per frame are obtained. These results enable an efficient power management algorithm that optimizes the idle timer and doze duration at the STA and the frame buffer at the access point. Moreover, similar statistics for the basic power management method in the IEEE 802.11 standard are derived as a special case of the proposed timer-based power management scheme. Numerical results are presented to demonstrate the effectiveness of the proposed algorithms. [J75]

"Statistical Control Approach for Sleep-Mode Operations in IEEE 802.16m Systems"

The power-saving class of type I (PSC I), which is one of the sleep-mode operations specified in the IEEE 802.16 e standard, is designed to reduce power consumption for nonreal-time traffic. However, the inefficiency of the PSC I comes from the configuration of its operation and the utilized mechanism of binary-exponential traffic detection. Based on the concepts of IEEE 802.16 m sleep-mode operation, a statistical sleep window control (SSWC) approach is proposed to improve the energy efficiency of a mobile station (MS) with nonreal-time downlink traffic in this paper. The SSWC approach constructs a discrete-time Markov-modulated Poisson process (dMMPP) for representing the states of nonreal-time traffic. Furthermore, a partially observable Markov decision process (POMDP) is exploited within the SSWC approach to conjecture the present traffic state. Based on the estimated traffic state and the considerations of tolerable delay and/or queue size, two suboptimal policies, including the sleep ratio-based (SR) and energy cost-based (EC) policies, are proposed within the SSWC approach. The efficiency of the proposed SSWC approach is evaluated and compared via simulations. Simulation results show that the proposed SSWC approach outperforms the conventional IEEE 802.16 e PSC I and the evolutional PSC I of the IEEE 802.16 m system in terms of both energy conservation and packet delay. [J76]

"IEEE 802.15.5 WPAN mesh standard-low rate part: Meshing the wireless sensor networks"

This paper introduces a new IEEE standard, IEEE 802.15.5,which provides mesh capability for wireless personal area network (WPAN) devices. The standard provides an architectural framework enabling WPAN devices to promote interoperable, stable, and scalable wireless mesh topologies. It is composed of two parts: low-rate WPAN mesh and high-rate WPAN mesh. In this paper, we present only low-rate WPAN mesh because it is designed to support wireless sensor networks. IEEE 802.15.5 low-rate part is a light-weight scalable mesh routing protocol that caters well to the requirements of resource-constrained wireless sensor networks. By binding logical addresses to the network topology, IEEE 802.15.5 obviates the need for route discovery. This eliminates the initial route discovery latency, saves storage space and reduces the communication overhead and energy consumption. A distributed link state scheme is further built atop the block addressing scheme to improve the quality of routes, robustness, and load balancing. The routing scheme scales well with regard to various performance metrics. The standard also provides enhanced functions such as multicast, reliable broadcast, power saving, time synchronization, route tracing and portability. We also present the performance evaluation of major functions performed with a 50-nodes tested deployed over a whole floor (100 Ч 140 ft2) at CUNY Engineering building. The results testify that the IEEE 802.15.5 will serve well for wireless personal area networks and wireless sensor networks. [J77]

"A Biased Random Walk Routing Protocol for Wireless Sensor Networks: The Lukewarm Potato Protocol"

Low-latency data delivery is an important requirement for achieving effective monitoring through wireless sensor networks. When sensor nodes employ duty cycling, sending a message along the shortest path, however, does not necessarily result in minimum delay. In this paper, we first study the lowest latency path problem, i.e., the characteristics of a path with minimum delay that connects a source node to the sink under random duty cycling nodes. Then, we propose a forwarding protocol based on biased random walks, where nodes only use local information about neighbors and their next active period to make forwarding decisions. We refer to this as lukewarm potato forwarding. Our analytical model and simulation experiments show that it is possible to reduce path latency without significantly increasing the number of transmissions (energy efficiency) needed to deliver the message to the destination. In particular, although deviating from the shortest path requires additional transmissions, and hence, higher energy consumption, this increase is compensated by a lighter duty cycle. Our experiments show that, overall, we can save up to 15 percent of energy while obtaining the same data delivery delay as shortest path routing. Additionally, the proposed solution is tunable. By changing the value of just one threshold parameter, it can be tuned to operate anywhere in the continuum from hot potato/random walk forwarding protocol to a deterministic shortest path forwarding protocol. [J78]

"Remote-controllable and energy-saving room architecture based on ZigBee communication"

This paper proposes remote-controllable and energy-saving room architecture to reduce standby power consumption and to make the room easily controllable with an IR remote control of a home appliance. To realize the proposed room architecture, we proposed and designed the automatic standby power cut-off outlet and a ZigBee controller with IR code learning functionality. The proposed power outlet monitors the power consumption for the predetermined time and completely cuts off the power supply when the monitored power is below the threshold. This power outlet has a function of changing the threshold power, which enables any kinds of home appliances to be applied to the power outlet. To efficiently manage the power outlets and the lights, we proposed the ZigBee controller with IR code learning functionality. The ZigBee controller has several onboard buttons to wake up the power outlets and control the dimming light. By using IR code learning functionality, the ZigBee controller can assign a certain IR code of a remote control of a home appliance to the power outlet or the dimming light. A user can control the power outlets and the dimming light with an IR remote control of any home appliance. Our proposed room architecture provides the remote-controllable and energy-saving room. [J79]

"Energy-Efficient Dynamic Instruction Scheduling Logic Through Instruction Grouping"

Dynamic instruction scheduling logic is quite complex and dissipates significant energy in microprocessors that support superscalar and out-of-order execution. We propose a novel microarchitectural technique to reduce the complexity and energy consumption of the dynamic instruction scheduling logic. The proposed method groups several instructions as a single issue unit and reduces the required number of ports and the size of the structure. This paper describes the microarchitecture mechanisms and shows evaluation results for energy savings and performance. These results reveal that the proposed technique can greatly reduce energy with almost no performance degradation, compared to the conventional dynamic instruction scheduling logic. [J80]

"The Transition to Solid-State Lighting"

Lighting constitutes more than 20% of total U.S. electricity consumption, a similar fraction in the European Union, and an even higher fraction in many developing countries. Because many current lighting technologies are highly inefficient, improved technologies for lighting hold great potential for energy savings and for reducing associated greenhouse gas emissions. Solid-state lighting shows great promise as a source of efficient, affordable, color-balanced white light. Indeed, assuming market discount rates, engineering-economic analysis demonstrates that white solid-state lighting already has a lower levelized annual cost (LAC) than incandescent bulbs. The LAC for white solid-state lighting will be lower than that of the most efficient fluorescent bulbs by the end of this decade. However, a large literature indicates that households do not make their decisions in terms of simple expected economic value. After a review of the technology, we compare the electricity consumption, carbon emissions, and cost-effectiveness of current lighting technologies, accounting for expected performance evolution through 2015. We then simulate the lighting electricity consumption and implicit greenhouse gases emissions for the U.S. residential and commercial sectors through 2015 under different policy scenarios: voluntary solid-state lighting adoption, implementation of lighting standards in new construction, and rebate programs or equivalent subsidies. Finally, we provide a measure of cost-effectiveness for solid-state lighting in the context of other climate change abatement policies. [J81]

"A Novel Scheduled Power Saving Mechanism for 802.11 Wireless LANs"

Power conservation is a general concern for mobile computing and communication. In this paper, we investigate the performance of the current 802.11 power saving mechanism (unscheduled PSM) and identify that background network traffic can have a significant impact on the power consumption of mobile stations. To improve power efficiency, a novel scheduled PSM protocol based on time slicing is proposed in this paper. The protocol adopts the mechanism of time division, schedules the access point to deliver pending data at designated time slices, and adaptively adjusts the power state of the mobile stations. The proposed scheme is near theoretical optimal for power saving. It greatly reduces the effect of background traffic, minimizes the station idle time, and maximizes its energy utilization. Comprehensive analysis and simulations are conducted to evaluate the new protocol. The results show that the new protocol provides significant energy saving over the unscheduled PSM, particularly in circumstances where multiple traffic streams coexist in a network. Moreover, it achieves the saving at the cost of only a slight degradation of the one-way-delay performance. [J82]

"Energy-Efficient Video Transmission Over a Wireless Link"

Energy minimization is an important design goal in wireless video transmission. We examine how the RF energy and the analog circuit energy, which account for a large part of the energy consumption for wireless video transmission, can be controlled with physical-layer parameters (e.g., modulation level, bit rate, bit error rate, and multiple access interference) and link-layer specifications (e.g., the buffer status, idle time, and active time). Building on these insights, we develop three energy-efficient video transmission schemes for the single-user

system, i.e., frame-by-frame transmission, group of pictures (GOP)-by-GOP transmission, and client-buffer-related energy-efficient video transmission (CBEVT). Our simulations indicate that energy savings of up to 85% is achievable in the radio frequency (RF) front end using the CBEVT algorithm. We also present an energy-efficient optimal smoothing algorithm for reducing the RF front-end energy consumption and the peak data rate. For CDMA-based multiuser systems, we propose an RF front-end energy model that assumes perfect power control. We find the signal-to-interference-noise ratio (SINR) for the entire system that minimizes the total energy consumption. We propose the multiuser-based energy-efficient video transmission (MBEVT) algorithm, which can achieve energy savings of up to 38% for a six-user CDMA system with an independent 16-MB buffer for every uplink. [J83]

"Joint Beamforming and Power Control for Multiantenna Relay Broadcast Channel With QoS Constraints"

This paper studies the two-hop relay broadcast channel (BC) for a relay-assisted wireless cellular network where the multiuser independent downlink signals from the base station (BS) are first transmitted to a fixed relay station (RS), and then forwarded by the RS to multiple mobile users. Assuming both the BS and RS are equipped with multiantennas, we study the joint optimization of linear beamforming and power control at the BS and RS so as to minimize their weighted sum-power consumption under the user minimum signal-to-interference-noise-ratio (SINR)-quality-of-service (QoS)-constraints. We apply two well-known criteria in the literature, namely, the ldquoSINR balancingrdquo and the ldquochannel-inversion,rdquo for the design of linear precoding in the traditional nonrelay-assisted multiantenna BC to the relay-assisted multiantenna BC. First, a convergence-ensured iterative SINR-balancing algorithm is proposed to successively in turn optimize the transmit parameters at one station (BS or RS) with those at the other station being fixed. Second, a joint BS and RS channel-inversion algorithm is proposed together with a novel technique, termed ldquoeigenmode switching,rdquo at the RS to reduce the power penalty of the channel inversion. Simulation results show that the proposed joint beamforming and power control schemes provide substantial power savings to achieve the assigned user QoS constraints. [J84]

"An Adaptive Interleaving Technique for Memory Performance-per-Watt Management"

With the increased complexity of platforms coupled with data centers' servers sprawl, power consumption is reaching unsustainable limits. Researchers have addressed data centers' performance-per-watt management at different hierarchies going from server clusters to servers to individual components within the server platform. This paper addresses performance-per-watt maximization of memory subsystems in a data center. Traditional memory power management techniques rely on profiling the utilization of memory modules and transitioning them to some low-power mode when they are sufficiently idle. However, fully interleaved memory presents an interesting research challenge because data striping across memory modules reduces the idleness of individual modules to warrant transitions to low-power states. In this paper, we present a novel technique for performance-per-watt maximization of interleaved memory by dynamically reconfiguring (expanding or contracting) the degree of interleaving to adapt to incoming workload. The reconfigured memory hosts the application's working set on a smaller set of modules in a manner that exploits the platform's memory hierarchy architecture. This creates the opportunity for the remaining memory modules to transition to low-power states and remain in those states for as long as the performance remains within given acceptable thresholds. The memory power expenditure is minimized subject to application memory requirements and end-to-end memory access delay constraints. This is formulated as a performance-per-watt maximization problem and solved using an analytical memory power and performance model. Our technique has been validated on a real server using SPECjbb benchmark and on a trace-driven memory simulator using SPECjbb and gcc memory traces. On the server, our techniques are shown to give about 48.8 percent (26.7 kJ) energy savings compared to traditional techniques measured at 4.5 percent. The maximum improvement in performance-per-wa--tt was measured at 88.48 percent. The simulator showed 89.7 percent improvement in performance-per-watt compared to the best performing traditional technique. [J85]

"Block-Layout Design Using MAX-MIN Ant System for Saving Energy on Mass Rapid Transit Systems"

This paper presents a method of block-layout design between successive stations for mass rapid transit systems (MRTSs). The aim is to save energy under the framework of the fixed-block signaling (FBS) system and the equi-block principle. Unlike past research regarding the energy savings of train operation, this paper proposes a combinatorial optimization model to reduce the computation time. In the presented approach, the problem of minimizing the energy consumption between successive stations is first formulated as a combinatorial optimization problem. Then, the train-speed trajectory for saving energy is optimized by a MAX-MIN ant system (MMAS) of ant colony optimization (ACO) algorithms. Finally, the block layout is designed in accordance with the shortest block length under the equi-block principle. It is shown that the method presents a significant

improvement for the reduction of computational burden on the block-layout design. The feasibility and benefits are verified via simulation study. Analyses and discussions are also given. [J86]

"Memory MISER: Improving Main Memory Energy Efficiency in Servers"

Main memory power in volume and mid-range servers is growing as a fraction of total system power. The resulting energy consumption increases system cost and the heat produced reduces reliability. Emergent memory technology will provide systems with the ability to dynamically turn-on (online) and turn-off (offline) memory devices at runtime. This technology, coupled with slack in memory demand, offers the potential for significant energy savings in servers. However, to gain general acceptance in the server community, power-aware techniques must maintain performance and scale to thousands of memory devices. We propose a memory management infra-structure for energy reduction (Memory MISER) that is transparent, performance-neutral, and scalable. Memory MISER provides: 1) a prototype Linux kernel that manages memory at device granularity, and 2) a user space daemon that tracks systemic memory demand and implements energy- and performance-constrained device controller policies. Experiments on an 8-node cluster of servers show our Memory MISER conserves memory energy up to 56.8 percent with no performance degradation for scientific codes that utilized the entire cluster. For multi-user workloads, we achieved memory energy savings of up to 67.94 percent with no performance degradation. Normalizing to total system energy consumption, our power-aware memory approach reduced energy between 18.81 percent and 39.02 percent. [J87]

"Extended maximizing unavailability interval (eMUI): maximizing energy saving in IEEE 802.16e for mixing type I and type II PSCs"

To conserve energy in IEEE 802.16e, earlier, we proposed maximizing unavailability interval (MUI) for type II power saving class (PSC). MUI is guaranteed to find the maximum unavailability interval. Therefore, energy consumption can be reduced significantly. In this paper, we further extend MUI for the mixture of Type I and Type II PSCs. The proposed eMUI still can achieve maximum unavailability interval. The simulation results show that the proposed eMUI reduces energy consumption and average packet response time. [J88]

"An Adaptive Partitioning Scheme for Sleep Scheduling and Topology Control in Wireless Sensor Networks"

This paper presents an adaptive partitioning scheme of sensor networks for node scheduling and topology control with the aim of reducing energy consumption. Our scheme partitions sensors into groups such that a connected backbone network can be maintained by keeping only one arbitrary node from each group in active status while putting others to sleep. Unlike previous approaches that partition nodes geographically, our scheme is based on the measured connectivity between pairwise nodes and does not depend on nodes' locations. In this paper, we formulate node scheduling with topology control as a constrained optimal graph partition problem, which is NP-hard, and propose a Connectivity-based Partition Approach (CPA), which is a distributed heuristic algorithm, to approximate a good solution. We also propose a probability-based CPA algorithm to further save energy. CPA can ensure K-vertex connectivity of the backbone network, which achieves the trade-off between saving energy and preserving network quality. Moreover, simulation results show that CPA outperforms other approaches in complex environments where the ideal radio propagation model does not hold. [J89]

"A Stochastic Optimization Approach to Rating of Energy Storage Systems in Wind-Diesel Isolated Grids"

Wind-diesel systems represent a proactive step towards sustainable remote communities. However, for high ratios of wind energy, the necessity of a dump load and the diesel operating constraints need to be considered. Energy storage systems offer a means of optimizing energy use and further reducing consumption of diesel fuel. This paper proposes a methodology for storage sizing based on stochastic optimization. The problem is formulated and solved using representative data. The dependence of storage sizing and the cost of delivered energy on wind penetration levels, storage efficiency, and diesel operating strategies are considered. Results demonstrate that for high wind penetration, the availability of storage, together with an appropriate diesel operating approach, can result in significant cost savings in terms of fuel and operating costs. [J90]

"Frequent-Pattern-Guided Multilevel Decomposition of Behavioral Specifications"

Conventional high-level synthesis algorithms treat specification operations as atomic elements that are executed in one or several consecutive cycles and over one functional unit. However, in most specifications, there exist different types, representations, and widths of operations that, handled at different decomposition levels, may produce better designs. In this way, most arithmetic operations can be decomposed into smaller operations,

applying several arithmetical properties. Different decompositions can be performed in order to improve the performance or reduce the area or power consumption. In this paper, we propose a pattern-based design methodology that is able to treat every operation at its most appropriate decomposition level. It produces reduced datapaths while meeting specified time constraints. In comparison to conventional algorithms, the amount of area saved averages 40%. [J91]

"iVisual: An Intelligent Visual Sensor SoC With 2790 fps CMOS Image Sensor and 205 GOPS/W Vision Processor"

iVisual, an intelligent visual sensor SoC integrating 2790 fps CMOS image sensor and 76.8 GOPS, 374 mW vision processor, is implemented on a 7.5 mm Ч 9.4 mm die in a UMC 0.18 mum CMOS Image Sensor process. Light-in, answer-out SoC architecture is adopted to avoid possible privacy problems. A feature processor is designed to eliminate the dataflow mismatch between processor array and scalar processor to increase 36% of average throughput. To increase hardware utilization, an inter-processor synchronization scheme is adopted to increase 23% of average throughput. Memory access is reduced by 94% to save 726 mW of power consumption. A bitplane-based single port memory structure is adopted to reduce SRAM area. The 205 GOPS/W power efficiency and 1.16 GOPS/mm2area efficiency are therefore achieved by use of the proposed techniques. [J92]

"Systematic Design and Modeling of a OTA-C Filter for Portable ECG Detection"

This study presents a systematic design of the fully differential operational transconductance amplifier-C (OTA-C) filter for a heart activities detection apparatus. Since the linearity and noise of the filter is dependent on the building cell, a precise behavioral model for the real OTA circuit is created. To reduce the influence of coefficient sensitivity and maintain an undistorted biosignal, a fifth-order ladder-type lowpass Butterworth is employed. Based on this topology, a chip fabricated in a 0.18- mum CMOS process is simulated and measured to validate the system estimation. Since the battery life and the integration with the low-voltage digital processor are the most critical requirement for the portable diagnosis device, the OTA-based circuit is operated in the subthreshold region to save power under the supply voltage of 1V. Measurement results show that this low-voltage and low-power filter possesses the HD3 of -48.9 dB, dynamic range (DR) of 50 dB, and power consumption of 453 nW. Therefore, the OTA-C filter can be adopted to eliminate the out-of-band interference of the electrocardiogram (ECG) whose signal bandwidth is located within 250 Hz. [J93]

"Fast Configurable-Cache Tuning With a Unified Second-Level Cache"

Tuning a configurable cache subsystem to an application can greatly reduce memory hierarchy energy consumption. Previous tuning methods use a level one configurable cache only, or a second level with separate instruction and data configurable caches. We instead use a commercially-common unified second level cache, a seemingly minor difference that actually expands the configuration space from 500 to about 20 000. We develop additive way tuning for tuning a cache subsystem with this large space, yielding 61% energy savings and 9% performance improvements over a nonconfigurable cache, greatly outperforming an extension of a previous method. [J94]

"Energy Management Analysis and Enhancement in IEEE 802.16e WirelessMAN"

One strategy for energy management is an indispensable component in the emerging IEEE 802.16e wireless metropolitan area networks (WirelessMAN) supporting mobility. An efficient energy saving mechanism is the basis for the guarantee of a long operating lifetime for a mobile subscriber station (MSS), because MSSs are normally powered by rechargeable batteries. In this paper, we will characterize and model the energy-saving scheme in the IEEE 802.16e WirelessMAN. A comprehensive analysis is performed to study the specified sleep mode with generalized traffic processes. The performance metrics are derived with respect to energy consumption and packet delay to evaluate the tradeoff in the energy management strategy. We then propose an enhanced scheme to offer favorable performance tradeoff by adaptively adjusting the sleep windows. The numerical result indicates that the new policy can significantly reduce power consumption. Simulation results are presented to validate the analytical model, which provides potential guidelines for the efficient management of limited energy. [J95]

"RandomCast: An Energy-Efficient Communication Scheme for Mobile Ad Hoc Networks"

In mobile ad hoc networks (MANETs), every node overhears every data transmission occurring in its vicinity and thus, consumes energy unnecessarily. However, since some MANET routing protocols such as dynamic source routing (DSR) collect route information via overhearing, they would suffer if they are used in combination with 802.11 PSM. Allowing no overhearing may critically deteriorate the performance of the underlying routing

protocol, while unconditional overhearing may offset the advantage of using PSM. This paper proposes a new communication mechanism, called RandomCast, via which a sender can specify the desired level of overhearing, making a prudent balance between energy and routing performance. In addition, it reduces redundant rebroadcasts for a broadcast packet, and thus, saves more energy. Extensive simulation using NS-2 shows that RandomCast is highly energy-efficient compared to conventional 802.11 as well as 802.11 PSM-based schemes, in terms of total energy consumption, energy goodput, and energy balance. [J96]

"Information Content-Based Sensor Selection and Transmission Power Adjustment for Collaborative Target Tracking"

For target tracking applications, wireless sensor nodes provide accurate information since they can be deployed and operated near the phenomenon. These sensing devices have the opportunity of collaboration among themselves to improve the target localization and tracking accuracies. An energy-efficient collaborative target tracking paradigm is developed for wireless sensor networks (WSNs). A mutual-information-based sensor selection (MISS) algorithm is adopted for participation in the fusion process. MISS allows the sensor nodes with the highest mutual information about the target state to transmit data so that the energy consumption is reduced while the desired target position estimation accuracy is met. In addition, a novel approach to energy savings in WSNs is devised in the information-controlled transmission power (ICTP) adjustment, where nodes with more information use higher transmission powers than those that are less informative to share their target state information with the neighboring nodes. Simulations demonstrate the performance gains offered by MISS and ICTP in terms of power consumption and target localization accuracy. [J97]

"Nanomechanical switches for power saving in CMOS applications"

The performance of a nanomechanical switch for integration with complementary metal-oxide-semiconductor electronics to reduce idle power consumption is presented. The DC performance shows a leakage current less than 100 fA, a through current of 10 A, and 1 mV/decade subthreshold slope. The operating voltage of the switch was approximately 13.2 V. The switch closure was measured at approximately 100 s, while the switch open was measured at less than 100 ns. A path forward is presented to reduce the operating voltage of future switches to 3.7 V and decrease the switching time to 27 ns. [J98]

"Intelligent power management device with middleware based living pattern learning for power reduction"

This paper presents design and implementation of intelligent power management devices using user location, user motion detection and user living patterns in home networks. Our design integrates the device to be controlled, the intelligent power management device (iPMD), and the adaptive light-weight middleware so that it can be used with minimal power consumption for a wide range of applications. iPMD which will be installed in every power outlet in a home, is made up of five blocks: the pyroelectric infrared (PIR) sensor circuit, the light sensor circuit, the microprocessor, the power meter with a LED display and the PLC module. iPMD detects if a human body enters the detection area or not. If there is no human body present, all controlled appliances are turned off and iPMDs help reduce standby power consumption. If there is, the iPMD detects the light intensity under the environment and maintains sufficient light by controlling the nearby lights. An iPMD transmits and receives the sensor data from nearby iPMDs so the IPG can control different lights and appliances in different regions. iPMDs also communicate with the lightweight middleware at an intelligent power gateway (IPG) that adaptively reason the optimal power control by analyzing user living pattern from the sensing data from devices. The experimental results obtained from the real apartments show that the total power consumption can be reduced up to 7.5 %. [J99]

"Performance study and system optimization on sleep mode operation in IEEE 802.16e"

Energy efficiency in mobile devices remains a critical issue in the design of wireless communication system. In order to provide a high quality of service (QoS), the IEEE 802.16e-2005 standard supports three unique power saving classes (PSCs) which aim to reduce the power consumption of mobile devices based on the different types of traffic. Our goal is to design an optimal sleep mode selection scheme so as to maximize the energy efficiency in a mobile WiMAX system while providing a certain QoS guarantee. In this paper, we propose a theoretical framework based on the semi-Markov decision process along with a performance evaluation on the sleep mode operation. Based on this model, we formulate a stochastic optimization problem and solve it through our novel policy optimization algorithm, which is capable of finding the optimal policy for the selection of different PSCs. The numerical and simulation results demonstrate the validity of our proposed scheme under different QoS requirements such as the packet delay and energy consumption level. We believe that our scheme has achieved a high energy efficiency and is best fit to the IEEE 802.16e mobile system. [J100]

"A lightweight and energy-efficient architecture for wireless sensor networks"

This paper presents a novel architecture designed for low power consumption, in which low computational complexity and reliability have also been important design constraints. It is suitable for sensor-actuator systems, is based on IEEE 802.15.4 and constitutes a more lightweight alternative than Zigbee. We provide a vision of how we have solved some problems that are out of the scope of IEEE 802.15.4 like addressing scheme, topology control, multi-hop synchronization, tasks scheduling, application data model, and other points related to software and hardware considered to extend the battery life. We have designed a centralized method for scheduling the beacon transmission time. Unlike the distributed one used by Zigbee, our method avoids beacon overlapping in any case and does not require the publication of information in the beacon payload. The proposed addressing scheme also does not require the publication of the depth of coordinators. Both methods allow us to implement efficient algorithms, reduce the memory used to store the network tables, and shorten the beacon payload, what entails a significant energy saving. These solutions together with others presented in this paper allow us to reach a battery life longer than 31 months for sensors and 42 months for actuators. [J101]

"Multicore Processing and Efficient On-Chip Caching for H.264 and Future Video Decoders"

Performance requirements for video decoding will continue to rise in the future due to the adoption of higher resolutions and faster frame rates. Multicore processing is an effective way to handle the resulting increase in computation. For power-constrained applications such as mobile devices, extra performance can be traded-off for lower power consumption via voltage scaling. As memory power is a significant part of system power, it is also important to reduce unnecessary on-chip and off-chip memory accesses. This paper proposes several techniques that enable multiple parallel decoders to process a single video sequence; the paper also demonstrates several on-chip caching schemes. First, we describe techniques that can be applied to the existing H.264 standard, such as multiframe processing. Second, with an eye toward future video standards, we propose replacing the traditional raster-scan processing with an interleaved macroblock ordering; this can increase parallelism with minimal impact on coding efficiency and latency. The proposed architectures allow Nparallel hardware decoders to achieve a speedup of up to a factor of N. For example, if N=3, the proposed multiple frame and interleaved entropy slice multicore processing techniques can achieve performance improvements of 2.64times and 2.91times, respectively. This extra hardware performance can be used to decode higher definition videos. Alternatively, it can be traded-off for dynamic power savings of 60% relative to a single nominal-voltage decoder. Finally, on-chip caching methods are presented that significantly reduce off-chip memory bandwidth, leading to a further increase in performance and energy efficiency. Data-forwarding caches can reduce off-chip memory reads by 53%, while using a last-frame cache can eliminate 80% of the off-chip reads. The proposed techniques were validated and benchmarked using full-system Verilog hardware simulations based on an existing decoder; they should--also be applicable to most other decoder architectures. The metrics used to evaluate the ideas in this paper are performance, power, area, memory efficiency, coding efficiency, and input latency. [J102]

"Resilient Self-V -Tuning Scheme With Speed-Margining for Low-Power SRAM"

Lowering the supply voltage is an effective way to significantly reduce the power consumption of a static random access memory (SRAM). However, the minimum supply voltage (Vminf) required to support a given operating frequency in an SRAM macro is often elusive from one chip to another due to process variations. Moreover, temperature could vary when an SRAM macro is in operation, and thus exacerbating the problem since temperature variation could affect the Vminf. In this paper, we propose an on-chip self-VDD-tuning scheme that automatically adjusts each manufactured SRAM macro to a minimal voltage near its Vminf. Our scheme can provide a user-specified speed margin (e.g., 10% of the target frequency), and thereby creating a guard band for assuring robust operations over a wide range of temperatures. Simulation results show that, with the proposed speed margining technique, a 64 Kb SRAM macro can tolerate temperature up to 125degC. Measurement results from a test chip in a 0.18-mum CMOS process also demonstrate that we can achieve 40% power savings for an 8 Kb SRAM macro operating at 150 MHz by means of this resilient self-VDD-tuning. [J103]

"Tiny module-linking for energy-efficient reprogramming in wireless sensor networks"

The remote and automatic reprogramming is an indispensable part in the wireless sensor networks. Especially, the energy saving problem is an important challenge because of a limited energy characteristics. Many kinds of conventional researches about reprogramming have tried to solve the energy saving problem. But they do not consider the energy consumption model and still have inefficient memory access times. In this paper, we propose a tiny module-linking scheme. It performs module relocation to decrease program code shifts and connects the relocated module with a tiny module-linker to eliminate module caller changes. This proposed scheme reduces access times to Electrically Erasable Programmable Read-Only Memory (EEPROM) and program memory during

the decoding procedure of the reprogramming. Experimental results show that our scheme outperforms the previous reprogramming schemes in terms of the energy consumption. [J104]

"Exploiting flash memory for reducing disk power consumption in portable media players"

Portable media players are increasingly using hard disk drives (HDD) to meet their storage requirements, but HDDs consume a significant amount of energy. Therefore video frames are prefetched into dynamic random access memory (DRAM) to allow the disk to go into low-power mode; but most mobile systems have limited DRAM, so little energy is actually saved in this way. We propose two new energy saving schemes: one improves the utilization of DRAM in storing prefetched frames, and the other extends this approach by making use of auxiliary flash memory. Simulations show that deploying a reasonable amount of auxiliary flash reduces disk energy consumption by up to 86% compared with conventional prefetching schemes. [J105]

"TelecomI+D09: Dynamic management of ICT service infrastructures for energy efficiency optimization"

Improving the energy efficiency of ICT service provisioning infrastructures presents many advantages, both from the corporate social responsibility and from the business competitiveness perspective. In this context, reducing data center energy consumption is one of the main tasks to focus on, since these facilities concentrate a great share of an ICT service provider's power demand in a small number of locations. The adoption of commercial energy-saving solutions, based on static configurations, introduces significant improvements, but considerable infrastructure underutilization levels remain. In order to allow ICT service providers to overcome the limitations found in existing energy efficiency tools, this paper describes an infrastructure management solution which dynamically adjusts the performance of the managed environment to match service demand, thus optimizing energy consumption. Additionally, the first validation experiences of the proposed management solution in the context of a telecom operator's service provisioning infrastructure are described. [J106]

"Integrated energy analysis of error correcting codes and modulation for energy efficient wireless sensor nodes"

Optimizing energy consumption is a key objective in designing wireless sensor nodes. It has been shown earlier that the node energy is strongly influenced by the modulation and the error correcting code (ECC) used. The utility of using ECC from an energy perspective is determined by the energy saving due to the ECC coding gain vis-a-vis the energy overhead of "redundant" bits and of energy saving. Furthermore, the node energy varies with the change in errorcorrecting capability and code word length of a particular ECC as well as the modulation constellation size. The ECC coding gain is influenced by the constellation size. In this paper, the node energy variations with ECC and modulation parameters are analyzed for an energy optimal node design for the nodes operating in the additive white Gaussian noise channel. Based on this analysis, we compute the per information bit node energy and this is used to select an "optimal" ECC and modulation scheme pair. Our results show that the energy optimal ECC-modulation pair selected for some specific operating conditions could save as much as 50% energy. In nutshell, our work is targeted towards reducing the search space and finding an energy optimal ECC modulation pair for the given environment and application. [J107]

"An Optimal Solution for the Heterogeneous Multiprocessor Single-Level Voltage-Setup Problem"

A heterogeneous multiprocessor (HeMP) system consists of several heterogeneous processors, each of which is specially designed to deliver the best energy-saving performance for a particular category of applications. A low-power real-time scheduling algorithm is required to schedule tasks on such a system to minimize its energy consumption and complete all tasks by their deadlines. Existing works assume that processor speeds are known as a prioriand cannot deliver the optimal energy-saving performance. The problem of determining the optimal voltage for each processor to minimize the total energy consumption is called a voltage-setup problem. To the best of our knowledge, this is the first paper to propose the optimal solution for the HeMP single-level voltage-setup problem. This paper provides an optimal solution for the HeMP single-level voltage-setup problem. We first formulate the problem as a nonlinear generalized assignment problem that has been proved to be nondeterministic polynomial-time hard (NP-hard). We next develop a pruning-based algorithm to obtain the optimal solution. A heuristic algorithm is also proposed to derive an approximate solution. After obtaining the optimal partition, each processor's speed is determined by its final workload. In our simulations, we model more than a couple dozens of off-the-shelf embedded processors including ARM processor and TI DSP. The results show that the pruning-based algorithm reduces the time needed to derive the optimal solution by at least 98%, compared with the exhaustive search. Also, our heuristic algorithm achieves the minimum energy consumption over existing works. [J108]

"Design and Analysis of A 5.3-pJ 64-kb Gated Ground SRAM With Multiword ECC"

This paper presents an SRAM architecture employing a multiword-based ECC (MECC) scheme for soft error mitigation and a row virtual ground technique for array leakage reduction. The MECC combines four data words to form a 128 bit composite ECC word, two of which are interleaved in a row to mitigate cosmic neutron-induced multi-bit errors. The use of a composite word reduces the number of check-bits by 68%, however, requires a unique write operation that updates the check-bits by writing one data word while reading the other three data words. The ground potential of the composite word is raised to a nonzero value during retention in order to limit the leakage power consumption. A critical charge-based soft error rate (SER) model is proposed to estimate the resulting increase in the SER. Both the MECC scheme and the SER model are verified by implementing a 64-kb SRAM macro in 90 nm CMOS technology. The SRAM consumes 5.34 pJ energy with a data latency of 3.3 ns, thus showing up to 82% per-bit energy saving and 8x speed improvement over previously reported multiword ECC schemes. Accelerated neutron radiation test of the SRAM confirms 85% soft error correction by the MECC and 90% accuracy of the SER model. [J109]

"Power Reduction of Asynchronous Logic Circuits Using Activity Detection"

Asynchronous circuits are well known for their benefits in terms of dynamic power savings because asynchronous logic does not switch when inactive. Nevertheless, in deep-submicron technologies, leakage currents have become an increasing issue, and thus, asynchronous circuits need to focus on static-power-consumption reduction. In this paper, we propose an innovative way to detect incoming asynchronous activity. Associated to an automatic power regulation, it efficiently reduces the supply voltage and, thus, both energy per operation and leakage currents. The proposed technique has been applied to an asynchronous network-on-chip node and successfully implemented in an ST Microelectronics CMOS 65-nm technology. [J110]

"A backlight dimming algorithm for low power and high image quality LCD applications"

A new backlight dimming algorithm is proposed to reduce power consumption of backlight and improve image quality in LCD applications. The proposed algorithm is consisted of two new techniques: the brightness modulation of the backlight and pixel compensation. The power saving ratio of four typical benchmarking images is 14-43% by using proposed brightness modulation algorithm. The proposed pixel compensation removes the clipping artifact and unnecessary luminance reduction. The proposed backlight dimming algorithm is demonstrated on 7-inch TFTLCD with LED backlight. [J111]

"Low-Power 32-bit Dual-MAC 120 W/MHz 1.0 V icyflex1 DSP/MCU Core"

A low-power programmable processor named icyflex1 was designed combining features of a digital signal processor (DSP) and a micro-controller unit (MCU). Implemented as a synthesizable VHDL software intellectual property core, the processor implements a broad range of power saving features including its customizable architecture and reconfigurable instruction set. Its performance is compared with other processors from the market and values are given for its integration in a 180 nm technology. The processor targets applications with tight power consumption constraints and correspondingly significant processing performance. [J112]

"An idle listening-aware energy efficient scheme for the DCF of 802.11n"

802.11 wireless local area network (WLAN) technology is now common in power sensitive devices like smart phones and personal digital assistants (PDAs). However, the energy efficiency of such devices will be very low, especially for next generation WLAN technology. The reasons for this include the existence of a large number of active stations, short data time and ultra high physical layer (PHY) data rate, which are the characteristics of next generation WLAN technology. This poor energy efficiency will be due to the fact that the device will consume a lot of idle-listening energy during the Distributed InterFrame Space (DIFS) and back-off time, and that the energy consumed for idle listening is similar to the energy consumed while receiving data. In this article, we propose an intelligent scheme for reducing the energy consumed in idle listening. Our analysis and simulation programs show that our scheme can lengthen the battery endurance due to the shortening in idle-listening time effectively especially when the number of active stations is large. An important characteristic of our scheme is that it is fully compatible with legacy Distributed Coordinated Function (DCF), and there will be no throughput reduction if this power saving scheme is applied to the DCF of 802.11. We also propose an accurate power consumption model in the MAC layer which to the best of our knowledge has not been presented in any earlier research. [J113]

"Compact Performance Models and Comparisons for Gigascale On-Chip Global Interconnect Technologies"

The on-chip global interconnect with conventional Cu/low-k and delay-optimized repeater scheme faces great challenges in the nanometer regime owing to its severe performance degradation. This paper describes the analytical models and performance comparisons of novel interconnect technologies and circuit architectures to cope with the interconnect performance bottlenecks. Carbon nanotubes (CNTs) and optics-based interconnects exhibit promising physical properties for replacing the current Cu/low-k-based global interconnects. We quantify the performance of these novel interconnects and compare them with Cu/low-k wires for future high-performance integrated circuits. The foregoing trends are studied with technology node and bandwidth density in terms of latency and power dissipation. Optical wires have the lowest latency and power consumption, whereas a CNT bundle has a lower latency than Cu. The new circuit scheme, i.e., "capacitively driven low-swing interconnect (CDLSI)," has the potential to effect a significant energy saving and latency reduction. We present an accurate analytical optimization model for the CDLSI wire scheme. In addition, we quantify and compare the delay and energy expenditure for not only the different interconnect circuit schemes but also the various future technologies, such as Cu, CNT, and optics. We find that the CDLSI circuit scheme outperforms the conventional interconnects in latency and energy per bit for a lower bandwidth requirement, whereas these advantages degrade for higher bandwidth requirements. Finally, we explore the impact of the CNT bundle and the CDLSI on a via blockage factor. The CNT shows a significant reduction in via blockage, whereas the CDLSI does not help to alleviate it, although the CDLSI results in a reduced number of repeaters due to the differential signaling scheme. [J114]

"Run-Time Adaptive Workload Estimation for Dynamic Voltage Scaling"

Dynamic voltage scaling (DVS) is a popular energy-saving technique for real-time tasks. The effectiveness of DVS critically depends on the accuracy of workload estimation, since DVS exploits the slack or the difference between the deadline and execution time. Many existing DVS techniques are profile based and simply utilize the worst-case or average execution time without estimation. Several recent approaches recognize the importance of workload estimation and adopt statistical estimation techniques. However, these approaches still require extensive profiling to extract reliable workload statistics and furthermore cannot effectively handle time-varying workloads. Feedback-control-based adaptive algorithms have been proposed to handle such nonstationary workloads, but their results are often too sensitive to parameter selection. To overcome these limitations of existing approaches, we propose a novel workload estimation technique for DVS. This technique is based on the Kalman filter and can estimate the processing time of workloads in a robust and accurate manner by adaptively calibrating estimation error by feedback. We tested the proposed method with workloads of various characteristics extracted from eight MPEG video clips. To thoroughly evaluate the performance of our approach, we used both a cycle-accurate simulator and an XScale-based test board. Our simulation result demonstrates that the proposed technique outperforms the compared alternatives with respect to the ability to meet given timing and Quality of Service constraints. Furthermore, we found that the accuracy of our approach is almost comparable to the oracle accuracy achievable only by offline analysis. Experimental results indicate that using our approach can reduce energy consumption by 57.5% on average, only with negligible deadline miss ratio (DMR) around 6.1%. Moreover, the average of computational overheads for the proposed technique is just 0.3%, which is the minimum value compared to other met--hods. More importantly, the DMR of our method is bounded by 11.7% in the worst case, while those of other methods are twice or more than ours. [J115]

"Power Management of Datacenter Workloads Using Per-Core Power Gating"

While modern processors offer a wide spectrum of software-controlled power modes, most datacenters only rely on dynamic voltage and frequency scaling (DVFS, a.k.a. P-states) to achieve energy efficiency. This paper argues that, in the case of datacenter workloads, DVFS is not the only option for processor power management. We make the case for per-core power gating (PCPG) as an additional power management knob for multi-core processors. PCPG is the ability to cut the voltage supply to selected cores, thus reducing to almost zero the leakage power for the gated cores. Using a testbed based on a commercial 4-core chip and a set of real-world application traces from enterprise environments, we have evaluated the potential of PCPG. We show that PCPG can significantly reduce a processor's energy consumption (up to 40%) without significant performance overheads. When compared to DVFS, PCPG is highly effective saving up to 30% more energy than DVFS. When DVFS and PCPG operate together they can save up to almost 60%. [J116]

"Delay analysis for sleep-based power saving mechanisms with downlink and uplink traffic"

In wireless networks, sleep-based power saving mechanisms can reduce the energy consumption at the expense of additional packet delay. This paper proposes a queueing model to analyze the packet queueing delay. Compared with the existing models which consider downlink traffic only, both downlink and uplink traffic are considered in the analysis. [J117]

"Toward Online Data Reduction for Portable Electroencephalography Systems in Epilepsy"

Portable EEG units are key tools in epilepsy diagnosis. Current systems could be made physically smaller and longer lasting by the inclusion of online data reduction methods to reduce the power required for storage or transmission of the EEG data. This paper presents a real-time data reduction algorithm based upon the discontinuous recording of the EEG: noninteresting background sections of EEG are discarded online, with only potentially diagnostically interesting sections being saved. MATLAB simulations of the algorithm on an EEG dataset containing 982 expert marked events in 4 days of data show that 90% of events can be correctly recorded while achieving a 50% data reduction. The described algorithm is formulated to have a direct, low power, hardware implementation and similar data reduction strategies could be employed in a range of body-area-network-type applications. [J118]

"Energy Minimization of Portable Video Communication Devices Based on Power-Rate-Distortion Optimization"

Portable video communication devices operate on batteries with limited energy supply. However, video compression is computationally intensive and energy-demanding. Therefore, one of the central challenging issues in portable video communication system design is to minimize the energy consumption of video encoding so as to prolong the operational lifetime of portable video devices. In this work, based on power-rate-distortion (P-R-D) optimization, we develop a new approach for energy minimization by exploring the energy tradeoff between video encoding and wireless communication and exploiting the nonstationary characteristics of input video data. Both analytically and experimentally, we demonstrate that incorporating the third dimension of power consumption into conventional R-D analysis gives us one extra dimension of flexibility in resource allocation and allows us to achieve significant energy saving. Within the P-R-D analysis framework, power is tightly coupled with rate, enabling us to trade bitsfor joulesand perform energy minimization through optimum bit allocation. We analyze the energy saving gain of P-R-D optimization. We develop an adaptive scheme to estimate P-R-D model parameters and perform online resource allocation and energy optimization for real-time video encoding. Our experimental studies show that, for typical videos with nonstationary scene statistics, using the proposed P-R-D optimization technology, the energy consumption of video encoding can be significantly reduced (by up to 50%), especially in delay-tolerant portable video communication applications. [J119]

"A Low-Power SRAM Using Bit-Line Charge-Recycling"

Low-power SRAM design is crucial since it takes a large fraction of total power and die area in high-performance processors. Reducing voltage swing of the bit-line is an effective way to save the power dissipation in write cycles. Voltage swing reduction of bit-lines is, however, limited due to possible write-failures. We propose a new low-power SRAM using bit-line charge recycling (CR-SRAM) for the write operation. In the proposed write scheme, differential voltage swing of a bit-line is obtained by recycled charge from its adjacent bit-line capacitance, instead of the power line. Applying such a charge recycling technique to the bit-line significantly reduces write power. A test chip with 32 Kbits (256 rows x 128 columns) is fabricated and measured in 0.13 mum CMOS to demonstrate operation of the proposed SRAM. Measurement results show 88% reduction in total power during write cycles compared to the conventional SRAM (CON-SRAM) at VDD= 1.5 V and f = 100 MHz. [J120]

"SEA: A Striping-Based Energy-Aware Strategy for Data Placement in RAID-Structured Storage Systems"

Many real-world applications need to frequently access data stored on large-scale parallel disk storage systems. On one hand, prompt responses to access requests are essential for these applications. On the other hand, however, with an explosive increase of data volume and the emerging of faster disks with higher power requirements, energy consumption of disk-based storage systems has become a salient issue. To achieve energy-conservation and prompt responses simultaneously, in this paper we propose a novel energy-aware strategy, called striping-based energy-aware (SEA), which can be integrated into data placement in RAID-structured storage systems to noticeably save energy while providing quick responses. Next, to illustrate the effectiveness of SEA, we implement two SEA-powered striping-based data placement algorithms, SEA0 and SEA5, by incorporating the SEA strategy into RAID-0 and RAID-5, respectively. Extensive experimental results demonstrate that compared with traditional non-stripping data placement algorithms, our algorithms significantly improve performance and save energy. Further, compared with an existing stripping-based data placement scheme, the two SEA-powered strategies noticeably reduce energy consumption with only a little performance degradation. [J121]

"A Mini-Invasive Long-Term Bladder Urine Pressure Measurement ASIC and System"

A mini-invasive system for long-term bladder urine pressure measurement system is presented. Not only is the design cost reduced, but also the reliability is enhanced by using a 1-atm canceling sensing instrumentation amplifier (IA). Because the urine pressure inside the bladder does not vary drastically, both the sleeping and working modes are required in order to save the battery power for long-term observation. The IA amplifies the signal sensed by the pressure sensor, which is then fed into the following analog-to-digital converter. Owing to the intrinsic 1-atm pressure existing inside the bladder, the IA must be able to cancel such a pressure from the signal picked up by the pressure sensor to keep the required linearity and the resolution for pressure measurement of the bladder urine. The pressure range of the proposed system is found out to be 14.7~19.7 Psi, which covers the range of all of the known unusual bladder syndromes or complications. [J122]

"Evaluation of low-energy and high-performance processor using variable stages pipeline technique"

A methodology for low-energy and high-performance computing that is essential in mobile and ubiquitous computing is proposed. The dynamic voltage scaling (DVS) is one of the current major methodologies for low-power devices. However by DVS, the lower the chip voltage becomes in the future, the less energy saving is obtained by DVS. Therefore in order to reduce the energy consumption for lower voltage devices, variable stages pipeline (VSP) processor with the latch D-FF selector (LDS)-cell that unifies pipeline stages dynamically and also decreases energy consumption caused by glitch propagations on a low- energy mode is proposed. With its features, the VSP technique can achieve low-energy computing without any dependence on chip voltage. It is shown that the VSP processor can achieve low-energy computing and higher performance computing than the DVS processor in the low-energy mode by evaluating the proposed approach using SpecINT2000 benchmark suite. [J123]

"Adaptive Channel Buffers in On-Chip Interconnection Networks— A Power and Performance Analysis"

Recent research in On-chip interconnection networks (OCINs) research has shown that the design of buffers in the router significantly influences the power, area overhead and overall performance of the network. In this paper, we propose a low-power, low-area OCIN architecture by reducing the number of buffers within the router. To minimize the performance degradation due to the reduced buffer size, we use the existing repeaters along the inter-router channels to double as buffers when required. At low network loads, the proposed adaptive channel buffers function as conventional repeaters propagating the signals. At high network loads, the adaptive channel buffers function as storage elements in addition to the router buffers. We evaluate the proposed adaptive channel buffers with both static and dynamic buffer allocation policies in the 90nm technology node, using 8Ч8 mesh and folded torus network topologies. Simulation results using the SPLASH-2 suite and synthetic traffic show that by reducing the router buffer size our proposed architecture achieves nearly 40% savings in router buffer power, 30% savings in overall network power and 40% savings in area, with only a marginal 1-5% drop in throughput under dynamic buffer allocation and about 10-20% drop in throughput for statically assigned buffers. [J124]

"Design and Implementation of Control Mechanism for Standby Power Reduction"

In other to save energy, several countries recently made laws related to standby power consumption. To success this exertion, we should consider not only power reduction of consumer electronics itself but also efficient automatic control in networked home environment. In this paper, we present a design approach and implementation result of control mechanism for standby power reduction. Proposed mechanism has the host-agent based structure and uses the IEEE 802.15.4 based ZigBee protocol for communication and security between host and agents. We verified reliability of proposed mechanism and reduction effect of standby power; also, we applied implemented device to scenario which is similar to user living pattern. Experimental results demonstrate that in the proposed mechanism, standby power consumption of Agent which is connected to consumer electronics can be reduced by 203 mW. [J125]

"Test Results for Energy Savings"

This article deals with the impact of different lubrication oils on electric motor energy consumption. Lubrication, and the analysis thereof is becoming a major field in the reliability world. All the samples of oil taken from the bearings machines, finds signs of existing or soon-to-come bearing damage and plan accordingly to reduce harmful downtime. Testing was conducted with the test motor on a motor test standard with seven ISO grade 68 lubrication oils over a two-day period. [J126]

"Adaptive Cluster-Based Data Collection in Sensor Networks with Direct Sink Access"

Recently wireless sensor networks featuring direct sink access have been studied as an efficient architecture to gather and process data for numerous applications. We focus on the joint effect of clustering and data correlation on the performance of such networks. We propose a novel cluster-based data collection scheme for sensor networks with direct sink access (CDC-DSA), and provide an analytical framework to evaluate its performance in terms of energy consumption, latency, and robustness. In our scheme, CHs use a low-overhead and simple medium access control (MAC) conceptually similar to ALOHA to contend for the reachback channel to the data sink. Since in our model data is collected periodically, the packet arrival is not modeled by a continuous random process and, therefore, our framework is based on transient analysis rather than a steady state analysis. Using random geometry tools, we study how the optimal average cluster size and energy savings vary in a response to various data correlation levels under the proposed MAC. Extensive simulations for various protocol parameters show that our analysis is fairly accurate for a wide range of parameters. Our results suggest that despite the tradeoff between energy consumption and latency, both of which can be substantially reduced by proper clustering design. [J127]

"An Efficient Motion-Resistant Method for Wearable Pulse Oximeter"

Reduction of motion artifact and power saving are crucial in designing a wearable pulse oximeter for long-term telemedicine application. In this paper, a novel algorithm, minimum correlation discrete saturation transform (MCDST) has been developed for the estimation of arterial oxygen saturation (SnO2), based on an optical model derived from photon diffusion analysis. The simulation shows that the new algorithm MCDST is more robust under low SNRs than the clinically verified motion-resistant algorithm discrete saturation transform (DST). Further, the experiment with different severity of motions demonstrates that MCDST has a slightly better performance than DST algorithm. Moreover, MCDST is more computationally efficient than DST because the former uses linear algebra instead of the time-consuming adaptive filter used by latter, which indicates that MCDST can reduce the required power consumption and circuit complexity of the implementation. This is vital for wearable devices, where the physical size and long battery life are crucial. [J128]

"Optimization of Global Data Center Thermal Management Workload for Minimal Environmental and Economic Burden"

The rapid deployment of information and communications technology (ICT) across the globe has led to a network of high-density computer data centers to store, process and transmit information. These large-scale technology warehouses consume vast amounts of energy for running the compute infrastructure and auxiliary cooling resources. Recent literature has suggested the possibility of globally staggering compute workloads to take advantage of local climatic conditions as a means to reducing cooling energy costs. This paper further explores this premise by performing an in-depth analysis of the environmental and economic burden of managing the thermal infrastructure of a globally connected data center network. The paper examines a case study where the potential energy savings achievable by staggering workloads across arbitrarily chosen data centers in the U.S., India, and Russia are examined. The results show that the environmental benefit of such off-shoring is mostly dependent on the fuel mix of the grid to which the workload is transferred and the energy consumption in each location. Further, we show that dynamic optimization of the thermal workloads based on local weather patterns can reduce the environmental burden by up to 30%. The paper concludes with a detailed economic assessment. For the case study in this paper, we find that such global workload staggering can potentially reduce operational costs by nearly 35%. [J129]

"Chameleon: Application-Level Power Management"

In this paper, we present Chameleon an application-level power management approach for reducing energy consumption in mobile processors. By using application domain knowledge, as opposed to OS-level or hardware-level inferred knowledge, Chameleon can substantially reduce CPU energy consumption. By exporting the energy management to user-space, designers can design more flexible and easily portable algorithms and systems, and use multiple energy management policies simultaneously. Specifically, we propose a minimal operating system interface that applications use to obtain global knowledge from the kernel in order to make local decisions. We consider three classes of applications soft real-time, interactive and batch and design user level power management strategies for representative applications such as a movie player, a word processor, a web browser, and a batch compiler. Our experiments show that, compared to the traditional system-wide CPU voltage scaling approaches, Chameleon can achieve up to 32-50% energy savings while delivering comparable or better performance to applications. Similarly, Chameleon extracts 9-41% more energy when compared to Grace OS, which uses some application knowledge but operates within the kernel. Further, Chameleon imposes minimal overhead and is effective at scheduling concurrent applications with diverse energy needs. [J130]

"Reducing the Energy Consumption of Ethernet with Adaptive Link Rate (ALR)"

The rapidly increasing energy consumption by computing and communications equipment is a significant economic and environmental problem that needs to be addressed. Ethernet network interface controllers (NICs) in the US alone consume hundreds of millions of US dollars in electricity per year. Most Ethernet links are underutilized and link energy consumption can be reduced by operating at a lower data rate. In this paper, we investigate adaptive link rate (ALR) as a means of reducing the energy consumption of a typical Ethernet link by adaptively varying the link data rate in response to utilization. Policies to determine when to change the link data rate are studied. Simple policies that use output buffer queue length thresholds and fine-grain utilization monitoring are shown to be effective. A Markov model of a state-dependent service rate queue with rate transitions only at service completion is used to evaluate the performance of ALR with respect to the mean packet delay, the time spent in an energy-saving low link data rate, and the oscillation of link data rates. Simulation experiments using actual and synthetic traffic traces show that an Ethernet link with ALR can operate at a lower data rate for over 80 percent of the time, yielding significant energy savings with only a very small increase in packet delay. [J131]

"Picture-Based Address Power Saving Method for High Resolution Plasma Display Panel (PDP)"

A picture-based high-speed address recovery technique for AC (adaptive control) plasma display panels (PDPs) is proposed. By removing the ground (GND) switching operation, the recovery speed can be increased and the switching loss due to the GND switch is reduced. The proposed method can perform load-adaptive operations by controlling the voltage level of the energy recovery capacitor, which prevents the increase of inefficient power consumption caused by circuit loss during the recovery operation. Thus, the technique shows the minimum address power consumption according to various displayed images, which is different from previous methods operating in fixed mode regardless of images. Test results with a 50-in HD single-scan PDP (resolution=1366 times 768) show that a recovery time of less than 350 ns is successfully accomplished and about 54% of the maximum power consumption can be reduced, by tracing the minimum power consumption curves. [J132]

"The Net’s Going Green: Multipronged Approach Might Save Costs, Energy — and the Climate"

This article deals with effort to reduce the Internet's energy usage. The Energy Efficient Internet Project explores the best ways to reduce energy use at the network's edge. The computer industry's most powerful companies are beginning a massive push to make the entire Internet efficient, from the backbone to the BlackBerry. Some of the work, such as the Climate Savers Computing Initiative (www.climatesaverscomputing.org) and the Green Grid (www.thegreen grid.org), are still in their infancy, having been recently formed. However, each is extremely earnest about accomplishing the task of squeezing the most efficiency possible out of its selected piece of the network puzzle. The next step is to define the technical and cultural best practices and communications channels. [J133]

"Wide Pulse Combined With Narrow-Pulse Generator for Food Sterilization"

This paper proposes a wide pulse combined with a narrow-pulse generator for solid-food sterilization. The proposed generator is composed of a full-bridge converter in phase-shift control to generate a high dc-link voltage and a full-bridge inverter associated with an L-C network and a transformer to generate wide pulses combined with narrow pulses. These combined pulses can prevent undesired strong air arcing in free space, reduce power consumption, and save power components, while sterilizing food effectively. The converter and inverter can be operated at high frequencies and with pulse width-modulation control; thus, its weight and size can be reduced significantly, and its efficiency can correspondingly be improved. Experimental results obtained from a prototype with plusmn10-kV wide pulses combined with plusmn10-kV narrow pulses and with 10- to 50-kW peak output power, depending on pulsewidth of the output pulses, have demonstrated its feasibility. [J134]

"Prediction-Based Power-Performance Adaptation of Multithreaded Scientific Codes"

Computing has recently reached an inflection point with the introduction of multi-core processors. On-chip thread-level parallelism is doubling approximately every other year. Concurrency lends itself naturally to allowing a program to trade performance for power savings by regulating the number of active cores, however in several domains users are unwilling to sacrifice performance to save power. We present a prediction model for identifying energy-efficient operating points of concurrency in well-tuned multithreaded scientific applications, and a runtime system which uses live program analysis to optimize applications dynamically. We describe a dynamic, phase-aware performance prediction model that combines multivariate regression techniques with runtime analysis of data collected from hardware event counters to locate optimal operating points of concurrency. Using our model, we develop a prediction-driven, phase-aware runtime optimization scheme that throttles concurrency

so that power consumption can be reduced and performance can be set at the knee of the scalability curve of each program phase. The use of prediction reduces the overhead of searching the optimization space while achieving near-optimal performance and power savings. A thorough evaluation of our approach shows a reduction in power consumption of 10.8% simultaneous with an improvement in performance of 17.9%, resulting in energy savings of 26.7%. [J135]

"A Current-Recycling Technique for Shadow-Match-Line Sensing in Content-Addressable Memories"

A current-recycling technique for shadow-match-line (SML) sensing in content-addressable memories (CAMs) is presented. In order to minimize energy-overhead, a novel current-recycling voltage detector (CRVD) is devised, whose working current is reused to charge up the match-line (ML) to determine matches or mismatches. Furthermore, with this CRVD, the word circuits realize fast-disable of the charging paths in case of mismatches. Since the majority of CAM words are mismatched, a significant power is reduced with a high search speed. Pre-layout simulation results show the proposed 256-word times 144-bit ternary CAM, based on a 0.13-mum 1.2-V CMOS process, achieves 0.51 fJ/bit/search for the word circuit with less than 900-ps search time. The achievement illustrates a 74.2% energy-delay-product (EDP) reduction as compared with the speed-optimized current-saving scheme. Post-layout simulation results of the word circuits show 0.65 fJ/bit/search energy per search with 1.2-ns search time. [J136]

"Error-Resilient Motion Estimation Architecture"

In this paper, we propose an energy-efficient motion estimation architecture. The proposed architecture employs the principle of error-resiliency to combat logic level timing errors that may arise in average-case designs in presence of process variations and/or due to overscaling of the supply voltage [voltage overscaling (VOS)] and thereby achieves power reduction. Error-resiliency is incorporated via algorithmic noise-tolerance (ANT). Referred to as input subsampled replica ANT (ISR-ANT), the proposed technique incorporates an input subsampled replica of the main sum-of-absolute-difference (MSAD) block for detecting and correcting errors in the MSAD block. Simulations show that the proposed technique can save up to 60% power over an optimal error-free system in a 130-nm CMOS technology. These power savings increase to 78% in a 45-nm predictive process technology. Performance of the ISR-ANT architecture in the presence of process variations indicates that average peak signal-to-noise ratio (PSNR) of the ISR-ANT architecture increases by up to 1.8 dB over that of the conventional architecture in 130-nm IBM process technology. Furthermore, the PSNR variation (sigma/mu) is also reduced by 7times over that of the conventional architecture at the slow corner while achieving a power reduction of 33%. [J137]

"An efficient energy saving mechanism for IEEE 802.16e wireless MANs"

This paper presents an energy conservation scheme, maximum unavailability interval (MUI), to improve the energy efficiency for the Power Saving Class of Type II in IEEE 802.16e. By applying the Chinese remainder theorem, the proposed MUI is guaranteed to find the maximum Unavailability Interval, during which the transceiver can be powered down. The proposed MUI only dynamically adjusts one parameter defined in the standard. In addition, it is fully compatible with 802.16e standard. We also propose a new technique to reduce the computational complexity when solving the Chinese remainder theorem problem. Simulation and analysis have been conducted to evaluate the performance. [J138]

"Match Sensing Using Match-Line Stability in Content-Addressable Memories (CAM)"

This paper presents a match-line (ML) sensing scheme that distinguishes a match from a miss by first shunting every ML with a fixed negative resistance, then exciting the MLs with an initial charge, and subsequently observing their voltage developments. It is shown that the voltage on the matched ML will grow to VDDas in an unstable system, whereas the voltage on a missed ML will decay to zero, as in a stable system. Since the initial excitation charge on the ML's can be as low as the noise level in the system, this scheme can approach the minimum possible energy consumption level for match-line sensing. We have implemented, in 0.18 mum CMOS, a 144 times 144 ternary CAM array that includes the stability-based sensing scheme along with two previously-reported sensing schemes. The measured results confirm the power savings of the proposed sensing scheme. In addition, the CAM includes a pipelined search-line (SL) architecture that can reduce the SL portion of CAM power by up to 50%. [J139]

"General Methodology for Soft-Error-Aware Power Optimization Using Gate Sizing"

Power consumption has emerged as the premier and most constraining aspect in modern microprocessor and application-specific designs. Gate sizing has been shown to be one of the most effective methods for power

(and area) reduction in CMOS digital circuits. Recently, as the feature size of logic gates (and transistors) is becoming smaller and smaller, the effect of soft-error rates caused by single-event upsets (SEUs) is becoming exponentially greater. As a consequence of technology feature size reduction, the SEU rate for typical microprocessor logic at sea level will go from one in hundred years to one every minute. Unfortunately, the gate sizing requirements of power reduction and resiliency against SEU can be contradictory. 1) We consider the effects of gate sizing on SEU and incorporate the relationship between power reduction and SEU resiliency to develop a new method for power optimization under SEU constraints. 2) Although a nonlinear programming approach is a more obvious solution, we propose a convex programming formulation that can be solved efficiently. 3) Many of the optimal existing techniques for gate sizing deal with an exponential number of paths in the circuit. We prove that it is sufficient to consider a linear number of constraints. 4) We generalize our methodology to include nonlinear delay models and leakage power as well. As an important preprocessing step, we apply statistical modeling and validation techniques to quantify the impact of fault masking on the SEU rate. Furthermore, we adapt our method to incorporate process variation and evaluate our gate sizing technique under uncertainty. We evaluate the effectiveness of our methodology on ISCAS benchmarks and show that error rates can be reduced by a factor of 100%-200% while, on average, the power reduction is simultaneously decreased by less than 6%-10%, respectively, compared to the optimal power saving with no error rate constraints. [J140]

"Scheduled power-saving mechanism to minimize energy consumption in IEEE 802.16e systems"

A mobile station in IEEE 802.16e operates power management using sleep-mode operation with one or more connections supporting several applications. After all of the connections of an MS transit into the sleep state, the MS powers down and then goes into an unavailable state without communicating with the serving base station. To improve energy conservation, this letter proposes a new scheduled power-saving mechanism, which schedules sleep-mode operations for connections, which newly initiate sleep-mode, by controlling operating parameters, such as the minimum sleep interval (Tmin) and the maximum sleep interval (Tmax), and the initiation time of sleepmode operations of low quality of service (QoS) connections. Performance results show that the proposed mechanism can reduce the available state of an MS through this scheduling, and thus achieve better energy conservation of the MS than the standard mechanism. [J141]

"IWPAAMS2007-05: Energy Saving By Means Of Multiagent Systems And Fuzzy Systems"

The reduction of the consumed energy in heating systems is one of the most important actions to be taken in order to achieve a global sustainability. To save energy is urgent, which means that the energy losses must be reduced. In Spain it is especially important as the construction rate is almost the half of that in Europe. It's designed a distributed solution by means of a multi-agent system, and a central control unit responsible for minimising the energy consumption. The central control unit (CCU) includes a fuzzy model-for estimating the energy needs- and a fuzzy controller-to set the power rate of each heater-. The CCU is responsible for distributing the available power over the set of heaters. This solution is the preliminary study to be included in a heating system product of a local company. [J142]

"Progressive Accumulative Routing: Fundamental Concepts and Protocol"

This paper considers a multi-hop network in which relay nodes cooperate to minimize the total energy consumed in transmitting a (unicast) packet from a source to a destination. We propose the Progressive Accumulative Routing (PAR) algorithm, which progressively performs relay discovery, relay ordering and relay power allocation in a distributed manner, such that each relay node only needs local information. We assume Destination Energy Accumulation, in which the destination accumulates the energy of multiple received copies of a packet, each of which is too weak to be reliably decoded by itself, while the lower complexity relay nodes use a decode-and-forward approach. We also provide a closed-form analysis of the energy-savings achieved by the PAR when a relay node is added to an already existing DEA route. Simulations verify that the algorithm considerably reduces the total energy consumption, and can be implemented efficiently. [J143]

"Adaptive disk power management for portable media players"

To support the large storage requirements, consumer electronics for video playback are increasingly being equipped with hard disk drives (HDD) that consume a significant amount of energy. A video player may prefetch many frames to give disk an opportunity to go to standby mode, but this may cause playback to be distorted or stopped if timely power mode transitions are not incorporated. We present the design, implementation and evaluation of a data prefetching scheme for energy-aware video data retrieval for portable media players (PMP). We formulate the problem when the prefetching is used for variable-bit-rate (VBR) streams to reduce disk energy consumption and then propose a new energy-aware data retrieval scheme that prefetches video data in a just-in-time way so as to increase the period in which disk stays in standby mode while guaranteeing the real-

time service. We implemented our scheme in the legacy video player called Mplayer that is typically used for Linux-based consumer devices. Experimental results show that it saves energy as much as 51% compared with conventional schemes. [J144]

"Energy-Efficient Digital Predistortion With Lookup Table Training Using Analog Cartesian Feedback"

We demonstrate energy-efficient low-complexity adaptive linearization for wideband handset power amplifiers (PAs). Due to power overhead and complexity, traditional wideband linearization techniques such as adaptive digital predistortion (DPD) thus far have not been used for wideband handset transmitters. Our energy-efficient lookup table training strategy resulted in a training energy of 1.83 nJ/entry for a 5-MHz bandwidth WiMAX orthogonal frequency division multiple access (OFDMA) transmission, which represents more than 40times improvement over state-of-the-art DPD implementations. Our experimental prototype transmitter achieves a maximum of 9.9-dB improvement of adjacent channel leakage power at 5.15-MHz offset with 22.0-dBm channel power in the 5-MHz bandwidth WiMAX-OFDMA transmission. This linearity improvement offers 26.5% savings in PA power consumption by reducing power backoff. [J145]

"Energy Efficient Scheduling of Real-Time Tasks on Multicore Processors"

Multicore processors deliver a higher throughput at lower power consumption than unicore processors. In the near future, they will thus be widely used in mobile real-time systems. There have been many research on energy-efficient scheduling of real-time tasks using DVS. These approaches must be modified for multicore processors, however, since normally all the cores in a chip must run at the same performance level. Thus, blindly adopting existing DVS algorithms that do not consider the restriction will result in a waste of energy. This article suggests Dynamic Repartitioning algorithm based on existing partitioning approaches of multiprocessor systems. The algorithm dynamically balances the task loads of multiple cores to optimize power consumption during execution. We also suggest Dynamic Core Scaling algorithm, which adjusts the number of active cores to reduce leakage power consumption under low load conditions. Simulation results show that Dynamic Repartitioning can produce energy savings of about 8 percent even with the best energy-efficient partitioning algorithm. The results also show that Dynamic Core Scaling can reduce energy consumption by about 26 percent under low load conditions. [J146]

"Backlight power reduction and image contrast enhancement using adaptive dimming for global backlight applications"

The paper presents an adaptive dimming technique to reduce backlight power consumption and enhance image contrast for global backlight applications. The proposed adaptive dimming technique consists of two new algorithms: backlight dimming algorithm and contrast enhancement algorithm. The backlight-dimming algorithm obtains appropriate 0% to 50% backlight power reduction depending on characteristics of the image data. The contrast enhancement algorithm not only reduces the adverse effect of backlight power saving, but also improves 20.75% enhancement of image contrast ratio on the average. Numerous simulation results are used for illustration of the effectiveness and merits of the proposed adaptive dimming technique. Experimental results are conducted to show the performance and usefulness of the proposed technique on a 2.2-inch mobile phone liquid crystal display (LCD) made by thin-film-transistor (TFT) technology. [J147]

"A Simple Algorithm for Data Compression in Wireless Sensor Networks"

Power saving is a critical issue in wireless sensor networks (WSNs) since sensor nodes are powered by batteries which cannot be generally changed or recharged. As radio communication is often the main cause of energy consumption, extension of sensor node lifetime is generally achieved by reducing transmissions/receptions of data, for instance through data compression. Exploiting the natural correlation that exists in data typically collected by WSNs and the principles of entropy compression, in this Letter we propose a simple and efficient data compression algorithm particularly suited to be used on available commercial nodes of a WSN, where energy, memory and computational resources are very limited. Some experimental results and comparisons with, to the best of our knowledge, the only lossless compression algorithm previously proposed in the literature to be embedded in sensor nodes and with two well- known compression algorithms are shown and discussed. [J148]

"A High Bandwidth Power Scalable Sub-Sampling 10-Bit Pipelined ADC With Embedded Sample and Hold"

A pipelined ADC architecture for use in sub-sampled systems which is power scalable in relation to its down

sampled bandwidth is presented. The ADC uses a technique to eliminate the front-end sample hold, thereby reducing power consumption. The technique allows for a power savings of 20% compared to a previous design. A method to improve the settling behavior of rapid power-on opamps is also presented. Measured results in a 1.8 V 0.18 CMOS process verify the removal of the front-end sample and hold does not cause gross MSB errors for input frequencies higher than 267 MHz. With 50 MS/s, for the SNDR is 51.5 dB, and with 4.55 MS/s for the SNDR is 52.2 dB. [J149]

"Injection-Locked Clocking: A Low-Power Clock Distribution Scheme for High-Performance Microprocessors"

We propose injection-locked clocking (ILC) to combat deteriorating clock skew and jitter, and reduce power consumption in high-performance microprocessors. In the new clocking scheme, injection-locked oscillators are used as local clock receivers. Compared to conventional clocking with buffered trees or grids, ILC can achieve better power efficiency, lower jitter, and much simpler skew compensation thanks to its built-in deskewing capability. Unlike other alternatives, ILC is fully compatible with conventional clock distribution networks. In this paper, a quantitative study based on circuit and microarchitectural-level simulations is performed. Alpha21264 is used as the baseline processor, and is scaled to 0.13 m and 3 GHz. Simulations show 20- and 23-ps jitter reduction, 10.1% and 17% power savings in two ILC configurations. A test chip distributing 5-GHz clock is implemented in a standard 0.18- m CMOS technology and achieved excellent jitter performance and a deskew range up to 80 ps. [J150]

"Saving energy using flywheels"

The flywheel system has shown through experimental testing to greatly reduce the fuel consumption and emissions output. In addition, the reduced peak power demand from the diesel engine increases the engine life. Furthermore, because of the energy storage made available by the flywheels, the diesel engine can be reduced in size for greater fuel and emissions savings. Initial field tests with a reduced-size engine have yielded fuel savings of up to 35% and more. As an added measure of reliability, if a single flywheel system were to become inoperable, the crane can continue operating with the remaining flywheel. If desired, this lone flywheel can be configured to perform at elevated power levels for a limited time until the service can be completed. [J151]

"A Nanogripper Employing Aligned Multiwall Carbon Nanotubes"

Nanogripper structures using aligned multiwall carbon nanotubes (MWCNTs) are demonstrated and their electromechanical properties have been studied in this paper. The balance of electrostatic force, together with elastostatic force and van der Waals force determines the driving conditions. A triode structure drastically reduces the bias between two moving parts, which consist of MWCNTs. Low bias also enables low power consumption as well as the reduction of electrical damage to an object. The moving parts can keep the same state without any applied biases after bending and connection. This also enables power saving during driving. The device can be a base structure for various nanorobotic or other nanoelectromechanical devices. [J152]

"Low-Complexity Policies for Energy-Performance Tradeoff in Chip-Multi-Processors"

Chip-multi-processor (CMP) utilize multiple energy-efficient processing elements (PEs) to deliver high performance while reducing energy-consumption. Dynamic frequency-Voltage Scaling (DVS) balances performance and energy consumption by varying PEs' frequency-voltage workpointsto save energy while meeting performance requirements. We consider multi-task CMP applications with unknown workloads, and dynamically set workpoints to minimize . Heuristic policies for serial/parallel task-graphs are investigated. We compare these policies to a theoretical bound and show that they achieve good results with low complexity. In most cases the simplest policy, which usually assigns constant workpoints, is also the most cost-effective one. [J153]

"Fast Algorithm and Architecture Design of Low-Power Integer Motion Estimation for H.264/AVC"

In an H.264/AVC video encoder, integer motion estimation (IME) requires 74.29% computational complexity and 77.49% memory access and becomes the most critical component for low-power applications. According to our analysis, an optimal low-power IME engine should be a parallel hardware architecture supporting fast algorithms and efficient data reuse (DR). In this paper, a hardware-oriented fast algorithm is proposed with the intra-/inter-candidate DR considerations. In addition, based on the systolic array and 2-D adder tree architecture, a ladder-shaped search window data arrangement and an advanced searching flow are proposed to efficiently support inter-candidate DR and reduce latency cycles. According to the implementation results, 97% computational complexity is saved by the proposed fast algorithm. In addition, 77.6% memory bandwidth is further saved with the proposed DR techniques at architecture level. In the ultra-low-power mode, the power consumption is 2.13 mW for real-time encoding CIF 30-fps videos at 13.5-MHz operating frequency [J154]

"Analyzing the Energy-Time Trade-Off in High-Performance Computing Applications"

Although users of high-performance computing are most interested in raw performance both energy and power consumption has become critical concerns. One approach to lowering energy and power is to use high-performance cluster nodes that have several power-performance states so that the energy-time trade-off can be dynamically adjusted. This paper analyzes the energy-time trade-off of a wide range of applications-serial and parallel-on a power-scalable cluster. We use a cluster of frequency and voltage-scalable AMD-64 nodes, each equipped with a power meter. We study the effects of memory and communication bottlenecks via direct measurement of time and energy. We also investigate metrics that can, at runtime, predict when each type of bottleneck occurs. Our results show that, for programs that have a memory or communication bottleneck, a power-scalable cluster can save significant energy with only a small time penalty. Furthermore, we find that, for some programs, it is possible to both consume less energy and execute in less time by increasing the number of nodes while reducing the frequency-voltage setting of each node [J155]

"Novel Memory Reference Reduction Methods for FFT Implementations on DSP Processors"

Memory references in digital signal processors (DSP) are expensive due to their long latencies and high power consumption. Implementing fast Fourier transform (FFT) algorithms on DSP involves many memory references to access butterfly inputs and twiddle factors. Conventional FFT implementations require redundant memory references to load identical twiddle factors for butterflies from different stages in the FFT diagrams. In this paper, we present novel memory reference reduction methods to minimize memory references due to twiddle factors for implementing various different FFT algorithms on DSP. The proposed methods first group the butterflies with identical twiddle factors from different stages in the FFT diagrams and compute them before computing other butterflies with different twiddle factors, and then reduce the number of twiddle factor lookups by taking advantage of the properties of twiddle factors. Consequently, each twiddle factor is loaded only once and the number of memory references due to twiddle factors can be minimized. We have applied the proposed methods to implement radix-2 DIF FFT algorithm on TI TMS320C64x DSP. Experimental results show the proposed methods can achieve average of 76.4% reduction in the number of memory references, 53.5% saving of memory spaces due to twiddle factors, and average of 36.5% reduction in the number of clock cycles to compute radix-2 DIF FFT on DSP comparing to the conventional implementation. Similar performance gain is reported for implementing radix-2 DIT FFT algorithms using the new methods [J156]

"Energy-Efficient Localized Topology Control Algorithms in IEEE 802.15.4-Based Sensor Networks"

Sensor networks have emerged as a promising technology with various applications, where power efficiency is one of the critical requirements. The recent IEEE 802.15.4 standard offers a promising platform for wireless sensor networks. Since each node can act as a coordinator or a device in the IEEE 802.15.4 standard, 802.15.4-based sensor networks have various possible network topologies. To reduce power consumption, in this paper, we try to construct network topologies with a small number of coordinators while still maintaining network connectivity. By reducing the number of coordinators, the average duty cycle is reduced and the battery life is prolonged. Three topology control algorithms are proposed in this paper. Self-pruning (SP) is the simplest one with O(1) running time and provides the shortest path to the sink node. Ordinal pruning (OP) can significantly improve SP in terms of power saving with O(n) running time. Layered pruning (LP) is a trade off between the first two pruning algorithms with O(radicn) running time and has a slightly higher power consumption than OP. Furthermore, all three algorithms are independent of the physical radio propagation characteristics. Extensive simulations have been performed to verify the effectiveness of the proposed topology control schemes [J157]

"Hybrid Power Saving Mechanism for VoIP Services with Silence Suppression in IEEE 802.16e Systems"

Current power saving mechanisms in the IEEE 802.16e standard are not designed to take into account silent periods in VoIP traffic. Therefore, we propose a hybrid power saving mechanism (HPSM) suitable for VoIP services with silence suppression, which basically follows the power saving class (PSC) II during talk-spurt periods, but uses the mechanism of PSC I during silent periods. The analysis and simulation results show that the proposed HPSM reduces energy consumption during silent periods while satisfying constraints on the packet drop probability imposed by VoIP services [J158]

"Gate Level Multiple Supply Voltage Assignment Algorithm for Power Optimization Under Timing Constraint"

We propose a multiple supply voltage scaling algorithm for low power designs. The algorithm combines a greedy approach and an iterative improvement optimization approach. In phase I, it simultaneously scales down as many gates as possible to lower supply voltages. In phase II, a multiple way partitioning algorithm is applied to further refine the supply voltage assignment of gates to reduce the total power consumption. During both phases, the timing correctness of the circuit is maintained. Level converters (LCs) are adjusted correctly according to the local connectivity of the different supply voltage driven gates. Experimental results show that the proposed algorithm can effectively convert the unused slack of gates into power savings. We use two of the ISPD2001 benchmarks and all of the ISCAS89 benchmarks as test cases. The 0.13-mum CMOS TSMC library is used. On average, the proposed algorithm improves the power consumption of the original design by 42.5% with a 10.6% overhead in the number of LCs. Our study shows that the key factor in achieving power saving is including the most comfortable supply voltage in the scaling process. [J159]

"Delay-guaranteed Energy Saving Algorithm for the Delay-sensitive Applications in IEEE 802.16e Systems"

The 802.16e power management helps to increase the lifetime of Mobile Subscriber Stations (MSSs) by reducing their energy consumption, but this reduction results in Medium Access Control (MAC) Service Data Unit (SOU) response delay. Hence, both energy consumption and MAC SDU response delay are important performance metrics; however, they have a trade-off relationship. To guarantee the delay constraints of delay-sensitive applications, operating parameters in sleep-mode operation such as minimum sleep interval, Tmin, and maximum sleep interval, Tmax, should be considered seriously. Especially, large Tmaxresults in high MAC SDU response delay. However, in the IEEE 802.16e standard, this point is not given enough attention. In this paper, we first propose a numerical model to determine Tmaxbased on MAC SDU response delay. Then, we propose a Delay -Guaranteed Energy Saving (DGES) algorithm to minimize energy consumption with a given MAC SDU response delay by finding the optimal Tmaxunder a fixed Tmin. Our proposed numerical model and DGES algorithm are verified by simulation results1. [J160]

"Total Power Minimization for Multiuser Video Communications Over CDMA Networks"

In this work, we consider a CDMA cell with multiple terminals transmitting video signals. We adapt the system parameters to minimize the sum of compression powers and transmitter powers of all users while guaranteeing the received video quality at each terminal. The adjustable parameters at user i include the transmitter power Pt,i, the video coding bit rate Rs,i, and video encoder parameters that control the complexity and hence power consumption of the video coder (referred simply as complexity betai). Instead of determining Pt,idirectly, we first determine the desired signal to interference-noise ratio (SINR) gammai. Based on the optimal gammaiand Rs,i, we then determine P t,i. Our analysis shows that the product of Rs,iand gammaiis an important quantity. Given the complexity betai(i.e., given the compression power) and quality constraint, in order to reduce the transmission power, one should choose Rs,iand gammaito minimize their product. When only the total transmission power is concerned, the optimal operating points can be determined at individual users separately: each user should run the encoder to minimize the product of Rs,iand gammai. When the objective is to minimize the sum of compression and transmission powers of all users, the optimal solution can be found in two steps. The first step searches the optimal Rs,i and gammaithat minimize Rs,itimesgammaifor each video category and each possible betaiwhile satisfying the quality constraint at user i. The second step searches the optimal {betai}i=1,...,Nfor all users jointly, that minimizes the sum of transmission and compression powers of all users. The first step can be completed offline in advance, only the second step needs to be computed in real time--based on channel conditions of the users. Our results indicate that for the same class of video users, the one who is closer to the base station compresses at a lower complexity. Simulation results show that significant power savings are obtained by our adaptive algorithms over nonadaptive approaches, where {Rs,i ,betai,gammai} are fixed regardless the channel conditions [J161]

"A New Coeff-Token Decoding Method With Efficient Memory Access in H.264/AVC Video Coding Standard"

In general, a large amount of memory accesses are required for context-based adaptive variable-length coding decoding in H.264/AVC standard. It is a serious problem for applications such as videophone and digital multimedia broadcasting services because of the considerable power consumption of the memory access function. In order to reduce the memory access, we carefully examined the codewords in variable-length code tables (VLCTs) of the coeff-token and found some distinctive features from the structure of codewords. Based on the features, a new coeff-token decoding method with an efficient memory organization is proposed in this paper. The simulation results show that the proposed algorithm achieves an approximately 95% memory access saving without video-quality degradation, compared with conventional decoding [J162]

"Reducing Data TLB Power via Compiler-Directed Address Generation"

Address translation using the translation lookaside buffer (TLB) consumes as much as 16% of the chip power on some processors because of its high associativity and access frequency. While prior work has looked into optimizing this structure at the circuit and architectural levels, this paper takes a different approach to optimizing its power by reducing the number of data TLB (dTLB) lookups for data references. The main idea is to keep translations in a set of translation registers (TRs) and intelligently use them in software to directly generate the physical addresses without going through the dTLB. The software has to work within the confines of the TRs provided by the hardware and has to maximize the reuse of such translations to be effective. The authors propose strategies and code transformations for achieving this in array-based and pointer-based codes, looking to optimize data accesses. Results with a suite of Spec95 array-based and pointer-based codes show dTLB energy savings of up to 73% and 88%, respectively, compared to directly using the dTLB for all references. Despite the small increase in instructions executed with the mechanisms, the approach can, in fact, provide performance benefits in certain cache-addressing strategies [J163]

"Low-Power Buffer Management for Streaming Data"

In this paper, a method for reducing the power consumption in a pipeline of streaming data is presented. The pipeline is divided into multiple stages and buffer memories are inserted between adjacent stages. By dynamically changing the power state of each stage, the overall power consumption of the pipeline, including the power consumed by each stage and by each buffer, can be reduced. For example, when a buffer is full, the stage immediately before it can be turned off for a certain time period to save power. In this paper, the problem of finding the optimal strategy for managing the power state to minimize average power consumption is studied for a pipeline of data consisting of three stages with two buffers in between. The problem is formulated as an optimal control problem of a hybrid system, namely, a dynamical system with both continuous dynamics and discrete transitions. Several important properties of the optimal solutions are derived. Using these properties, the optimal periodic solutions are obtained analytically for the special case when each stage is allowed to turn on and off at most once during each period. Simulation results using practical data are presented. The results show substantial power savings of the proposed method over heuristic buffering strategies [J164]

"SyncWUF: An Ultra Low-Power MAC Protocol for Wireless Sensor Networks"

In wireless sensor networks, power consumption is one of the key design issues because a large number of sensor nodes are powered by cheap batteries. Switching the RF transceiver, which is one of the biggest power consumers in a sensor node, to low-power sleep mode as much as possible has been proven to be a very efficient way to save power with a factor of tens or even hundreds. So far, several schemes have been proposed to reduce the duty cycle of the RF transceiver by MAC layer scheduling. Among them, the wake-up-frame scheme and the WiseMAC are two very efficient protocols based on the so-called preamble sampling technology. This paper proposes combining these two schemes to obtain a further optimized low-power MAC protocol, called SyncWUF, for low-traffic wireless sensor network. Analytical and simulation results prove that our proposal achieves significant battery lifetime gain in different application cases without negatively affecting other important system parameters such as channel capacity and latency [J165]

"Adaptive energy conserving algorithms for neighbor discovery in opportunistic Bluetooth networks"

In this paper, we introduce and evaluate novel adaptive schemes for neighbor discovery in Bluetooth-enabled ad-hoc networks. In an ad-hoc peer-to-peer setting, neighbor search is a continuous, hence battery draining process. In order to save energy when the device is unlikely to encounter a neighbor, we adaptively choose parameter settings depending on a mobility context to decrease the expected power consumption of Bluetooth-enabled devices. For this purpose, we first determine the mean discovery time and power consumption values for In different Bluetooth parameter settings through a comprehensive exploration of the parameter space by means of simulation validated by experiments on real devices. The fastest average discovery time obtained is 0.2 s, while at an average discovery time of I s the power consumption is just 1.5 times that of the idle mode on our devices. We then introduce two adaptive algorithms for dynamically adjusting the Bluetooth parameters based on past perceived activity in the ad-hoc network. Both adaptive schemes for selecting the discovery mode are based only on locally-available information. We evaluate these algorithms in a node mobility simulation. Our adaptive algorithms reduce energy consumption by 50% and have up to 8% better performance over a static power-con serving scheme [J166]

"Power controlled channel allocation for multiuser multiband UWB systems"

Emerging ultra-wideband (UWB) technology offers a great potential for the design of high-speed short-range

communications. However, in order for a UWB device to coexist with other devices, the transmitted power level of UWB is strictly limited by the FCC spectral mask. Such limitation poses a significant design challenge to any UWB system. An efficient management of the limited power is thus a key feature to fully exploit the advantages of UWB. In this paper, a cross layer multiuser multiband UWB scheme is proposed to obtain the optimal subband and power allocation strategy. Optimization criteria involve minimization of power consumption under the constraints on the packet error rate, the data rate, and the FCC limit. To ensure the system feasibility in variable channel conditions, an algorithm to jointly manage the rate assignment of UWB devices, subband allocation, and power control is proposed. A computationally inexpensive suboptimal approach is also developed to reduce the complexity of the problem, which is found to be NP hard. Simulation results under UWB channel model specified in the IEEE 802.15.3a standard show that the proposed algorithm achieves comparable performances to those of the complex optimal full search approach, and it can save up to 61% of transmit power compared to the current multiband scheme in the standard proposal. Moreover, the proposed algorithm can obtain the feasible solutions adaptively when the initial system is not feasible for the rate requirements of the users [J167]

"Distributed Sequential Bayesian Estimation of a Diffusive Source in Wireless Sensor Networks"

We develop an efficient distributed sequential Bayesian estimation method for applications relating to diffusive sources-localizing a diffusive source, determining its space-time concentration distribution, and predicting its cloud envelope evolution using wireless sensor networks. Potential applications include security, environmental and industrial monitoring, as well as pollution control. We first derive the physical model of the substance dispersion by solving the diffusion equations under different environment scenarios and then integrate the physical model into the distributed processing technologies. We propose a distributed sequential Bayesian estimation method in which the state belief is transmitted in the wireless sensor networks and updated using the measurements from the new sensor node. We propose two belief representation methods: a Gaussian density approximation and a new LPG function (linear combination of polynomial Gaussian density functions) approximation. These approximations are suitable for the distributed processing in wireless sensor networks and are applicable to different sensor network situations. We implement the idea of information-driven sensor collaboration and select the next sensor node according to certain criterions, which provides an optimal subset and an optimal order of incorporating the measurements into our belief update, reduces response time, and saves energy consumption of the sensor network. Numerical examples demonstrate the effectiveness and efficiency of the proposed methods [J168]

"Low-Power Cache Design Using 7T SRAM Cell"

On-chip cache consumes a large percentage of the whole chip area and expected to increase in advanced technologies. Charging/discharging large bit lines capacitance represents a large portion of power consumption during a write operation. We propose a novel write mechanism which depends only on one of the two bit lines to perform a write operation. Therefore, the proposed 7T SRAM cell reduces the activity factor of discharging the bit line pair to perform a write operation. Experimental results using HSPICE simulation shows that the write power saving is at least 49%. Both read delay and static noise margin are maintained after carefully sizing the cell transistors [J169]

"Organizing an optimal cluster-based ad hoc network architecture by the modified Quine-McCluskey algorithm"

An optimal cluster-based ad hoc network architecture that requires the minimum number of cluster maintenance overheads not only reduces the waste of the precious bandwidth but also saves the consumption of the limited battery power. Mathematical analyses show that the cluster maintenance overheads can be minimized by minimizing the number of generated clusters and the variance of the number of cluster members. By using the modified Quine-McCluskey (MQM) algorithm, the number of generated clusters and the variance of the number of cluster members of the generated cluster-based network architecture are minimized. Thus, the number of overheads required to maintain the cluster architecture is minimized and the precious bandwidth and the limited battery power are saved [J170]

"Energy-Efficient MAC-Layer Error Recovery for Mobile Multimedia Applications in 3GPP2 BCMCS"

Combining broadcast and mobile phone technologies, 3GPP2 has introduced the Broadcast and Multicast Services (BCMCS) architecture to deliver multimedia content over cdma2000 1xEV-DO wireless networks. In designing a mobile device to support multimedia broadcast services, it is important to reduce delay and energy consumption, while maintaining a tolerable level of data loss. We analyse the energy consumed by a mobile

device receiving broadcast services, focusing on error recovery using the Reed-Solomon (RS) MAC-layer coding scheme. Our model is based on the energy consumed by each computational component of the RS decoder, which we determined by running the decoding process on a realistic ARM7TDMI testbed with experimentally justified cache sizes, and characterizing the energy consumption accurately with the SNU Energy Explorer. By varying the radio channel conditions, RS coding scheme and other system parameters, we determined energy-efficient cache configurations and operating ranges for each RS encoding scheme, corresponding to given levels of service quality in a video application. We have also found that significant energy can be saved by selecting a size of error control block that is appropriate to the target video quality and the channel conditions at the mobile [J171]

"Leakage Control Through Fine-Grained Placement and Sizing of Sleep Transistors"

Multithreshold CMOS (MTCMOS) technology has become a popular technique for standby power reduction. Sleep transistor insertion in circuits is an effective application of MTCMOS technology for reducing leakage power. In this paper, we present a fine-grained approach where each gate in the circuit is provided with an independent sleep transistor. Key advantages of this approach include better circuit slack utilization and improvements in ground-bounce-related signal integrity (which is a major disadvantage in clustering-based approaches). To this end, we propose an optimal polynomial-time fine-grained sleep transistor sizing algorithm. We also prove the selective sleep transistor placement problem as NP-complete and propose an effective heuristic. Finally, in order to reduce the sleep transistor area penalty, we propose a placement-area-constrained sleep transistor sizing formulation. Our experiments show that, on average, the sleep transistor placement and optimal sizing algorithms gave 50.9% and 46.5% savings in leakage power as compared with the conventional fixed-delay penalty algorithms for 5% and 7% circuit slowdown, respectively. Moreover, the postplacement area penalty was less than 5%, which is comparable to clustering schemes. [J172]

"Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating"

The exponential increase in leakage power due to technology scaling has made power gating an attractive design choice for low-power applications. In this paper, we explore this design style in large combinational circuit blocks and latch-to-latch datapaths and introduce a novel power gating approach to yield an improved power-performance tradeoff. We first present a multiple sleep mode power gating technique where each mode represents a different point in the wake-up overhead versus leakage savings design space. We show that the high wake-up latency and wake-up power penalty of traditional power gating limits its application to large stretches of inactivity. The multiple-mode feature allows a processor to enter power saving modes more frequently, hence, resulting in enhanced leakage savings. We apply the multimode power gating technique to datapaths where the degree of applied power gating becomes progressively stronger (harder) along the datapath. This configuration allows us to further balance wake-up overhead with leakage savings by exploiting the fact that logic circuits deep in the datapath have higher wakeup margin and hence can be strongly gated. Simulations show that multiple sleep mode capability provides an extra 17% reduction in overall leakage compared to traditional single mode gating. The multiple modes can be designed to allow state-retentive modes. The results on benchmarks show that a single state-retentive mode can reduce leakage by 19% while preserving state of the circuit. [J173]

"New Investigation in Energy Regeneration of Hydraulic Elevators"

In the conventional valve-controlled hydraulic elevator, when the cabin moves downwards, the entire potential energy of the cabin is wasted and converted into fluid heat by throttling. Thus, the energy consumption of a traditional hydraulic elevator is much higher than that of the traction elevator. To reduce the energy consumption and power installation requirements, the energy-regenerative hydraulic elevators have been developed since 1997. In this paper, different generations of the design are discussed for energy-regenerative system; in particular, a new generation is focused on in detail. Experimental studies of this new design are carried out to compare the energy consumption of different system designs of hydraulic elevator. Finally, a conclusion is drawn that the new generation of hydraulic elevator can achieve a significant energy-saving performance compared to the traditional elevators. [J174]

"On the New Stopping Criteria of Iterative Turbo Decoding by Using Decoding Threshold"

Although many stopping methods of iterative decoding have been discussed in the literature extensively, many of them only focus on the solvable decoding (information is enough for successful decoding). In this paper, we discuss the limitation of the decoding ability based on the extrinsic information transform (EXIT) chart. Then, we propose a new information measurement by using cross correlation to predict the decoding threshold. Moreover, we propose two early termination (ET) schemes (ET-I and ET-II) based on the predicted decoding threshold.

The iterative decoding can stop in either high-signal-to-noise ratio (SNR) situations where the decoded bits are highly reliable (solvable decoding), or low-SNR situations where the decoder already has no capability to decode (unsolvable decoding). The simulation results show that the reduced iterations due to the ET-I scheme almost will not affect the SNR performance, and the ones due to the ET-II scheme can still satisfy the requirement of the specification. Based on our analysis and simulation results, we can further modify the conventional GENIE chart by considering the decoding threshold. By using our new ET concepts, the previous stopping techniques can also be modified to stop in low-SNR situations. The ET property for the iterative decoding can help reduce the unnecessary iterations, so as to save computational complexity and power consumptions in digital signal processors (DSPs) or application-specific integrated circuits (ASICs) in mobile handsets. [J175]

"Wireless sensor networks with energy harvesting technologies: a game-theoretic approach to optimal energy management"

Energy harvesting technologies are required for autonomous sensor networks for which using a power source from a fixed utility or manual battery recharging is infeasible. An energy harvesting device (e.g., a solar cell) converts different forms of environmental energy into electricity to be supplied to a sensor node. However, since it can produce energy only at a limited rate, energy saving mechanisms play an important role to reduce energy consumption in a sensor node. In this article we present an overview of the different energy harvesting technologies and the energy saving mechanisms for wireless sensor networks. The related research issues on energy efficiency for sensor networks using energy harvesting technology are then discussed. To this end, we present an optimal energy management policy for a solar-powered sensor node that uses a sleep and wakeup strategy for energy conservation. The problem of determining the sleep and wakeup probabilities is formulated as a bargaining game. The Nash equilibrium is used as the solution of this game. [J176]

"Modeling UMTS Power Saving with Bursty Packet Data Traffic"

The universal mobile telecommunications system (UMTS) utilizes the discontinuous reception (DRX) mechanism to reduce the power consumption of mobile stations (MSs). DRX permits an idle MS to power off the radio receiver for a predefined sleep period and then wake up to receive the next paging message. The sleep/wake-up scheduling of each MS is determined by two DRX parameters: the inactivity timer threshold and the DRX cycle. In the literature, analytic and simulation models have been developed to study the DRX performance mainly for Poisson traffic. In this paper, we propose a novel semi-Markov process to model the UMTS DRX with bursty packet data traffic. The analytic results are validated against simulation experiments. We investigate the effects of the two DRX parameters on output measures including the power saving factor and the mean packet waiting time. Our study provides inactivity timer and DRX cycle value selection guidelines for various packet traffic patterns. [J177]

"Quasi-Reduced-State Soft-Output Viterbi Detector for Magnetic Recording Read Channel"

Reduced-state trellis detection with decision feedback is widely used to reduce the energy consumption of trellis detectors, particularly for soft-output trellis detectors that are energy-hungry by nature. However, the decision feedback tends to increase the circuit critical path and, more important, makes it difficult to apply some well-proven high-speed trellis detector design techniques such as bit-level pipelining. This paper presents a method, referred to as quasi-reduced-state trellis detection, to tackle such speed bottlenecks. The basic idea is to simply obviate the use of decision feedback by mapping only the data storage block of the trellis detector onto a reduced-state trellis and keeping the trellis state metric computation on the original full-state trellis. This makes sense because the data storage block tends to dominate the overall energy consumption while the decision feedback is due to the reduced-state trellis metric computation. Therefore, it is intuitive that such quasi-reduced-state detectors may largely maintain the energy saving potentials of reduced-state trellis detection without being subject to decision-feedback-induced speed bottlenecks. We demonstrated the effectiveness of this proposed design method by using soft-output Viterbi algorithm (SOVA) detection for a magnetic recording read channel as a test vehicle. [J178]

"Gradient Boundary Detection for Time Series Snapshot Construction in Sensor Networks"

In many applications of sensor networks, the sink needs to keep track of the history of sensed data of a monitored region for scientific analysis or supporting historical queries. We call these historical data a time series of value distributions or snapshots. Obviously, to build the time series snapshots by requiring all of the sensors to transmit their data to the sink periodically is not energy efficient. In this paper, we introduce the idea of gradient boundary and propose the gradient boundary detection (GBD) algorithm to construct these time series snapshots of a monitored region. In GBD, a monitored region is partitioned into a set of subregions and all sensed data in one subregion are within a predefined value range, namely, the gradient interval. Sensors located

on the boundaries of the subregions are required to transmit the data to the sink and, then, the sink recovers all subregions to construct snapshots of the monitored area. In this process, only the boundary sensors transmit their data and, therefore, energy consumption is greatly reduced. The simulation results show that GBD is able to build snapshots with a comparable accuracy and has up to 40 percent energy savings compared with the existing approaches for large gradient intervals. [J179]

"Memory hierarchy for high-performance and energyaware reconfigurable systems"

Run-time reconfigurable resources present many of the features such as high performance, flexibility and reusability demanded by next generation embedded systems. In addition, many emerging reconfigurable architectures have been optimised for low power. However, carrying out run-time reconfigurations often involves a costly reconfiguration overhead both in execution time and in energy consumption. Only the execution-time overhead was dealt with in the previous work. Here, the approach is significantly extended in order to reduce the reconfiguration energy overhead as well. To this end, a configuration memory hierarchy is proposed, with a shared memory layer consisting of a module optimised for performance combined with a module optimised for energy-efficient accesses. For this hierarchy, the authors have developed a mapping algorithm that decides where to load each configuration in order to achieve significant energy savings without introducing any performance degradation. [J180]

"Scalable Dynamic Instruction Scheduler through Wake-Up Spatial Locality"

In a high-performance superscalar processor, the instruction scheduler often comes with poor scalability and high complexity due to the expensive wake-up operation. From detailed simulation-based analyses, we find that 95 percent of the wake-up distances between two dependent instructions are short, in the range of 16 instructions, and 99 percent are in the range of 31 instructions. We apply this wake-up spatial locality to the design of conventional CAM-based and matrix-based wakeup logic, respectively. By limiting the wake-up coverage to i + 16 instructions, where 0 les i les 15 for 16-entry segments, the proposed wake-up designs confine the wake-up operation to two matrix-based or three CAM-based 16-entry segments no matter how large the issue window size is. The experimental results show that, for an issue window of 128 entries (IW128) or 256 entries (IW256), the proposed CAM-based wake-up locality design saves 65 percent (IW128) and 76 percent (IW256) of the power consumption and reduces 44 percent (IW128) and 78 percent (IW256) in the wake-up latency compared to the conventional CAM-based design with almost no performance loss. For the matrix-based wake-up logic, applying wake-up locality to the design drastically reduces the area cost. Extensive simulation results, including comparisons with previous works, show that the wake-up spatial locality is the key element to achieving scalability for future sophisticated instruction schedulers. [J181]

"Near-Memory Caching for Improved Energy Consumption"

The main memory has become one of the largest contributors to overall energy consumption and offers many opportunities for power/energy reduction. In this paper, we propose a power-aware cached-dynamic-RAM (PA-CDRAM) organization that integrates a moderately sized cache directly into a memory chip. We use this near-memory cache to turn a memory bank off immediately after it is accessed to reduce power consumption. We modify the operation and structure of CDRAM with the goal of reducing energy consumption while retaining the performance advantage for which CDRAM was originally proposed. In this paper, we describe our PA-CDRAM organization and show how to incorporate it into the Rambus memory. We evaluate the approach using a cycle-accurate processor and memory simulator. Our results show that PA-CDRAM achieves up to 84 percent (28 percent on the average) improvement in the energy-delay product and up to 76 percent (19 percent on the average) savings in energy when compared to a time-out power management technique. [J182]

"Resource Allocation and Outage Control for Solar-Powered WLAN Mesh Networks"

In this paper, resource allocation and outage control are considered for solar-powered WLAN mesh networks. Solar-powered nodes are a very cost effective option in WLAN mesh deployments where continuous power sources are not practical. In such nodes, the cost of the solar panel and battery can be a significant fraction of the total and, therefore, reducing AP power consumption is very important. A solar panel/battery configuration methodology is introduced based on a proposed AP power-aware version of IEEE 802.11. Public meteorological data is used to provision each node based on an averaged offered capacity profile. Since a node is configured statistically, it is possible that future loading may result in nonzero outage even when negligible outage is the design target. Control algorithms are introduced which can improve node outage performance by sometimes introducing an access point capacity deficit. Results are presented which show the value of the proposed configuration methodology and show that the control algorithms can prevent outage even at high levels of excess loading. [J183]

"Improved power-saving medium-access protocol for IEEE 802.11e QoS-enabled wireless networks"

The performance of a new pointer-based medium-access control protocol that was designed to significantly improve the energy efficiency of user terminals in quality-of-service-enabled wireless local area networks was analysed. The new protocol, pointer- controlled slot allocation and resynchronisation protocol (PCSARe), is based on the hybrid coordination function-controlled channel access mode of the IEEE 802.11e standard. PCSARe reduces energy consumption by removing the need for power-saving stations to remain awake for channel listening. Discrete event network simulations were performed to compare the performance of PCSARe with the non-automatic power save delivery (APSD) and scheduled-APSD power- saving modes of IEEE 802.11e. The simulation results show a demonstrable improvement in energy efficiency without significant reduction in performance when using PCSARe. For a wireless network consisting of an access point and eight stations in power-saving mode, the energy saving was up to 39% when using PCSARe instead of IEEE 802.11e non-APSD. The results also show that PCSARe offers significantly reduced uplink access delay over IEEE 802.11e non-APSD, while modestly improving the uplink throughput. Furthermore, although both had the same energy consumption, PCSARe gave a 25% reduction in downlink access delay compared with IEEE 802.11e S-APSD. [J184]

"A Novel Charge Recycling Design Scheme Based on Adiabatic Charge Pump"

Power consumption has become a critical design criterion for integrated circuits given the growing importance of portable battery-operated devices. A typical CMOS gate driven by power supply (VDD), draws energy equal to CLVDD2during every cycle of operation. We propose a new approach to recycle the charge with an adiabatic charge pump that moves the slower adiabatic components away from the critical path of logic. The critical path of the system, and hence the delay, do not change. This is achieved by overlapping the adiabatic charge pump delays with the computing path logic delays. Many embedded high performance applications such as digital signal processing (DSP), which exhibit datapath parallelism, are ideal candidates for this scheme. The proposed method has been implemented in DSP computations. SPICE simulations-based results indicate that the proposed scheme reduces energy consumption in these DSP circuits by as much as 18% (on average 9.94%) with no perceptible loss in performance. The area penalty for these energy savings are in the 1%-2% range, The leakage energy reduction in 45-nm BPTM averages 46%. [J185]

"Energy-Aware Clock-Frequency Assignment in Microprocessors and Memory Devices for Dynamic Voltage Scaling"

Dynamic supply-voltage scaling (DVS) can reduce the energy consumption of microprocessors, but most DVS schemes only scale the clock frequency of the microprocessor and ignore the memory system. In this paper, we show how more energy can be saved by changing the clock frequency of the memory as well as that of the microprocessor in a coordinated fashion. The contributions of this paper include: 1) consideration of both the energy and access time of the memory; 2) derivation of a mathematical formulation of a system-wide energy model as a function of the clock frequencies of the microprocessor and memory; 3) derivation of analytic solutions of system-wide energy-optimal clock-frequency pairs for the microprocessor and the memory, and, finally, 4) extension of the frequency-assignment technique to handle discrete voltages and frequencies. Cycle-accurate system-level energy simulation shows that the proposed scheme can save up to 50% more energy than previous DVS schemes. Our approach can also be applied to other synchronous peripheral devices [J186]

"Variations-Aware Low-Power Design and Block Clustering With Voltage Scaling"

We present a new methodology which takes into consideration the effect of within-die (WID) process variations on a low-voltage parallel system. We show that in the presence of process variations one should use a higher supply voltage than would otherwise be predicted to minimize the power consumption of a parallel systems. Previous analyses, which ignored WID process variations, provide a lower nonoptimal supply voltage which can underestimate the energy/operation by 8.2. We also present a novel technique to limit the effect of temperature variations in a parallel system. As temperatures increases, the scheme reduces the power increase by 43% allowing the system to remain at it's optimal supply voltage across different temperatures. To further limit the effect of variations, and allow for a reduced power consumption, we analyzed the effects of clustering. It was shown that providing different voltages to each cluster can provide a further 10% reduction in energy/operation to a low-voltage parallel system, and that the savings by clustering increase as technology scales. [J187]

"PMOS-Only Sleep Switch Dual-Threshold Voltage Domino Logic in Sub-65-nm CMOS Technologies"

A circuit technique is proposed in this paper for simultaneously reducing the subthreshold and gate oxide leakage power consumption in domino logic circuits. Only p-channel sleep transistors and a dual-threshold voltage CMOS technology are utilized to place an idle domino logic circuit into a low leakage state. Sleep transistors are added to the dynamic nodes in order to reduce the subthreshold leakage current by strongly turning off all of the high-threshold voltage transistors. Similarly, the sleep switches added to the output nodes suppress the voltages across the gate insulating layers of the transistors in the fan-out gates, thereby minimizing the gate tunneling current. The proposed circuit technique lowers the total leakage power by up to 77% and 97% as compared to the standard dual-threshold voltage domino logic circuits at the high and low die temperatures, respectively. Similarly, a 22% to 44% reduction in the total leakage power is observed as compared to a previously published sleep switch scheme in a 45-nm CMOS technology. The energy overhead of the circuit technique is low, justifying the activation of the proposed sleep scheme by providing a net savings in total energy consumption during short idle periods. [J188]

"A Single-Pair Serial Link for Mobile Displays With Clock Edge Modulation Scheme"

A low-power, single-channel clock-edge modulated serial link has been fabricated in a standard 0.18-mum CMOS technology. The link core size is 343 times 188 mum2for the transmitter and 173 times 83 mum2for the receiver. The link consumes 3.12 mW when operating at 270 Mb/s with a 1.2-V supply. The proposed link transfers all necessary signals between a graphic processor and a mobile display device over a single pair channel, thereby greatly saving the power and cost of the existing full swing parallel lines. The proposed clock edge modulation (CEM) encoding can keep the channel DC-balanced without an additional bit overhead. Since a clock edge is present for each bit, an external reference clock is not needed and its operating frequency can be varied without the possibility of harmonic locking typically found in a referenceless clock and data recovery circuit. A simple DLL-based CEM decoder is described that recovers the data with low power consumption and high jitter tolerance. An analysis of the jitter tolerance to sinusoidal jitter is included along with measured data. The measurement results show jitter tolerance of 20 UIP-Pwith 1-MHz sinusoidal jitter. The use of a push-pull voltage-mode driver further reduces the power consumption. [J189]

"Compiler-Directed Energy Optimization for Parallel Disk Based Systems"

Disk subsystem is known to be a major contributor to overall power consumption of high-end parallel systems. Past research proposed several architectural-level techniques to reduce disk power by taking advantage of idle periods experienced by disks. Although such techniques have been known to be effective in certain cases, they share a common drawback: they operate in a reactive manner, i.e., they control disk power by observing past disk activity (for example, idle and active periods) and estimating future ones. Consequently, they can miss opportunities for saving power and incur significant performance penalties due to inaccuracies in predicting idle and active times. Motivated by this observation, this paper proposes and evaluates a compiler-driven approach to reducing disk power consumption of array-based scientific applications executing on parallel architectures. The proposed approach exposes disk layout information to the compiler, allowing it to derive the disk access pattern, i.e., the order in which parallel disks are accessed. This paper demonstrates two uses of this information. First, we can implement proactive disk power management, i.e., we can select the most appropriate power-saving strategy and disk-preactivation strategy based on the compiler-predicted future idle and active periods of parallel disks. Second, we can restructure the application code to increase the length of idle disk periods, which leads to better exploitation of available power-saving capabilities. We implemented both these approaches within an optimizing compiler and tested their effectiveness using a set of benchmark codes from the Spec 2000 suite and a disk power simulator. Our results show that the compiler-driven disk power management is very promising. The experimental results also reveal that, although proactive disk power management is very effective, code restructuring for disk power achieves additional energy savings across all the benchmarks tested, and these savings a- re very close to optimal savings that can be obtained through an integer linear programming (ILP)-based scheme. [J190]

"Efficient rate-distortion estimation for H.264/AVC coders"

In video coders, the optimal coding mode decision for each coding block can be achieved by exhaustively calculating the rate-distortion cost, which simultaneously considers the distortion performance and the coding bit consumption of all possible modes. The best mode is chosen from the one with the minimum Lagrange cost. To avoid the expensive computation of Lagrange costs, in this paper, we propose transform-domain bit-rate estimation and distortion measures, based on quantized and inverse quantized integer transform coefficients, for the inter-mode decision in H.264/AVC coders. With the proposed scheme, entropy coding, inverse transform, and pixel-reconstructions are not required in the process. With ignorable degradation in coding performance, simulations demonstrate that the proposed estimation method achieves about 40% reduced computation time of rate-distortion cost for the inter-mode decision and saves about 17% total encoding time while combining with

fast motion estimation and fast mode decision algorithms. [J191]

"New 802.11h mechanisms can reduce power consumption"

The original purpose of the IEEE 802.11h standard was to extend WLAN operation in Europe to the 5 GHz band, where WLAN devices need dynamic frequency selection (DFS) and transmit power control (TPC) to coexist with the band's primary users, i.e. radar and satellite systems. Although 802.11h defines the mechanisms or protocols for DFS and TPC, it does not cover the implementations themselves. With some amendments to the 802.11h standard to address this need, the mechanisms for DFS and TPC can be used for many other applications with the benefits of automatic frequency planning, power consumption reduction, range control, interference reduction, and quality-of-service enhancement. MiSer is presented as a simple application example for saving significant communication energy for 802.11h devices [J192]

"Level C+ data reuse scheme for motion estimation with corresponding coding orders"

The memory bandwidth reduction for motion estimation is important because of the power consumption and limited memory bandwidth in video coding systems. In this paper, we propose a Level C+ scheme which can fully reuse the overlapped searching region in the horizontal direction and partially reuse the overlapped searching region in the vertical direction to save more memory bandwidth compared to the Level C scheme. However, direct implementation of the Level C+ scheme may conflict with some important coding tools and then induces a lower hardware efficiency of video coding systems. Therefore, we propose n-stitched zigzag scan for the Level C+ scheme and discuss two types of 2-stitched zigzag scan for MPEG-4 and H.264 as examples. They can reduce memory bandwidth and solve the conflictions. When the specification is HDTV 720p, where the searching range is [-128,128), the required memory bandwidth is only 54%, and the increase of on-chip memory size is only 12% compared to those of traditional Level C data reuse scheme. [J193]

"Efficient rate control for JPEG-2000"

In this paper, we present two new methods for efficient rate control and entropy coding in lossy image compression using JPEG-2000. These two methods enable significant improvements in computation complexity and power consumption over the traditional JPEG-2000 algorithms. First, we propose a greedy heap-based rate-control algorithm (GHRaC), which achieves efficient postcompression rate control by implementing a greedy marginal analysis method using the heap sort algorithm. Second, we propose an integrated rate-control and entropy-coding (IREC) algorithm that reduces the computation complexity of entropy coding by selectively entropy coding only the image data that is likely to be included in the final bitstream, as opposed to entropy coding all image data. Together, these two methods enable significant savings in computation time and power consumption. For example, the GHRaC method demonstrates 16 Ч speedup for rate control when encoding the Lena color image using a target compression ratio of 128:1, one quality layer, and code blocks of 32 Ч 32 pixels. The IREC method expands upon GHRaC to perform entropy coding in conjunction with rate control. Using an enhanced version of IREC, these two methods jointly achieve a speedup in execution time of 14 Ч over traditional rate control and entropy coding, which first entropy codes all image coefficients and then separately performs postcompression rate control using the generalized Lagrange multiplier method to select which data are included in the final bitstream. Both theoretical analysis and empirical results are presented in validating the advantages of the proposed methods. [J194]

"Program counter-based prediction techniques for dynamic power management"

Reducing energy consumption has become one of the major challenges in designing future computing systems. This paper proposes a novel idea of using program counters to predict I/O activities in the operating system. It presents a complete design of program-counter access predictor (PCAP) that dynamically learns the access patterns of applications and predicts when an I/O device can be shut down to save energy. PCAP uses path-based correlation to observe a particular sequence of program counters leading to each idle period and predicts future occurrences of that idle period. PCAP differs from previously proposed shutdown predictors in its ability to: 1) correlate I/O operations to particular behavior of the applications and users, 2) carry prediction information across multiple executions of the applications, and 3) attain higher energy savings while incurring lower mispredictions. We perform an extensive evaluation study of PCAP using a detailed trace-driven simulation and an actual Linux implementation. Our results show that PCAP achieves lower average mispredictions and higher energy savings than the simple timeout scheme and the state-of-the-art learning tree scheme [J195]

"Combined time and information redundancy for SEU-tolerance in energy-efficient real-time systems"

Recently, the tradeoff between energy consumption and fault-tolerance in real-time systems has been

highlighted. These works have focused on dynamic voltage scaling (DVS) to reduce dynamic energy dissipation and on-time redundancy to achieve transient-fault tolerance. While the time redundancy technique exploits the available slack-time to increase the fault-tolerance by performing recovery executions, DVS exploits slack-time to save energy. Therefore, we believe there is a resource conflict between the time-redundancy technique and DVS. The first aim of this paper is to propose the use of information redundancy to solve this problem. We demonstrate through analytical and experimental studies that it is possible to achieve both higher transient fault-tolerance [tolerance to single event upsets (SEUs)] and less energy using a combination of information and time redundancy when compared with using time redundancy alone. The second aim of this paper is to analyze the interplay of transient-fault tolerance (SEU-tolerance) and adaptive body biasing (ABB) used to reduce static leakage energy, which has not been addressed in previous studies. We show that the same technique (i.e., the combination of time and information redundancy) is applicable to ABB-enabled systems and provides more advantages than time redundancy alone. [J196]

"A low-power ROM using single charge-sharing capacitor and hierarchical bit line"

This paper describes a low-power read-only memory (ROM) using a single charge-sharing capacitor (SCSC) and hierarchical bit line (HBL). The SCSC-ROM reduces the power consumption in bit lines. It lowers the swing voltage of bit lines to a minimal voltage by using a charge-sharing technique with a single capacitor. It implements the capacitor with dummy bit lines to improve noise immunity and to make it easier to design. Furthermore, the HBL saves power by reducing the capacitance and leakage current in bit lines. The SCSC-ROM also reduces the power consumption in control unit and predecoder by using the hierarchical word line decoder. The simulation result shows that the SCSC-ROM with 4 КЧ32 bits consumes only 37% power of a conventional ROM. An SCSC-ROM chip is fabricated in a 0.25-μm CMOS process. It consumes 8.2 mW at 240 MHz with 2.5 V. [J197]

"Linear and neural dynamic models: shared benefits between the industrial customer and the ESCo from the energy services' perspective"

In this corrspondence, we investigate the application of linear and neurodynamic models to solve the critical problem of obtaining the most cost-effective electrical load forecast for an industrial site. This is done from the perspective of an energy service company (ESCo). The ESCos' business model is based on the notion of making money by providing a means to enable their commercial customers to lower their electric bills. This in turn is based on the idea that the energy supplier's cost of doing business is reduced if its commercial customers can provide a reliable load forecast. A portion of that cost savings is passed on to the user as a discount in the selling price. Since it is not cost effective for the customer to install extensive monitoring instrumentation, the load forecast must be made on the basis of a model that is determined by applying systems identification techniques to the user's consumption pattern. By a single-point observation of the electrical energy consumption in a dairy plant at quarter-hour intervals over a two-year period, we were able to identify a model and use it to devise a straightforward strategy for nontrivial cost savings to the user and a profitable line of service for the ESCo. The performance of several models is compared. The results for the weekly-based models are reported and the effective cost reduction along with the implementation time to set up the service package are quantified and verified in the proposed final business plan. The project produces overall revenues of roughly euro13 600 over a five-year contracting period [J198]

"Power-efficient access-point selection for indoor location estimation"

An important goal of indoor location estimation systems is to increase the estimation accuracy while reducing the power consumption. In this paper, we present a novel algorithm known as CaDet for power-efficient location estimation by intelligently selecting the number of access points (APs) used for location estimation. We show that by employing machine learning techniques, CaDet is able to use a small subset of the APs in the environment to detect a client's location with high accuracy. CaDet uses a combination of information theory, clustering analysis, and a decision tree algorithm. By collecting data and testing our algorithms in a realistic WLAN environment in the computer science department area of the Hong Kong University of Science and Technology, we show that CaDet (clustering and decision tree-based method) can be much higher in accuracy as compared to other methods. We also show through experiments that, by intelligently selecting APs, we are able to save the power on the client device while achieving the same level of accuracy. [J199]

"An adaptive quorum-based energy conserving protocol for IEEE 802.11 ad hoc networks"

The lifetime of a mobile ad hoc network (MANET) depends on the durability of the mobile hosts' battery resources. In the IEEE 802.11 Power Saving Mode, a host must wake up at every beacon interval, to check if it should remain awake. Such a scheme fails to adjust a host's sleep duration according to its traffic, thereby

reducing its power efficiency. This paper presents new MAC protocols for power saving in a single hop MANET. The essence of these protocols is a quorum-based sleep/wake-up mechanism, which conserves energy by allowing the host to sleep for more than one beacon interval, if few transmissions are involved. The proposed protocols are simple and energy-efficiency. Simulation results showed that our protocols conserved more energy and extended the lifetime of a MANET. [J200]

"Ultra-dynamic Voltage scaling (UDVS) using sub-threshold operation and local Voltage dithering"

Local voltage dithering provides near optimum savings when workload varies for fine-grained blocks. Combining this approach with sub-threshold operation permits ultra-dynamic voltage scaling from 1.1 V to below 300 mV for a 90-nm test chip. Operating at 330 mV provides minimum energy per cycle at 9Ч less energy than ideal shutdown for reduced performance scenarios. Measurements from the test chip characterize the impact of temperature on the minimum energy point. [J201]

"Dynamic resizing of superscalar datapath components for energy efficiency"

The "one-size-fits-all" philosophy used for permanently allocating datapath resources in today's superscalar CPUs to maximize performance across a wide range of applications results in the overcommitment of resources in general. To reduce power dissipation in the datapath, the resource allocations can be dynamically adjusted based on the demands of applications. We propose a mechanism to dynamically, simultaneously, and independently adjust the sizes of the issue queue (IQ), the reorder buffer (ROB), and the load/store queue (LSQ) based on the periodic sampling of their occupancies to achieve significant power savings with minimal impact on performance. Resource upsizing is done more aggressively (compared to downsizing), using the relative rate of blocked dispatches to limit the performance penalty. Our results are validated by the execution of the SPEC 2000 benchmark suite on a substantially modified version of the Simplescalar simulator, where the IQ, the ROB, the LSQ, and the register files are implemented as separate structures, as is the case with most practical implementations. We also use actual VLSI layouts of the datapath components in a 0.18 micron process to accurately measure the energy dissipations for each type of access. For a 4-way superscalar CPU, an average power savings of about 42 percent within the IQ, 74 percent within the ROB (integrating the register file), and 41 percent within the LSQ can be achieved with an average performance penalty of about 5 percent. [J202]

"On the effectiveness of movement prediction to reduce energy consumption in wireless communication"

Node movement can be exploited to reduce the energy consumption of wireless network communication. The strategy consists in delaying communication until a mobile node moves close to its target peer node within an application- imposed deadline. We evaluate the performance of various heuristics that, based on the movement history of the mobile node, estimate an optimal time (in the sense of least energy use) of communication subject to the delay constraint. We evaluate the impact of the node movement model, length of movement history maintained, allowable delay, single hop versus multiple hop communication, and size of data transfer on the energy consumption. We also present measurement results on an iPAQ pocket PC that quantity energy consumption in executing the prediction algorithms. Our results show that, with relatively simple and, hence, efficient prediction heuristics, energy savings in communication can significantly outweigh the energy expenses in executing the prediction algorithms. Moreover, it is possible to achieve robust system performance across diverse node movement models. [J203]

"A unified approach for fault tolerance and dynamic power management in fixed-priority real-time embedded systems"

This paper investigates an integrated approach for achieving fault tolerance and energy savings in real-time embedded systems. Fault tolerance is achieved via checkpointing, and energy is saved using dynamic voltage scaling (DVS). The authors present a feasibility analysis for checkpointing schemes for a constant processor speed as well as for variable processor speeds. DVS is then carried out on the basis of the feasibility analysis. The authors incorporate important practical issues such as faults during checkpointing, rollback recovery time, memory access time, and energy needed for checkpointing, as well as DVS and context switching overhead. Numerical results based on real-life checkpointing data and processor data sheets show that compared to fault-oblivious methods, the proposed approach significantly reduces power consumption and guarantees timely task completion in the presence of faults. [J204]

"Memory access scheduling and binding considering energy minimisation in multi-bank memory systems: integrated approach"

Memory-related activity is one of the major sources of energy consumption in embedded systems. Many types of memories used in embedded systems allow multiple operating modes (e.g. active, standby, nap, power-down) to facilitate energy saving. Furthermore, it has been known that the potential energy saving increases when the embedded systems use multiple memory banks in which their operating modes are controlled independently. The authors propose a compiler-directed integrated approach to the problem of maximally utilising the operating modes of multiple memory banks by solving the three important tasks simultaneously: (1) assignment of variables to memory banks, (2) scheduling of memory access operations and (3) determination of operating modes of banks. Specifically, for an instance of tasks 1 and 2, the authors formulate task 3 as a shortest path (SP) problem in a network and solved it optimally. Then, an SP-based heuristic that solves tasks 2 and 3 efficiently in an integrated fashion is developed. Then the proposed approach is extended to address the limited register constraint in the processor. From experiments with a set of benchmark programs, it is confirmed that the proposed approach is able to reduce the energy consumption by 15.76% over that by the conventional approach. [J205]

"Memory-aware dynamic voltage scaling for multimedia applications"

As the computing environments are continuously moving towards battery-operated mobile and handheld systems, the development of energy-saving mechanisms for such devices has recently become a technical challenge. Dynamic voltage scaling (DVS) has historically been considered an effective method to reduce the processor power consumption. Conventional DVS techniques typically consider only processor utilisation issues in a policy-making process. However, as memory-bound multimedia applications are becoming popular in handheld devices, the DVS policies should consider the so-called 'memory wall' problem to maximise energy gain. Recent DVS techniques suffer from the inefficiency of their policies caused by the memory-wall problem while executing multimedia applications, and no previous research on DVS considers the problem explicitly. The existence of the memory wall problem in a real system is revealed and a metric that can be used to detect the problem in advance is found. A memory-aware DVS (M-DVS) technique that takes the memory wall problem fully into consideration is proposed. The experimental results on a PDA show that M-DVS can reduce 8% of additional power consumption, compared with conventional DVS, without any QoS degradation for handling multimedia clips. [J206]

"A time-based VLSI potentiostat for ion current measurements"

A time-based CMOS integrated potentiostatic control circuit has been designed and fabricated. The design maintains a constant bias potential between the reference and working electrodes for an amperometric chemical sensor. A technique of converting input currents into time for amperometric measurements is proposed. This technique eliminates current amplifying circuitry, reduces matching problems, and increases dynamic range while saving on area and power consumption. Redox currents ranging from 1 pA to 200 nA can be measured with a maximum nonlinearity of ±0.1% over this range. The design can be used to generate cyclic voltammograms for an electrochemical reaction by sweeping the voltages across a range specified by the user. Analog inputs are processed and digital outputs are generated without requiring a power-hungry A/D converter. A prototype chip has been fabricated in the 0.5-µm AMI CMOS process. Experimental results are reported showing the performance of the circuit as a chemical sensor. [J207]

"Dynamic voltage scaling of mixed task sets in priority-driven systems"

This paper describes dynamic voltage scaling (DVS) algorithms for real-time systems with both periodic and aperiodic tasks. Although many DVS algorithms have been developed for real-time systems with periodic tasks, none of them can be used for a system with both periodic and aperiodic tasks because of the arbitrary temporal behaviors of aperiodic tasks. This paper proposes off-line and on-line DVS algorithms that are based on existing DVS algorithms. The proposed algorithms utilize the execution behaviors of scheduling servers for aperiodic tasks. Since there is a tradeoff between the energy consumption and the response time of aperiodic tasks, the proposed algorithms focus on bounding the response time degradation of aperiodic tasks although they delay the response time by stretching the task execution to get high energy savings in mixed task sets. Experimental results show that the proposed algorithms reduce the energy consumption by 48% and 35% over the non-DVS scheme under rate monotonic (RM) scheduling and earliest deadline first (EDF) scheduling, respectively. [J208]

"Distance-based recent use (DRU): an enhancement to instruction cache replacement policies for transition energy reduction"

According to the International Technology Roadmap for Semiconductors (ITRS), the minimum feature size for microprocessors will shrink to 40 nm by 2010. Leakage currents in devices fabricated at these dimensions have been shown to be so dominant that design methodologies driven by power budgets will face challenges in

reducing static power in addition to active power. An effective solution to tackle static power is to transition devices to a low-static-power sleep mode using special circuit-level techniques. However, these transitions come with energy costs, and as these techniques are perfected, and devices transition more often to sleep state, the relative contribution of transition energy to total energy will increase. To deal with the transition overhead, often used techniques are history-based and concentrate only on recognizing when to transition, but do not provide for reducing total transitions without adversely effecting the total sleep time of the devices. In this paper, we study transition-overhead reduction in associative instruction caches. We take advantage of the fact that many programs, particularly those for multimedia applications, spend most of their time in loops and most execution is near-sequential (high spatial locality). We present a technique called DRU (Distance-based Recent Use), which constrains near-sequential fetches to a single bank from the set of associative banks. Evaluation of DRU for different replacement policies in a system-level environment using Mediabench's applications and with various processor architectures (including SPARC and MIPS) have shown energy savings between 20%-28% with negligible hardware and timing overheads. [J209]

"Low leakage techniques for FPGAs"

Reconfigurable architectures are well suited for wireless applications since they provide high performance computation together with the capability to adapt to changing communication protocols. Moving to 90-nm technology and below, FPGAs could suffer from leakage energy consumption due to the large number of inactive transistors. This paper presents an extensive study on the application of different low-leakage techniques to the design of FPGAs. The approaches are compared and mixed to find an implementation of switch blocks and look-up tables which reduces leakage without affecting delay and area. The circuits we propose achieve an 86% stand-by energy saving and 46% active leakage reduction with respect to standard implementations. The FPGA delay is not affected, while area is increased by only 3% [J210]

"Combined Frame Memory Motion Compensation for Video Coding"

The frame memory has long been the dominant component in a video decoder in terms of energy, area, and latency. We proposed a non-combined frame memory motion compensation (CFMMC) for video decoding which facilitates the characteristic of the perfect-matched macroblock (MB) to avoid unnecessary memory access and to save energy. The statistic result confirms that some sequences have more than 70% of MBs being perfect-matched MB. The CFMMC hardware architecture is further evaluated for latency, area, and energy. The hardware architecture shows that with SRAM-base frame memory, the equivalent gate count can be reduced by 37.7%, and the energy consumption and the latency may also be improved for sequences with enough percentage of perfect-matched MBs. Since the benefit of the CFMMC is highly dependent on the percentage of perfect-matched MBs, it is best suited for applications with large portion of static background, such as video surveillance, video telephony, and video conferencing [J211]

"Exploiting Hysteresys in MCML Circuits"

In this brief, hysteresis is introduced to improve the noise margin of positive-feedback source-coupled logic (PFSCL) gates, that are a modification of MOS current-mode logic recently proposed by the same authors. To better understand the effect of hysteresis on the performance and the design of these circuits, a simple analytical model of the noise margin is developed. Extensive simulations on a 0.18-mum CMOS process confirm the adequate accuracy of the model. The noise margin improvement due to the hysteresis is then exploited to reduce the logic swing, which can be beneficial in terms of the speed performance or the power consumption. Practical cases where hysteresis is advantageous are identified, and a comparison with PFSCL gates without hysteresis is carried out. Simulations confirm that, in some well-defined cases, hysteresis can significantly reduce the gate delay under a power constraint, or achieve a power saving under a speed constraint. As a fundamental result, hysteresis turns out to be an interesting design option to improve the power efficiency of PFSCL gates [J212]

"Performance analysis of an improved power-saving medium access protocol for IEEE 802.11 point coordination function WLAN"

Wireless enabled portable devices must operate with the highest possible energy efficiency while still maintaining a minimum level and quality of service to meet the user's expectations. The authors analyse the performance of a new pointer-based medium access control protocol that was designed to significantly improve the energy efficiency of user terminals in wireless local area networks. The new protocol, pointer controlled slot allocation and resynchronisation protocol (PCSAR), is based on the existing IEEE 802.11 point coordination function (PCF) standard. PCSAR reduces energy consumption by removing the need for power saving stations to remain awake and listen to the channel. Using OPNET, simulations were performed under symmetric channel loading

conditions to compare the performance of PCSAR with the infrastructure power saving mode of IEEE 802.11, PCF-PS. The simulation results demonstrate a significant improvement in energy efficiency without significant reduction in performance when using PCSAR. For a wireless network consisting of an access point and 8 stations in power saving mode, the energy saving was up to 31% while using PCSAR instead of PCF-PS, depending upon frame error rate and load. The results also show that PCSAR offers significantly reduced uplink access delay over PCF-PS while modestly improving uplink throughput. [J213]

"Wake-Up Logic Optimizations Through Selective Match and Wakeup Range Limitation"

This paper presents two effective wakeup designs that improve the speed, power, area, and scalability without instructions per cycle (IPC) loss for dynamic instruction schedulers. First, a wakeup design is proposed to aim at reducing the power consumption and wakeup latency. This design removes the read of the destination tags from the wakeup path by matching the source tags directly with the grant lines. Moreover, this design eliminates the redundant matches during the wakeup operations by matching the source tags with only the selected grant lines. Next, the second design explores a metric called wakeup locality to further reduce the area cost of the wakeup logic. By limiting the wakeup ranges for the instructions in the issue window, this design not only reduces the area requirement but also improves the scalability. The experimental results show that this range-limited-wakeup design saves 76%-94% of the power consumption and reduces 29%-77% in the wakeup latency compared to the conventional CAM-based scheme with only 5%-44% of the area cost in a traditional RAM-based scheme. The results also show that this design scales well with the increase of both the issue width and the window size [J214]

"Joint Power Management of Memory and Disk Under Performance Constraints"

This paper presents a method to combine memory resizing and disk shutdown to achieve better energy savings than can be achieved individually. The method periodically adjusts the size of physical memory and the timeout value to shut down a hard disk to reduce the average energy consumption. Pareto distributions are used to model the disk idle time. The parameters of the distributions are estimated at runtime and used to calculate the appropriate timeout value. The memory size is changed based on the predicted number of disk accesses at different memory sizes. The method also considers the delay caused by power management and limits the performance degradation. The method is simulated and compared with other power management methods. Simulation results show that the method consistently achieves better energy savings and less performance degradation across different workloads [J215]

"The power black hole-The cost of power and the security of supply is a growing concern, but many data centre managers are neglecting this important issue."

The cost of power and the security of supply is a growing concern, but many data centre managers are neglecting this important issue. Many fail to take into account the energy consumed by the storage of their ever-expanding base of data. Reducing ongoing power needs with better overall design, planning and data center management should be just as a key concern as disaster recovery and backup plans already are for business. Fortunately, an array of products is available to handle real-world challenges of high power densities and cooling in IT environments. Data center outsourcing is another option that is growing in popularity among businesses. Finally, advances in research into direct current power distribution in the data center are expected to provide more energy savings [J216]

"Energy-Aware Clock-Frequency Assignment in Microprocessors and Memory Devices for Dynamic Voltage Scaling"

Dynamic supply-voltage scaling (DVS) can reduce the energy consumption of microprocessors, but most DVS schemes only scale the clock frequency of the microprocessor and ignore the memory system. In this paper, we show how more energy can be saved by changing the clock frequency of the memory as well as that of the microprocessor in a coordinated fashion. The contributions of this paper include: 1) consideration of both the energy and access time of the memory; 2) derivation of a mathematical formulation of a system-wide energy model as a function of the clock frequencies of the microprocessor and memory; 3) derivation of analytic solutions of system-wide energy-optimal clock-frequency pairs for the microprocessor and the memory, and, finally, 4) extension of the frequency-assignment technique to handle discrete voltages and frequencies. Cycle-accurate system-level energy simulation shows that the proposed scheme can save up to 50% more energy than previous DVS schemes. Our approach can also be applied to other synchronous peripheral devices [J217]

"A Design Technique for Energy Reduction in NORA CMOS Logic"

In this work, a design technique to reduce the energy consumption in NO RAce (NORA) circuits is presented. The technique is based on a unidirectional switch topology combined with a new clocking scheme permitting both charge recycling between circuit nodes and elimination of the short circuit current. Calculations proved that energy savings higher than 20% can be achieved. Simulation results from NORA designs in a 0.18-mum CMOS technology are presented to demonstrate the effectiveness of the proposed technique to achieve both energy and energy-delay product reduction [J218]

"Aviation-Less of a drag-Researchers may only need to look skin-deep to cut aircraft fuel"

As part of the effort to reduce air fuel consumption, researchers are looking at how an aircraft interacts with the air around it as it flies, and the potential savings from managing this interaction using techniques including microelectromechanical systems (MEMS) and plasma jets. Using MEMS devices, researchers were able to selectively roughen the surface of the aircraft to prevent energy-sapping turbulent eddies from forming, thereby reducing skin friction and drag. Another alternative is to use plasma to control a process called separation, which helps force the airflow back over the surface of the wing. Plasma jets can also be used to reduce noise by altering the flow of air around the landing gear to make it less turbulent, which in turn reduces noise [J219]

"Client-Centered, Energy-Efficient Wireless Communication on IEEE 802.11b Networks"

In mobile devices, the wireless network interface card (WNIC) consumes a significant portion of overall system energy. One way to reduce energy consumed by a device is to transition its WNIC to a lower-power steep mode when data is not being received or transmitted. In this paper, we investigate client-centered techniques for energy efficient communication, using IEEE 802.11b, within the network layer. The basic idea is to conserve energy by keeping the WNIC in high-power mode only when necessary. We track each connection, which allows us to determine inactive intervals during which to transition the WNIC to sleep mode. Whenever necessary, we also shape the traffic from the client side to maximize sleep intervals-convincing the server to send data in bursts. This trades lower WNIC energy consumption for an increase in transmission time. Our techniques are compatible with standard TCP and do not rely on any assistance from the server or network infrastructure. Results show that during Web browsing, our client-centered technique saved 21 percent energy compared to PSM and incurred less than a 1 percent increase in transmission time compared to regular TCP. For a large file download, our scheme saved 27 percent energy on average with a transmission time increase of only 20 percent [J220]

"Throttling-Based Resource Management in High Performance Multithreaded Architectures"

Up to now, the power problems which could be caused by the huge amount of hardware resources present in modern systems have not been a primary concern. More recently, however, power consumption has begun limiting the number of resources which can be safely integrated into a single package, lest the heat dissipation exceed physical limits (before actual package meltdown). At the same time, new architectural techniques such as simultaneous multithreading (SMT), whose goal it is to efficiently use the resources of a superscalar machine without introducing excessive additional control overhead, have appeared on the scene. In this paper, we present a new resource management scheme which enables an efficient low power mode in SMT architectures. The proposed scheme is based on a modified pipeline throttling technique which introduces a throttling point at the last stage of the processor pipeline in order to reduce power consumption. We demonstrate that resource utilization plays an important role in efficient power management and that our strategy can significantly improve performance in the power-saving mode. Since the proposed resource management scheme tests the processor condition cycle by cycle, we evaluate its performance by setting a target IPC as one sort of immediate power measure. Our analysis shows that an SMT processor with our dynamic resource management scheme can yield significantly higher overall performance [J221]

"Reducing memory energy consumption of embedded applications that process dynamically allocated data"

The authors present a set of strategies for reducing the energy consumption in a multibank memory architecture using an energy conscious dynamic memory allocation/deallocation. Applications that make dynamic memory allocations are used very frequently in embedded computing and mobile networking areas. The authors' strategies focus on such applications exclusively and cluster dynamically allocated data with a temporal affinity in the physical address space such that the data occupy a small number of memory banks. The remaining banks can be shut off, saving energy. One of the authors' strategies also employs dynamic data migration to further increase energy savings. The experimental results show that all the authors' strategies save a significant amount of energy [J222]

"Multiple-valued logic buses for reducing bus energy in low-power systems"

The viability of bus interconnection models is explored, using the multiple-valued logic (MVL) paradigm to reduce the cost and energy consumption of off-chip and on-chip address, data and instruction buses within system-on-a-chip platforms. Data can be transferred over the buses using ternary, balanced ternary or quaternary number systems, rather than binary. This allows more compact bus design with a fewer number of bus lines, which can result in lower input/output pin cost for off-chip buses. Reducing the number of bus lines also allows us to increase the distance between the adjacent bus lines using the same silicon area. This further reduces interwire capacitance and may lead to significant on-chip bus energy reduction for low-power embedded systems. First, a combinatorial probabilistic view of digit transition patterns in binary and MVL number systems is provided. This is followed by an empirical study conducted by running various applications to measure bus switching activities as well as total bus energy consumption of real-world applications. It is observed that the number of bus transitions in a multiple-valued bus, particularly in a quaternary bus, is significantly less than the number of bus transitions in a binary bus. Our experimental results show that MVL bus models, replacing the binary equivalent, can be viable interconnection structures and are able to provide up to 29, 29 and 30% reduction in energy consumption for off-chip address, data and instruction buses, respectively. These savings are 55, 53 and 62% for on-chip quaternary address, data and instruction buses, respectively using 0.25 μm technology. [J223]

"Embedded power-aware cycle by cycle variable speed processor"

A variable speed processor (VSP) that can adjust its clock period at each cycle, according to the instruction flow in a pipelined program, is presented. This allows performance enhancement and energy consumption reduction, which is an important consideration for the next generation of embedded processor designs. With little change to the standard synchronous design, speed can be enhanced without increasing energy or speed can be maintained with energy savings. The VSP concept is validated by coupling a Nios® processor with a variable period clock synthesiser (VPCS). No modifications to the core other than extracting internal signals from the pipeline are needed to control the VPCS. The VPCS cleanly switches between period lengths at each cycle, over a wide range of possible lengths and with any resolution depending on available clock phases. One VPCS design, in CMOS 0.18 μm, consumes less than 10 μW/MHz and is able to instantly switch inside the 4-250 MHz range. The VSP design is implemented with the Altera® Embedded System platform, in its Stratix® FPGA. With the proposed method, the dynamic energy consumed per program loop is reduced by 14%, while the processing time is reduced by 3.6% compared to the original standard Nios® processor running the same program at its maximum frequency (133 MHz). [J224]

"Control of Rubber Tyred Gantry Crane With Energy Storage Based on Supercapacitor Bank"

This paper proposes a hybrid energy system, which consists of a diesel-engine generator and a supercapacitor, for improving performance of a rubber tyred gantry crane (RTGC). The supercapacitor contributes to the energy recovery associated with regenerative braking in "Hoist-Down" braking operation and to the rapid energy consumption related with acceleration in "Hoist-Up" operation of the RTGC. Hence, it does save energy which is conventionally wasted by a braking resistor. Moreover, the large engine generator is replaced by the much smaller one, because the supercapacitor reduces high power demands away from it. For the power conversion between the supercapacitor and the dc link, a three-leg bidirectional dc-dc converter, which has the same structure as the commercially available three-phase inverter, is used. Two kinds of simulations are performed to study the behaviors of the proposed system under the worst operating conditions. The performance of the proposed hybrid energy system is evaluated through several experiments with a real RTGC. The proposed system can cut down the fuel consumption by 35% and the emission of engine by more than 40% [J225]

"An Efficient Pre-Traceback Architecture for the Viterbi Decoder Targeting Wireless Communication Applications"

A large portion of silicon area and the energy consumed by the Viterbi decoder (VD) is dedicated to the survivor memory and the access operations associated with it. In this work, an efficient pre-traceback architecture for the survivor-path memory unit (SMU) of high constraint length VD targeting wireless communication applications is proposed. Compared to the conventional traceback approach which is based on three kinds of memory access operations: decision bits write, traceback read, and decode read, the proposed architecture exploits the inherent parallelism between the decision bit write and decode traceback operation by introducing pre-traceback operation. Consequently, the proposed pre-traceback approach reduces the survivor memory read operations by 50%. As a result of the reduction of the memory access operations, compared to the conventional 2-pointer traceback algorithm, the size of the survivor memory as well as the decoding latency is reduced by as much as 25%. Implementation results show that the pre-traceback architecture achieves up to 11.9% energy efficiency and 21.3% area saving compared to the conventional traceback architecture for typical wireless applications

[J226]

"Leakage Power Characteristics of Dynamic Circuits in Nanometer CMOS Technologies"

Temperature-dependent subthreshold and gate-oxide leakage power characteristics of domino logic circuits under the influence of process parameter variations are evaluated in this paper. Preferred input vectors and node voltage states that minimize the total leakage power consumption are identified at the lower and upper extremes of a typical die temperature spectrum. New low-leakage circuit design guidelines are presented based on the results. Significantly increased gate dielectric tunneling current, as described in this paper, dramatically changes the leakage power characteristics of dynamic circuits in deeply scaled nanometer CMOS technologies. Contrary to the previously published techniques, a charged dynamic-node voltage state with low inputs is preferred for reducing the total leakage power consumption in the most widely used types of single- and dual-threshold voltage domino gates, particularly at low die temperatures. Furthermore, leakage power savings provided by the dual-threshold voltage domino logic circuit techniques based on input gating are all together reduced due to the significance of gate dielectric tunneling in sub-45-nm CMOS technologies [J227]

"An address-light, integrated MAC and routing protocol for wireless sensor networks"

We propose an address-light, integrated MAC and routing protocol (abbreviated AIMRP) for wireless sensor networks (WSNs). Due to the broad spectrum of WSN applications, there is a need for protocol solutions optimized for specific application classes. AIMRP is proposed for WSNs deployed for detecting rare events which require prompt detection and response. AIMRP organizes the network into concentric tiers around the sink(s), and routes event reports by forwarding them from one tier to another, in the direction of (one of) the sink(s). AIMRP is address-light in that it does not employ unique per-node addressing, and integrated since the MAC control packets are also responsible for finding the next-hop node to relay the data, via an anycast query. For reducing the energy expenditure due to idle-listening, AIMRP provides a power-saving algorithm which requires absolutely no synchronization or information exchange. We evaluate AIMRP through analysis and simulations, and compare it with another MAC protocol proposed for WSNs, S-MAC. AIMRP outperforms S-MAC for event-detection applications, in terms of total average power consumption, while satisfying identical sensor-to-sink latency constraints [J228]

"On the complexity reduction of turbo decoding for wideband CDMA"

Two simple but effective methods for reducing the average complexity (and power consumption) of the conventional turbo-cyclic-redundancy-check decoding scheme with negligible performance degradation in a wideband direct-sequence code-division multiple-access (W-CDMA) environment are introduced. When applied to a W-CDMA turbo code with frame length 640 b at a bit-error rate (BER) of 10-6, the resultant modified schemes can save up to 73% of the average decoding complexity, relative to the conventional scheme. In general, the proposed schemes are more attractive for short-frame and low-BER applications. [J229]

"Optimizing array-intensive applications for on-chip multiprocessors"

With energy consumption becoming one of the first-class optimization parameters in computer system design, compilation techniques that consider performance and energy simultaneously are expected to play a central role. In particular, compiling a given application code under performance and energy constraints is becoming an important problem. In this paper, we focus on an on-chip multiprocessor architecture and present a set of code optimization strategies. We first evaluate an adaptive loop parallelization strategy (i.e., a strategy that allows each loop nest to execute using a different number of processors if doing so is beneficial) and measure the potential energy savings when unused processors during execution of a nested loop are shut down (i.e., placed into a power-down or sleep state). Our results show that shutting down unused processors can lead to as much as 67 percent energy savings at the expense of up to 17 percent performance loss in a set of array-intensive applications. To eliminate this performance penalty, we also discuss and evaluate a processor preactivation strategy based on compile-time analysis of nested loops. Based on our experiments, we conclude that an adaptive loop parallelization strategy combined with idle processor shut down and preactivation can be very effective in reducing energy consumption without increasing execution time. We then generalize our strategy and present an application parallelization strategy based on integer linear programming (ILP). Given an array-intensive application, our optimization strategy determines the number of processors to be used in executing each loop nest based on the objective function and additional compilation constraints provided by the user/programmer. Our initial experience with this constraint-based optimization strategy shows that it is very successful in optimizing array-intensive applications on on-chip multiprocessors under multiple energy and performance constraints. [J230]

"Power-aware storage cache management"

Reducing energy consumption is an important issue for data centers. Among the various components of a data center, storage is one of the biggest energy consumers. Previous studies have shown that the average idle period for a server disk in a data center is very small compared to the time taken to spin down and spin up. This significantly limits the effectiveness of disk power management schemes. This article proposes several power-aware storage cache management algorithms that provide more opportunities for the underlying disk power management schemes to save energy. More specifically, we present an offline energy-optimal cache replacement algorithm using dynamic programming, which minimizes the disk energy consumption. We also present an offline power-aware greedy algorithm that is more energy-efficient than Belady's offline algorithm (which minimizes cache misses only). We also propose two online power-aware algorithms, PA-LRU and PB-LRU. Simulation results with both a real system and synthetic workloads show that, compared to LRU, our online algorithms can save up to 22 percent more disk energy and provide up to 64 percent better average response time. We have also investigated the effects of four storage cache write policies on disk energy consumption. [J231]

"Combined circuit and architectural level variable supply-voltage scaling for low power"

Energy-efficient processor design is becoming more and more important with technology scaling and with high performance requirements. Supply-voltage scaling is an efficient way to reduce energy by lowering the operating voltage and the clock frequency of processor simultaneously. We propose a variable supply-voltage (VSV) scaling technique based on the following key observation: upon an L2 miss, the pipeline performs some independent computations but almost always ends up stalling and waiting for data, despite out-of-order issue and other latency-hiding techniques. Therefore, during an L2 miss we scale down the supply voltage of certain sections of the processor in order to reduce power dissipation while it carries on the independent computations at a lower speed. However, operating at a lower speed may degrade performance, if there are sufficient independent computations to overlap with the L2 miss. Similarly, returning to high speed may degrade power savings, if there are multiple outstanding misses and insufficient independent computations to overlap with them. To avoid these problems, we introduce two state machines that track parallelism on-the-fly, and we scale the supply voltage depending on the level of parallelism. We also consider circuit-level complexity concerns which limit VSV to two supply voltages, stability and signal-propagation speed issues which limit how fast VSV may transition between the voltages, and energy overhead factors which disallow supply-voltage scaling of large RAM structures such as caches and register file. Our simulations show that VSV achieves an average of 7.7% total processor power reduction with 0.9% performance degradation in an eight-way, out-of-order-issue processor that implements deterministic clock gating and software prefetching, across all the SPEC2K benchmarks. For those benchmarks that have high L2 miss rates (more than 4 misses per 1000 instructions), VSV achieves 23.0% reduction in total processor power with 2.0% performance degradation on average. [J232]

"A low-power SRAM using hierarchical bit line and local sense amplifiers"

This paper proposes a low power SRAM using hierarchical bit line and local sense amplifiers (HBLSA-SRAM). It reduces both capacitance and write swing voltage of bit lines by using the hierarchical bit line composed of a bit line and sub-bit lines with local sense amplifiers. The HBLSA-SRAM reduces the write power consumption in bit lines without noise margin degradation by applying a low swing signal to the high capacitive bit line and by applying a full swing signal to the low capacitive sub-bit line. The HBLSA-SRAM reduces the swing voltage of bit lines to VDD/10 for both read and write. It saves 34% of the write power compared to the conventional SRAM. An SRAM chip with 8 КЧ32 bits is fabricated in a 0.25-μm CMOS process. It consumes 26 mW read power and 28 mW write power at 200 MHz with 2.5 V. [J233]

"Query processing in a mobile computing environment: exploiting the features of asymmetry"

With the cutting edge technology advance in wireless and mobile computers, the query processing in a mobile environment involves join processing among different sites, which include static servers and mobile computers. Because of the need for energy saving and also the presence of asymmetric features in a mobile computing environment, the conventional query processing for a distributed database cannot be directly applied to a mobile computing system. In this paper, we first explore three asymmetric features of a mobile environment. Then, in light of these features, we devise query processing methods for both join and query processing. Intuitively, employing semijoin operations in a mobile computing environment is able to further reduce both the amount of data transmission and energy consumption. A semijoin which is initiated by a mobile computer (respectively, the server) and is beneficial to reduce the cost of a join operation is termed a mobile-initiated or MI (respectively, server-initiated or SI) profitable semijoin. According to those asymmetric features of a mobile computing system, we examine three different join methods and devise some specific criteria to identify MI/SI profitable semijoins. For query processing, which refers to the processing of multijoin queries, we develop three query processing

schemes. In particular, we formulate the query processing in a mobile computing system as a two-phase query processing procedure that can determine a join sequence and interleave that join sequence with SI profitable semijoins to reduce both the amount of data transmission and energy consumption. Performance of these join and query methods is comparatively analyzed and sensitivity analysis on several parameters: is conducted. Furthermore, we develop a systematic procedure to derive the characteristic functions of MI and SI profitable semijoins. It is noted that, given some system parameters, those characteristic functions are very important in determining which join method is the most appropriate one to employ in that configuration. It is shown by our simulation results that, by exploiting the three asymmetric features, these characteristic functions are very powerful in reducing both the amounts of energy consumption and data transmission incurred and can- lead to the design of an efficient and effective query processing procedure for a mobile computing environment. [J234]

"Design techniques for single-low-VDD CMOS systems"

In this paper, a new CMOS design scheme called the single-low-VDDCMOS (SLVCMOS) is proposed. With this scheme, a CMOS design implemented in a multi-VTHCMOS technology can be operated with a very low external supply voltage, say 0.5-V, with a sleep current at the level of only picoampere per gate. The key items for a single-chip SLVCMOS design include a sleepless mixed-VTHflip-flop, a boosted sleeping clock signal, and three low-power hard blocks. Analysis shows that additional benefits of using the SLVCMOS include higher performance and lower power consumption in the active mode, smaller leakage current in the sleep mode, shorter wake-up time and reduced wake-up energy during the sleep-to-active transition, and a reduced number of sleep-control signals, saving precious routing resources and reducing the chip area. A dual-rail SLVCMOS cell library and two test chips, one 32-b RISC core and the other verifying the design of hard blocks, are designed and implemented to show the feasibility of the proposed design scheme and the design techniques. [J235]

"Cosynthesis of energy-efficient multimode embedded systems with consideration of mode-execution probabilities"

We present a novel co-design methodology for the synthesis of energy-efficient embedded systems. In particular, we concentrate on distributed embedded systems that accommodate several different applications within a single device, i.e., multimode embedded systems. Based on the key observation that operational modes are executed with different probabilities, that is, the system spends uneven amounts of time in the different modes, we develop a new co-design technique that exploits this property to significantly reduce energy dissipation. Energy and cost savings are achieved through a suitable synthesis process that yields better hardware-resource-sharing opportunities. We conduct several experiments, including a realistic smart phone example, that demonstrate the effectiveness of our approach. Reductions in power consumption of up to 64% are reported. [J236]

"Pipelined array-based FIR filter folding"

The elaborate design of folded finite-impulse response (FIR) filters based on pipelined multiplier arrays is presented in this paper. The design is considered at the bit-level and the internal delays of the pipelined multiplier array are fully exploited in order to reduce hardware complexity. Both direct and transposed FIR filter forms are considered. The carry-save and the carry-propagate multiplier arrays are studied for the filter implementations. Partially folded architectures are also proposed which are implemented by cascading a number of folded FIR filters. The proposed schemes are compared as to the aspect of hardware complexity with a straightforward implementation of a folded FIR filter based on the pipelined Wallace Tree multiplier. The comparison reveals that the proposed schemes require 20%-30% less hardware. Finally, efficient implementation of partially folded FIR filter circuits is presented when constraints in area, power consumption and clock frequency are given. [J237]

"Execution cache-based microarchitecture for power-efficient superscalar processors"

This paper investigates a possible solution to the problem of power consumption in superscalar, out-of-order processors by proposing a new microarchitecture, specifically designed to reduce increasing power requirements of high-end processors. More precisely, we show that by modifying the well-established superscalar processor architecture, significant savings can be achieved in terms of power consumption. Our approach aims at limiting the growing amount of power used in a typical processor for dynamic optimizations (including out-of-order scheduling and register renaming). Our proposed approach achieves significant power savings by reusing as much as possible from the work done by the front-end of a typical superscalar, out-of-order pipeline, via the use of a special cache nested deeply into the processor structure. By reusing instructions that are already decoded, reordered, and have their registers already renamed, the front end of the pipeline can be turned off for large

periods of time with significant savings in the overall power consumption. Experimental results show up to 35% (30% on average) savings in average energy per committed instruction, and 35% (20% on average) savings in energy-delay product, with about 9% average performance loss, over a large spectrum of SPEC95 and SPEC2000 benchmarks. [J238]

"Contact-extended zone-based transactions routing for energy-constrained wireless ad hoc networks"

In future wireless ad hoc networks, transactions are expected to become one of the primary types of flows. Transactions require only a small number of packets to complete. Hence, providing optimal (shortest path) routes to such transactions consumes more energy than the actual data transfer. Conventional shortest path routing protocols are, thus, unsuitable for routing transactions. In this paper, we present a novel architecture, called TRANSFER, for transactions routing in large-scale wireless ad hoc networks. In our approach, we aim to reduce the total energy consumption by transactions as opposed to finding shortest path routes. Our architecture uses a hybrid approach, in which each mobile node obtains information about nodes in its proximity (zone), up to R hops away, using a proactive link-state protocol. Beyond the proximity, we introduce the novel notion of contacts that act as shortcuts to reduce the degrees of separation between the source of the transaction and the destination. We propose an efficient on-demand protocol for contact selection that does not assume knowledge of location information. Contacts are used during transactions and queries to discover valid routes in an energy-efficient manner. Extensive simulations are used to evaluate the performance of our protocol in terms of energy consumption and success rate. We compare our architecture to flooding, dynamic source routing (DSR), zone-routing protocol (ZRP), and two power-aware schemes. Our results show substantial power savings for our contact-based protocol, especially for large ad hoc networks. [J239]

"A 2K/8K mode small-area FFT processor for OFDM demodulation of DVB-T receivers"

We present a novel implementation for 2K/8K dual-mode FFT (fast Fourier transform) for OFDM (orthogonal frequency division multiplexing) of DVB-T (digital video broadcasting terrestrial) receivers. Besides pipelining the FFT to reduce the area and enhance the data throughput, SDF (single-path delay feedback) butterfly units for radix-2 and radix-4 processing are adopted to resolve the power consumption difficulty and the P&R (place and route) problem. The SRAM is used in the butterfly units to relax the auto-refreshing requirement if DRAM is used such that not only is the dynamic power saved, the timing control is also less stingy. The 2K/8K FFT comprises 5/6 cascaded stages of radix-4 and one stage of radix-2 butterfly units. The proposed design is carried out by 0.35 μm 2P4M CMOS process to verify the high processing 8 MHz rate with power dissipation as low as 535 mW at a 16 MHz system clock. [J240]

"A centralized energy-efficient routing protocol for wireless sensor networks"

Wireless sensor networks consist of small battery powered devices with limited energy resources. Once deployed, the small sensor nodes are usually inaccessible to the user, and thus replacement of the energy source is not feasible. Hence, energy efficiency is a key design issue that needs to be enhanced in order to improve the life span of the network. Several network layer protocols have been proposed to improve the effective lifetime of a network with a limited energy supply. In this article we propose a centralized routing protocol called base-station controlled dynamic clustering protocol (BCDCP), which distributes the energy dissipation evenly among all sensor nodes to improve network lifetime and average energy savings. The performance of BCDCP is then compared to clustering-based schemes such as low-energy adaptive clustering hierarchy (LEACH), LEACH-centralized (LEACH-C), and power-efficient gathering in sensor information systems (PEGASIS). Simulation results show that BCDCP reduces overall energy consumption and improves network lifetime over its comparatives. [J241]

"Experiences in managing energy with ECOSystem"

Mobile devices are becoming increasingly popular, from laptops, PDAs, and cell phones to emerging platforms such as wireless sensor networks. Available battery energy has become a critical mobile-system resource. A mobile device's usefulness is often limited not by its hardware's raw speed but by its battery's energy. Energy consumption is a major systems-design challenge. We designed our ECOSystem (Energy-Centric Operating System) prototype to manage energy consumption at the OS level, complementing existing power-management techniques, such as DVS and application adaptation. It's based on the ideas that energy management should be a system-wide effort, that we should explicitly recognize energy as a resource, and that we should unify energy management across the system. Even managing one hardware device might require coordination with other system components. Without unified management, application-level energy-saving efforts might not result in reduced energy consumption. ECOSystem incorporates the "currentcy model", which lets the operating system

manage energy as a first-class resource. It can also express complex energy-related goals and behaviors, leading to more effective, unified management policies. [J242]

"On supporting power-efficient streaming applications in wireless environments"

Reducing the power consumption of the wireless network interface (WNI) is an effective way to prolong the battery lifetime of the mobile terminal. It takes some time for the WNI to transit from the power-saving mode to the active mode. This transition delay and the error-prone wireless link bring many challenges for designing power-aware and QoS-aware service models. In this paper, we present a novel power-conserving service model for streaming applications over wireless networks. At the base station side, a new scheduling algorithm, called rate-based bulk scheduling (RBS), is designed to decide which flow should be served at which time. The mobile terminal relies on a proxy to buffer data so that the WNI can sleep for a long time period to save power. To deal with channel errors, a novel adaptive technique is presented to adjust the sleep time of the WNI according to the channel condition. Through analysis, we prove that RBS can provide delay guarantee and it is more power efficient than other rate-based fair queuing algorithms. We use audio-on-demand as a case study to evaluate the performance of RBS. Experimental results show that RBS achieves excellent QoS provision for each flow and significantly reduces the power consumption. [J243]

"Using an operand file to save energy and to decouple commit resources"

The register file of a modern superscalar processor is a critical component of the processor pipeline that can have a large impact on processor performance. Large register files provide larger windows of speculation to the processor and allow greater levels of instruction-level parallelism. However, the access time and energy consumption of these structures can grow quite large when these structures increase in size, especially considering the number of ports required. The paper proposes an architecture that moves the large register file needed to fully exploit greater levels of instruction level parallelism off the schedule to the execute path of the processor. This is accomplished by decoupling the instruction window (the amount of instruction state maintained in the reorder buffer and register file) from the scheduling window (the working set of registers required by the instruction scheduler and execution core). The state of the scheduling window is maintained by an operand file and a speculative logical register file. The operand file stores only the set of input registers to be consumed by instructions in the issue queue, and provides low-latency and energy efficient storage for the working set of registers. This design can reduce the energy dissipation by a factor of 6.5 on average over a traditional large register file, and allows the instruction window to be scaled independently of the register file structures on the schedule to execute path. [J244]

"Level-shifter free design of low power dual supply voltage CMOS circuits using dual threshold voltages"

Usage of dual supply voltages in a digital circuit is an effective way of reducing the dynamic power consumption due to the quadratic relation of supply voltage to dynamic power consumption. But the need for level shifters when a low voltage gate drives a high voltage gate has been a limiting factor preventing widespread usage of dual supply voltages in digital circuit design. The overhead of level shifters forces designers to increase the granularity of dual voltage assignment, reducing the maximum obtainable savings. We propose a method of incorporating voltage level conversion into regular CMOS gates by using a second threshold voltage. Proposed level shifter design makes it possible to apply dual supply voltages at gate level granularity with much less overhead compared to traditional level shifters. We modify the threshold voltage of the high voltage gates that are driven by low voltage gates in order to obtain the level shifting operation together with the logic operation. Using our method, we obtained an average of 20% energy savings for ISCAS'85 benchmark circuits designed using 180-nm technology and 17% when 70-nm technology is used. [J245]

"Energy scalable universal hashing"

Message authentication codes (MACs) are valuable tools for ensuring the integrity of messages. MACs may be built around a universal hash function (NH) which was explored in the construction of UMAC. In this paper, we use a variation on NH called WH. WH reaches optimally in the sense that it is universal with half the hash length of NH and it achieves perfect serialization in hardware implementation. We achieved substantial power savings of up to 59 percent and a speedup of up to 7.4 times over NH. Moreover, we show how the technique of multihashing and the Toeplitz approach can be combined to reduce the power and energy consumption even further while maintaining the same security level with a very slight increase in the amount of the key material. At low frequencies, the power and energy reductions are achieved simultaneously while keeping the hashing time constant. We developed formulae for estimation of the leakage and dynamic power consumptions as well as the energy consumption based on the frequency and the Toeplitz parameter t. We introduce a powerful method for

scaling WH according to specific energy and power consumption requirements. Our implementation of WH-16 consumes only 2.95 μW at 500 kHz. It can therefore be integrated into a self-powered device. [J246]

"Reducing radiation-hardened DigitalCircuit power consumption"

Low-power radiation-hardened sequential digital circuits supporting multiple supply voltages, integrated logic, and a low standby power state are presented. By basing the design on proven radiation hard circuits, single event effects hardness is guaranteed. The circuit is based on differential cascode voltage switch logic, which provides an integral level shift and allows storage at the full supply voltage supported by the process, while allowing the combinatorial logic supply voltage to scale for power savings. When compared to a conventional master-slave flip-flop design, the proposed flip-flop design provides up to 80% energy reduction with logic operating at reduced voltage and speed. Fifty-percent energy reduction is obtained without compromising speed when operating with all circuits at maximum voltage. [J247]

"Digital implementation of a wavelet-based event detector for cardiac pacemakers"

This paper presents a digital hardware implementation of a novel wavelet-based event detector suitable for the next generation of cardiac pacemakers. Significant power savings are achieved by introducing a second operation mode that shuts down 2/3 of the hardware for long time periods when the pacemaker patient is not exposed to noise, while not degrading performance. Due to a 0.13-μm CMOS technology and the low clock frequency of 1 kHz, leakage power becomes the dominating power source. By introducing sleep transistors in the power-supply rails, leakage power of the hardware being shut off is reduced by 97%. Power estimation on RTL-level shows that the overall power consumption is reduced by 67% with a dual operation mode. Under these conditions, the detector is expected to operate in the sub-μW region. Detection performance is evaluated by means of databases containing electrograms to which five types of exogenic and endogenic interferences are added. The results show that reliable detection is obtained at moderate and low signal to noise-ratios (SNRs). Average detection performance in terms of detected events and false alarms for 25-dB SNR is PD=0.98 and PFA=0.014, respectively. [J248]

"An ultra-wideband transceiver architecture for low power, low rate, wireless systems"

This paper presents the system architecture, modeling, and design constraints for a baseband, integrated, CMOS, impulse ultra-wideband transceiver targeting very low power consumption on the order of 1 mW. Intended for a sensor network application, the radio supports low communication rates (100 kpbs) and ranging capabilities over short distances (10 m). Based on a "mostly digital" architecture, the analog complexity is reduced by moving the A/D convertor as close to the antenna as is reasonable. Pulses are generated from simple digital switches, overlaying the signal energy on the lower FCC UWB band (0-960 MHz). Reception is achieved using baseband gain blocks feeding a time-interleaved bank of low resolution A/D converters. A window of energy is captured in time and fed to the digital backend for processing. To save power and area, the digital backend implements only a pulse template correlation filter block overlaid with an additional spreading code. As a pulse template is used, no specific channel estimation or interference cancellation is assumed. The system performance is quantified for this case and implementation tradeoffs are explored with a strong focus on reducing power consumption. In particular, the issues of modulation choice, clock generation, gain and noise figure, ADC resolution, and digital signal processing requirements will be discussed. [J249]

"Quality-adaptive requantization for low-energy MPEG-4 video decoding in mobile devices"

Current mobile devices usually provide streaming media for users. While the online multimedia processing requires intensive computation, the characteristics of mobility and portability place a severe energy constraint on the system. In this paper, we aim to develop a systematic methodology for dealing with low-energy computation for the MPEG-4 video decoding. Our approach is based on a new fine-controllable, quality-adaptive technique to reduce data volumes, which results in energy saving. To do so, we introduce a requantization step to the video decoding process. The proposed requantization ensures that the energy consumption reduces at higher rate than the video quality degrades, and that the videos remain intelligible to a human viewer. The experimental results show that the energy consumption is reduced by up to 42% with 13% quality degradation, thereby confirming the efficacy of the quality-adaptive requantization. [J250]

"A holistic approach to designing energy-efficient cluster interconnects"

Designing energy-efficient clusters has recently become an important concern to make these systems economically attractive for many applications. Since the cluster interconnect is a major part of the system, the focus of this paper is to characterize and optimize the energy consumption in the entire interconnect. Using a cycle-accurate simulator of an InfiniBand Architecture (IBA) compliant interconnect fabric and actual designs of its

components, we investigate the energy behavior on regular and irregular interconnects. The energy profile of the three major components (switches, network interface cards (NICs), and links) reveals that the links and switch buffers consume the major portion of the power budget. Hence, we focus on energy optimization of these two components. To minimize power in the links, first we investigate the dynamic voltage scaling (DVS) algorithm and then propose a novel dynamic link shutdown (DLS) technique. The DLS technique makes use of an appropriate adaptive routing algorithm to shut down the links intelligently. We also present an optimized buffer design for reducing leakage energy in 70nm technology. Our analysis on different networks reveals that, while DVS is an effective energy conservation technique, it incurs significant performance penalty at low to medium workload. Moreover, energy saving with DVS reduces as the buffer leakage current becomes significant with 70nm design. On the other hand, the proposed DLS technique can provide optimized performance-energy behavior (up to 40 percent energy savings with less than 5 percent performance degradation in the best case) for the cluster interconnects. [J251]

"Efficient idle: on the electrification of class-8 trucks"

This article presents the research program, which covers the developments associated with the electrification of class 8 on-highway trucks to reduce parasitic losses. Truck electrification provides a great opportunity for reducing fuel consumption on long-haul class 8 trucks. The dominant fuel savings opportunity is in reducing the amount of time the main engine idles. This creates a significant cost challenge if the fuel efficiency of a truck is to be improved by boosting the efficiency of individual components. Components could be remotely placed, away from challenging or harsh locations, e.g., engine compartments, improving their durability, serviceability and reducing maintenance cost. [J252]

"Design of a power-reduction Viterbi decoder for WLAN applications"

In this paper, a 64-state four-bit soft-decision Viterbi decoder with power saving mechanism for high speed wireless local area network applications is presented. Based on path merging and prediction techniques, a survivor memory unit with hierarchical memory design is proposed to reduce memory access operations. It is found that more than 70% memory access can be reduced by taking advantage of locality. Moreover, a low complexity compare-select-add unit is also presented, leading to save 15% area and 14.3% power dissipation as compared to conventional add-compare-select design. A test chip has been designed and implemented in 0.18-μm standard CMOS process. The test results show that 30 40% power dissipation can be reduced, and the power efficiency reaches 0.75 mW per Mb/s at 6 Mb/s and 1.26 mW per Mb/s at 54 Mb/s as specified in IEEE 802.11a. [J253]

"Modeling and sizing for minimum energy operation in subthreshold circuits"

This paper examines energy minimization for circuits operating in the subthreshold region. Subthreshold operation is emerging as an energy-saving approach to many energy-constrained applications where processor speed is less important. In this paper, we solve equations for total energy to provide an analytical solution for the optimum VDDand VTto minimize energy for a given frequency in subthreshold operation. We show the dependence of the optimum VDDfor a given technology on design characteristics and operating conditions. This paper also examines the effect of sizing on energy consumption for subthreshold circuits. We show that minimum sized devices are theoretically optimal for reducing energy. A fabricated 0.18-μm test chip is used to compare normal sizing and sizing to minimize operational VDDand to verify the energy models. Measurements show that existing standard cell libraries offer a good solution for minimizing energy in subthreshold circuits. [J254]

"Low-Power Small-Area Digital I/O Cell"

A novel low-power and small-area digital I/O cell is proposed in this work. The new input/output (I/O) cell drastically reduces the I/O power consumption, which has been considered as the major power dissipation of the whole chip. The maximum operating clock is 500 MHz given a 10-pF offchip load. On top of the power saving feature, the proposed cell occupies merely$10535.2=4167.45 (transmitter)$$+6367.8 (receiver) muhbox m^2$which is far less than any prior commercially available I/O and low-voltage differential signaling I/O cells. Physical measurements of the proposed I/O cells show that the delays of the transmitter and the receiver are 1.1 and 1.8 ns, respectively. The largest power/bandwidth of the proposed design is 38.9$mu hbox W/MHz$when transmitting. [J255]

"An energy efficient instruction set synthesis framework for low power embedded system designs"

Energy efficiency, performance, area, and cost are critical concerns in designing microprocessors for embedded systems such as portable handheld computing and personal telecommunication devices. This work introduces the

concept of framework-based instruction set synthesis (FITS), which is a new instruction synthesis paradigm that falls between a general-purpose embedded processor and a synthesized application specific processor (ASP). FITS processors reduce code size and energy consumption by tailoring the instruction set to the requirement of a target application. This is achieved by replacing the fixed instruction and register decoding of a general purpose embedded processor with programmable decoders that can achieve ASP performance, low energy consumption, and smaller code size with the fabrication advantages of a mass produced single chip solution. Experimental results show that our synthesized instruction sets result in significant power reduction in the level one instruction cache compared to ARM instructions. The instruction cache is one of the most predominant sources of power dissipation on the processor. For instance, in Intel's StrongARM processor, 27 percent of total chip power loss goes into the instruction cache. For 21 MiBench benchmarks, our simulation results, indicate, on average, a 49.4 percent saving for switching power, a 43.9 percent saving for internal power, a 14.9 percent saving for leakage power, a 46.6 percent saving for total instruction cache power with up to 60.3 percent saving for peak power. [J256]

"Memory energy minimization by data compression: algorithms, architectures and implementation"

Storing data in compressed form is becoming common practice in high-performance systems, where memory bandwidth constitutes a serious bottleneck to program execution speed. In this paper, we suggest hardware-assisted data compression as a tool for reducing energy consumption of processor-based systems. We propose a novel and efficient architecture for on-the-fly data compression and decompression whose field of operation is the cache-to-memory path. Uncompressed cache lines are compressed before they are written back to main memory, and decompressed when cache refills take place. We explore two classes of table-based compression schemes. The first, based on offline data profiling, is particularly suitable to embedded systems, where predictability of the data set is usually higher than in general-purpose systems. The second solution we introduce is adaptive, that is, it takes decisions on whether data words should be compressed according to the data statistics of the program being executed. We describe in details the architecture of the compression/decompression unit and we provide an insight about its implementation as a hardware (HW) block. We present experimental results concerning memory traffic and energy consumption in the cache-to-memory path of a core-based system running standard benchmark programs. The obtained energy savings range from 8%-39% when profile-driven compression is adopted, and from 7%-26% when the adaptive scheme is used. Performance improvements are also achieved as a by-product, showing the practical applicability of the proposed approach. [J257]

"A simplified computational kernel for trellis-based decoding"

A simplified branch metric and add-compare-select (ACS) unit is presented for use in trellis-based decoding architectures. The simplification is based on a complementary property of best feedforward and some systematic feedback encoders. As a result, one adder is saved in every other ACS unit. Furthermore, only half the branch metrics have to be calculated. It is shown that this simplification becomes especially beneficial for rate 1/2 convolutional codes. Consequently, area and power consumption will be reduced in a hardware implementation. [J258]

"Chromatic encoding: a low power encoding technique for digital visual interface"

This paper presents a low-power encoding technique, called chromatic encoding, for the digital visual interface standard (DVI), a digital serial video interface. Chromatic encoding reduces power consumption by minimizing the transition counts on the DVI. This technique relies on the notion of tonal locality, i.e., the observation-first made in this paper-that the signal differences between adjacent pixels in images follow a Gaussian distribution. Based on this observation, an optimal code assignment is performed to minimize the transition counts. Furthermore, the three-color channels of the DVI may be reciprocally encoded to achieve even more power saving. The idea is that given the signal values from the three-color channels, one or two of these channels are encoded by reciprocal differences with a number of redundant bits used to indicate the selection. The channel selection problem is formulated as a minimum spanning tree problem and solved accordingly. The proposed technique requires only three redundant bits for each 24-bit pixel. Experimental results show up to a 75% power reduction in the DVI. [J259]

"A CAM with mixed serial-parallel comparison for use in low energy caches"

A novel, low-energy content addressable memory (CAM) structure is presented which achieves an approximately four-fold improvement in energy per access, compared to a standard parallel CAM, when used as tag storage for caches. It exploits the address patterns commonly found in application programs, where testing the four least significant bits of the tag is sufficient to determine over 90% of the tag mismatches; the proposed CAM checks

those bits first and evaluates the remainder of the tag only if they match. Although, the energy savings come at the cost of a 25% increase in search time, the proposed CAM organization also supports a parallel operating mode without a speed loss but with reduced energy savings. [J260]

"A low-power reduced swing global clocking methodology"

In this brief, we investigate the potential of reduced swing clock networks for low-power applications. We designed and laid out a full swing conventional and a reduced swing H-tree clock distribution network in 0.13-μm CMOS technology operating at 500 MHz. In the reduced swing clock network, the swing was reduced in the global clock distribution network and was restored to the full swing in the local clock distribution domains. The post-layout simulation results of this research shows that a power saving of 22% under nominal operating condition is feasible. [J261]

"Sleep switch dual threshold Voltage domino logic with reduced standby leakage current"

A circuit technique is presented for reducing the subthreshold leakage energy consumption of domino logic circuits. Sleep switch transistors are proposed to place an idle dual threshold voltage domino logic circuit into a low leakage state. The circuit technique enhances the effectiveness of a dual threshold voltage CMOS technology to reduce the subthreshold leakage current by strongly turning off all of the high threshold voltage transistors. The sleep switch circuit technique significantly reduces the subthreshold leakage energy as compared to both standard low-threshold voltage and dual threshold voltage domino logic circuits. A domino adder enters and leaves a low leakage sleep mode within a single clock cycle. The energy overhead of the circuit technique is low, justifying the activation of the proposed sleep scheme by providing a net savings in total power consumption during short idle periods. [J262]

"Pulsed wave interconnect"

Pulsed wave interconnect is proposed for global interconnect applications. Signals are represented by localized wave-packets that propagate along the interconnect lines at the local speed of light to trigger the receivers. Energy consumption is reduced through charging up only part of the interconnect lines and using the voltage doubling property of the receiver gate capacitances. In a 0.18-μm CMOS technology case study, SPICE simulations show that pulsed wave interconnect can save up to 50% of energy and 30% of chip area in comparison with the repeater insertion method. A proposed signal splitting structure provides reasonable isolations between different receivers. Measured S-parameters of 3.8-mm interconnect lines fabricated through CMOS foundry showed that the distortion and attenuation of a pico second signal are much less serious than the theoretical predictions. Pulsed wave interconnect also enables time division application of a single line to boost its bit rate capacity. The use of nonlinear transmission lines (NLTL) is also proposed to overcome pulse broadening and attenuation caused by dispersion and frequency-dependent losses. Pulsed waves on an NLTL may be generated, transmitted, split and detected with components realizable in bulk and SOI CMOS technologies. Tapered NLTL can be used for pulse compression. NLTL edge sharpening abilities may be applicable for signal rise time control. [J263]

"Low-power multiplierless DCT architecture using image correlation"

Low-power design is one of the most important challenges to maximize battery life in portable devices and to save the energy during system operation. In this paper, we propose a low-power DCT (discrete cosine transform) architecture using a modified multiplierless CORDIC (coordinate rotation digital computer) arithmetic. The switching power consumption is reduced during DCT: the proposed architecture does not perform arithmetic operations of unnecessary bits during the CORDIC calculations. The experiment results show that we can reduce up to 26.1% power dissipation without compromise of the final DCT results. Also, the speed of the proposed architecture is increased about 10%. The proposed low-power DCT architecture can be applied to consumer electronics and portable multimedia systems requiring high throughput and low-power. [J264]

"The interplay of power management and fault recovery in real-time systems"

We describe how to exploit the scheduling slack in a real-time system to reduce energy consumption and achieve fault tolerance at the same time. During failure-free operation, a task takes checkpoints to enable recovery from failure. Additionally, the system exploits the slack to conserve energy by reducing the processor speed. If a task fails, it will restart from a saved checkpoint and execute at maximum speed to guarantee that the deadlines are met. We show that the number of checkpoints and their placements interact in subtle ways with the power management policy. We study two checkpoint placement policies for aperiodic tasks and analytically derive the optimal number of checkpoints to conserve energy under each. This optimal number allows the CPU speed to be slowed down to the level that yields minimum energy consumption, while still

guaranteeing recoverability of tasks under each checkpointing policy. The results show that traditional periodic checkpointing is not the best policy for the combined purpose of conserving energy and guaranteeing recovery. Instead, better energy savings are possible through a nonuniform distribution of checkpoints that takes into account the energy consumption and reliability factors. Depending on the amount of slack and the checkpointing overhead, energy can be reduced by up to 68 percent under nonuniform checkpointing. We also demonstrate the applicability of these checkpoint placement policies to periodic tasks. [J265]

"Power-aware branch prediction: characterization and design"

This uses Wattch and the SPEC 2000 integer and floating-point benchmarks to explore the role of branch predictor organization in power/energy/performance trade offs for processor design. Even though the direction predictor by itself represents less than 1 percent of the processor's total power dissipation, prediction accuracy is nevertheless a powerful lever on processor behavior and program execution time. A thorough study of branch predictor organizations shows that, as a general rule, to reduce overall energy consumption in the processor, it is worthwhile to spend more power in the branch predictor if this results in more accurate predictions that improve running time. This not only improves performance, but can also improve the energy-delay product by up to 20 percent. Three techniques, however, can reduce power dissipation without harming accuracy. Banking reduces the portion of the branch predictor that is active at any one time. A new on-chip structure, the prediction probe detector (PPD), uses predecode bits to entirely eliminate unnecessary predictor and branch target buffer (BTB) accesses. Despite the extra power that must be spent accessing it, the PPD reduces local predictor power and energy dissipation by about 31 percent and overall processor power and energy dissipation by 3 percent. These savings can be further improved by using profiling to annotate branches, identifying those that are highly biased and do not require static prediction. Finally, we explore the effectiveness of a previously proposed technique, pipeline gating, and find that, even with adaptive control based on recent predictor accuracy, pipeline gating yields little or no energy savings. [J266]

"Array regrouping and its use in compiling data-intensive, embedded applications"

One of the key challenges facing computer architects and compiler writers is the increasing discrepancy between processor cycle times and main memory access times. To alleviate this problem in array-intensive embedded signal and video processing applications, compilers may employ either control-centric transformations that change data access patterns of nested loops or data-centric transformations that modify memory layouts of multidimensional arrays. Most of the memory layout optimizations proposed so far either modify the layout of each array independently or are based on explicit data reorganizations at runtime. We focus on a compiler technique, called array regrouping, that automatically maps multiple arrays into a single data (array) space to improve data access pattern. We present a mathematical framework that enables us to systematically derive suitable mappings for a given array-intensive embedded application. The framework divides the arrays accessed in a given program into several groups and each group is independently layout-transformed to improve spatial locality and reduce the number of conflict misses. As compared to the previous approaches, the proposed technique makes two new contributions: 1) It presents a graph based formulation of the array regrouping problem and 2) it demonstrates potential benefits of this aggressive array-regrouping strategy in optimizing behavior of embedded systems. Extensive experimental results demonstrate significant improvements in cache miss rates and execution times. An important advantage of this approach over the previous techniques that target conflict misses is that it reduces conflict misses without increasing the data space requirements of the application being optimized. This is a very desirable property in many embedded/portable environments where data space requirements determine the minimum physical memory capacity. In addition to performance related issues, with the increased use of embedded/portable devices, improving energy efficiency of applications is becoming a critical issue. To develop a truly energy-efficient system, energy constraints should be taken into account early in the design process, i.e., at the source level in software compilation and behavioral level in hardware compilation. Source-- level optimizations are particularly important in data-dominated media applications. We also show how our array regrouping strategy increases energy savings from using multiple low-power operating modes provided in current memory modules. Using a set of array-intensive benchmarks, we observe significant savings in memory system energy. [J267]

"Low-power design using multiple channel lengths and oxide thicknesses"

Two CMOS design techniques use dual threshold voltages to reduce power consumption while maintaining high performance. Simulation results show power savings of 21% for one technique at low activity, and for the other, 19% at high activity and 38% at tow activity. [J268]

"Power minimization in a backlit TFT-LCD display by concurrent brightness and contrast scaling"

This paper presents a concurrent brightness and contrast scaling (CBCS) technique for a cold cathode fluorescent lamp (CCFL) back/it TFT-LCD display. The proposed technique aims at conserving power by reducing the backlight illumination while retaining the image fidelity through preservation of the image contrast. First, we explain how CCFL works and show how to model the non-linearity between its backlight illumination and power consumption. Next, we propose the contrast distortion metric to quantify the image quality loss after backlight scaling. Finally, we formulate and optimally solve the CBCS optimization problem subject to contrast distortion. Experimental results show that an average of 3.7X power saving can be achieved with only 10% of contrast distortion. [J269]

"Automatic rate adaptation and energy-saving mechanisms based on cross-layer information for packet-switched data networks"

A set of novel PHY-MAC mechanisms based on a cross layer dialogue have been proposed, and their performance has been analyzed. System efficiency improvement is achieved by means of automatic transmission rate adaptation, trading off bit rate for power, with resulting energy saving features in a generic packet-switched CDMA access network. The rate adaptation mechanism improves spectrum efficiency while keeping packet delay minimized. On the other hand, power dependent strategies reduce power consumption and intercell interference. Simulation results show that the benefits obtained are very encouraging, so the proposed schemes could be used in future communication systems. [J270]

"Access pattern restructuring for memory energy"

Improving memory energy consumption of programs that manipulate arrays is an important problem as these codes spend large amounts of energy in accessing off-chip memory. We propose a data-driven strategy to optimize the memory energy consumption in a banked memory system. Our compiler-based strategy modifies the original execution order of loop iterations in array-dominated applications to increase the length of the time period(s) in which memory banks are idle (i.e., not accessed by any loop iteration). To achieve this, it first classifies loop iterations according to their bank accesses patterns and then, with the help of a polyhedral tool, tries to bring the iterations with similar bank access patterns close together. Increasing the idle periods of memory banks brings two major benefits: first, it allows us to place more memory banks into low-power operating modes and, second, it enables us to use a more aggressive (i.e., more energy saving) operating mode (hence, saving more energy) for a given bank (instead of a less aggressive mode). The proposed strategy can reduce memory energy consumption in both sequential and parallel applications. Our strategy has been implemented in an experimental compiler using a polyhedral tool and evaluated using nine array-dominated applications on both a cacheless system and a system with cache memory. Our experimental results indicate that the proposed strategy is very successful in reducing the memory system energy and improves the memory energy by as much as 36.8 percent over a strategy that uses low-power modes without optimizing data access pattern. Our results also show that optimizations that target reducing off-chip memory energy can generate very different results from those that target at improving only cache locality. [J271]

"An 800-MHz low-power direct digital frequency synthesizer with an on-chip D/a converter"

An 800-MHz low-power direct digital frequency synthesizer (DDFS) with an on-chip digital-to-analog (D/A) converter is presented. The DDFS consists of a phase accumulator, two phase-to-sine converters, and a D/A converter. The high-speed operation of the DDFS is enabled by applying parallelism to the phase-to-sine converter and by including a D/A converter in a single chip. The on-chip D/A converter saves delay and power consumption due to interchip interconnections. The DDFS considerably reduces power consumption by using several low-power techniques. The pipelined parallel accumulator consumes only 22% power of a conventional pipelined accumulator with the same throughput. The quad line approximation (QLA) and the quantization and error ROM (QE-ROM) minimize the ROM to generate a sine wave. The QLA saves 4 bits of the sine amplitude by approximating the sine function with four lines. The QE-ROM quantizes the ROM data by magnitude and address and then it stores the quantized values and the quantization errors separately. The ROM size for a 9-bit sine output is only 368 bits. A DDFS chip is fabricated in a 0.35-μm CMOS process. It consumes only 174 mW at 800 MHz with 3.3 V. The chip core area is 1.47 mm2. The spurious-free dynamic range (SFDR) is 55 dBc. [J272]

"A low-power content-addressable memory (CAM) using pipelined hierarchical search scheme"

This paper presents two techniques to reduce power consumption in content-addressable memories (CAMs). The first technique is to pipeline the search operation by breaking the match-lines into several segments. Since most stored words fail to match in their first segments, the search operation is discontinued for subsequent segments, hence reducing power. The second technique is to broadcast small-swing search data on less

capacitive global search-lines, and only amplify this signal to full swing on a shorter local search-line. As few match-line segments are active, few local search-lines will be enabled, again saving power. We have employed the proposed schemes in a 1024Ч144-bit ternary CAM in 1.8-V 0.18-μm CMOS, illustrating an overall power reduction of 60% compared to a nonpipelined, nonhierarchical architecture. The ternary CAM achieves a 7-ns search cycle time at 2.89fJ/bit/search. [J273]

"Distributed sleep transistor network for power reduction"

Sleep transistors are effective to reduce leakage power during standby modes. The cluster-based design was proposed to save sleep transistor area by clustering gates to minimize the simultaneous switching current per cluster and inserting a sleep transistor per cluster. In this paper, we propose a novel distributed sleep transistor network (DSTN), and show that DSTN is intrinsically better than the cluster-based design in terms of the sleep transistor area and circuit performance. We reveal properties of optimal DSTN designs, and then develop an efficient algorithm for gate level DSTN synthesis. The algorithm obtains DSTN designs with up to 70.7% sleep transistor area reduction compared to cluster-based designs. Furthermore, we present custom layout designs to verify the area reduction by DSTN. [J274]

"Low-power high-performance reconfigurable computing cache architectures"

The demand for higher computing power and, thus, more on-chip computing resources; is ever increasing. The size of on-chip cache memory has also been consistently increasing to keep up with developments in implementation technology. However, some applications may not utilize full cache capacity and, on the contrary, require more computing resources. To efficiently utilize silicon real-estate on the chip, we exploit the possibility of using a part of cache memory for computational purposes to strike a balance in the usage of memory and computing resources for various applications. In an earlier part of our work, the idea of adaptive balanced computing (ABC) architecture was evolved, where a module of an L1 data cache is used as a coprocessor controlled by main processor. A part of an L1 data cache is designed as a reconfigurable functional cache (RFC) that can be configured to perform a selective core function in the media application whenever such computing capability is required. ABC architecture provides speedups ranging from 1.04x to 5.0x for various media applications. We show that a reduced number of cache accesses and lesser utilization of other on-chip resources, due to a significant reduction in execution time of application, will result in power savings. For this purpose, we first develops a model to compute the power consumed by the RFC while accelerating the computation of multimedia applications. The results show that up to a 60 percent reduction in power consumption is achieved for MPEG decoding and a reduction in the range of 10 to 20 percent for various other multimedia applications. Besides, beyond the discussions in earlier work on ABC architecture, we present a detailed circuit level implementation of the core functions in the RFC modules. Further, we go much further and study the impact of converting the conventional cache into RFC on both access time and energy consumption. The analysis is performed on a wide spectrum of cache organizations with size varying from 8KB to 256KB for varying set associativity. [J275]

"Power-aware scheduling for AND/OR graphs in real-time systems"

Power aware computing has become popular, recently and many techniques have been proposed to manage processor energy consumption for traditional real-time applications. In this paper, we are concerned mainly with the AND/OR model of real-time applications that have different execution paths consisting of different tasks. The contribution of this paper is twofold. First, we propose a greedy slack stealing algorithm to deal with applications represented by AND/OR graphs and prove its correctness in terms of meeting the timing constraints. Then, using statistical information about the applications, we propose a few variations of speculative scheduling algorithms that intend to save energy by reducing the number of speed changes (and, thus, the overhead) while ensuring that the application meets its timing constraints. Some practical issues are also considered, such as shared memory access contention and idle energy consumption. The performance of the algorithms is analyzed with respect to processor energy savings. The results surprisingly show that the greedy slack stealing scheme is better than some speculative schemes and that the greedy scheme is good enough when a reasonable minimal speed exists in the system or when there are only a few (four to six) voltage/speed levels. [J276]

"REMcode: relocating embedded code for improving system efficiency"

The memory hierarchy subsystem has a significant impact on performance and energy consumption of an embedded system. Methods which increase the hit ratio of the cache hierarchy will typically enhance the performance and reduce the embedded system's total energy consumption. This is mainly due to reduced cache-to-memory bus transactions, fewer main memory accesses and fewer processor waiting cycles. A heuristic approach is presented to reduce the total number of cache misses by carefully relocating selected sections of

the application's software code within the main memory, thus reducing conflict misses resulting from the cache hierarchy. The method requires no hardware modifications i.e. it is a software-only approach. For the first time such a method is applied to large program traces, and the miss rates and corresponding energy savings are observed while varying cache size, line size and associativity. Relocating the code consistently produces superior performance on direct-mapped cache. Since direct-mapped caches, being smaller in silicon area than caches with higher associativity (for the same size), cost less in terms of energy/access, and access faster, using direct-mapped instruction cache with code relocation for performance-oriented embedded systems is recommended. A maximum cache miss rate reduction from 71% down to less than 1% is achieved, with energy reductions of up to 63% with only a small increase in main memory size. [J277]

"On optimizing energy consumption for mobile handsets"

To reduce energy consumption (EC), a mobile handset system can be designed in such a way that while the data-receiving unit in a mobile handset is receiving and monitoring data packets, the rest part of the handset (i.e., a processing unit and a user interface) is switched off into a sleep mode. In this paper, we study the timing when the rest part of the handset should wake up. Several schemes (i.e., Always-ON, Always-OFF, Wake-up upon Arrival, Wake-up upon Full, and the fractional threshold scheme) are studied and compared in terms of energy saving and the packet dropping probability (PDP). We formulate the total EC for all theses schemes analytically. Furthermore, we show how to choose optimal thresholds for the fractional threshold scheme for the following two-optimization problems: 1) minimizing the switch-on rate with a bound on the PDP and 2) minimizing the total EC with a bound on the PDP. Our study shows that the fractional threshold scheme is the best scheme. Simulations are carried out to validate analytic models. [J278]

"On the better protection of short-frame turbo codes"

Protecting short data frames by turbo coding is a challenging task because of the small interleaver size and the need for transmission efficiency. In this letter, turbo-decoding-metrics aided short cyclic redundancy check codes are applied to novel tailbiting encoded trellis codes with a twofold purpose: to stop the iterative decoding processes to achieve low-power design and to reduce fractional coding-rate loss. Significant coding gains can be achieved by actually increasing the transmission rate with a negligible increase in power consumption. Performance improvement is demonstrated over additive white Gaussian noise channels. The savings is up to 21.4% for the transmission throughput and 21.5% for the energy consumption of the turbo decoder when frame size 49 is used. [J279]

"Medium access control with coordinated adaptive sleeping for wireless sensor networks"

This paper proposes S-MAC, a medium access control (MAC) protocol designed for wireless sensor networks. Wireless sensor networks use battery-operated computing and sensing devices. A network of these devices will collaborate for a common application such as environmental monitoring. We expect sensor networks to be deployed in an ad hoc fashion, with nodes remaining largely inactive for long time, but becoming suddenly active when something is detected. These characteristics of sensor networks and applications motivate a MAC that is different from traditional wireless MACs such as IEEE 802.11 in several ways: energy conservation and self-configuration are primary goals, while per-node fairness and latency are less important. S-MAC uses a few novel techniques to reduce energy consumption and support self-configuration. It enables low-duty-cycle operation in a multihop network. Nodes form virtual clusters based on common sleep schedules to reduce control overhead and enable traffic-adaptive wake-up. S-MAC uses in-channel signaling to avoid overhearing unnecessary traffic. Finally, S-MAC applies message passing to reduce contention latency for applications that require in-network data processing. The paper presents measurement results of S-MAC performance on a sample sensor node, the UC Berkeley Mote, and reveals fundamental tradeoffs on energy, latency and throughput. Results show that S-MAC obtains significant energy savings compared with an 802.11-like MAC without sleeping. [J280]

"90% write power-saving SRAM using sense-amplifying memory cell"

This paper describes a low-power write scheme which reduces SRAM power by 90% by using seven-transistor sense-amplifying memory cells. By reducing the bitline swing to VDD/6 and amplifying the voltage swing by a sense-amplifier structure in a memory cell, the charging and discharging component of the power of the bit/data lines is reduced. A 64-kb test chip has been fabricated and correct read/write operation has been verified. It is also shown that the scheme can also have the capability of leakage power reduction with small modifications. Achievable leakage power reduction is estimated to be two orders of magnitude from SPICE simulation results. [J281]

"Input space adaptive design: a high-level methodology for optimizing energy and performance"

This paper presents a high-level design methodology, called input space adaptive design, and new design automation algorithms for optimizing energy consumption and performance. Our techniques can be applied to behaviors described in hardware description languages, predesigned register-transfer level (RTL) circuits, or in the context of traditional high-level design methodologies. An input space adaptive design exploits the well-known fact that the quality of circuits can be significantly optimized by employing algorithms and implementation architectures that adapt to input statistics. This paper shows that harnessing the principles of input space adaptive design into a structured high-level design methodology can lead to large improvements in performance and energy consumption. We illustrate the tradeoffs involved in such designs, and demonstrate the need for a systematic design methodology in order to realize the full potential for performance and energy improvements. We propose a methodology for input space adaptive design that consists of the following steps: identification of parts of the behavior that hold the highest potential for optimization, selection of input subspaces whose occurrence can lead to significant reductions in implementation complexity, and transformation of the behavior to realize performance and/or energy savings. Evaluations of performance, energy, and area characteristics of input space adaptive designs in the context of a commercial high-level design flow indicate that such designs can reduce energy consumption by up to 58.9% (average of 40.0%), and simultaneously improve performance by up to 57.5% (average of 41.8%) compared to well-optimized designs that do not employ such techniques. The energy-delay product is reduced by up to 77.9% (average of 64.8%). When the performance improvements are translated into additional energy savings through supply voltage reduction, input space adaptive designs consume up to 74.2% (average of 68.8%) less energy at the same performance. The average area overhead is only 7.4%. [J282]

"View-dependent, scalable texture streaming in 3-D QoS with MPEG-4 visual texture coding"

Multimedia applications are characterized by high resource demands (computing power, memory, network bandwidth, and power consumption). Efficient implementations aim at reducing these resources to a minimum, which is of the utmost importance for small, low-cost terminals in low-bandwidth networks. Resource savings can also be obtained by content adaptation without impeding the quality of the decoded audio-visual media. In this context, the paper analyzes texture adaptation and streaming for three-dimensional applications, using MPEG-4's Visual Texture Coding tool, in conjunction with eXtensible Markup Language (XML)-based description techniques. Augmented features for content adaptation are supported, such as region selection, accompanied by resolution and SNR settings. As a result, quality is optimized for the terminal's computing capabilities and display resolution, taking the user's viewing conditions into account. Moreover, the instantaneous bandwidth utilization is highly reduced in streaming scenarios. [J283]

"Minimizing energy consumption in large-scale sensor networks through distributed data compression and hierarchical aggregation"

In this paper, we study how to reduce energy consumption in large-scale sensor networks, which systematically sample a spatio-temporal field. We begin by formulating a distributed compression problem subject to aggregation (energy) costs to a single sink. We show that the optimal solution is greedy and based on ordering sensors according to their aggregation costs-typically related to proximity-and, perhaps surprisingly, it is independent of the distribution of data sources. Next, we consider a simplified hierarchical model for a sensor network including multiple sinks, compressors/aggregation nodes, and sensors. Using a reasonable metric for energy cost, we show that the optimal organization of devices is associated with a Johnson-Mehl tessellation induced by their locations. Drawing on techniques from stochastic geometry, we analyze the energy savings that optimal hierarchies provide relative to previously proposed organizations based on proximity, i.e., associated Voronoi tessellations. Our analysis and simulations show that an optimal organization of aggregation/compression can yield 8%-28% energy savings depending on the compression ratio. [J284]

"PACE: a new approach to dynamic voltage scaling"

By dynamically varying CPU speed and voltage, it is possible to save significant amounts of energy while still meeting prespecified soft or hard deadlines for tasks; numerous algorithms have been published with this goal. We show that it is possible to modify any voltage scaling algorithm to minimize energy use without affecting perceived performance and present a formula to do so optimally. Because this formula specifies increased speed as the task progresses, we call this approach PACE (Processor Acceleration to Conserve Energy). This optimal formula depends on the probability distribution of the task's work requirement and requires that the speed be varied continuously. We therefore present methods for estimating the task work distribution and evaluate how effective they are on a variety of real workloads. We also show how to approximate the optimal continuous schedule with one that changes speed a limited number of times. Using these methods, we find we can apply PACE practically and efficiently. Furthermore, PACE is extremely effective. Simulations using real workloads and the standard model for energy consumption as a function of voltage show that PACE can reduce the CPU

energy consumption of existing algorithms by up to 49.5 percent, with an average of 20.6 percent, without any effect on perceived performance. The consequent PACE-modified algorithms reduce CPU energy consumption by an average of 65.4 percent relative to no dynamic voltage scaling, as opposed to only 54.3 percent without PACE. [J285]

"A novel multiplexer-based low-power full adder"

The 1-bit full adder circuit is a very important component in the design of application specific integrated circuits. This paper presents a novel low-power multiplexer-based 1-bit full adder that uses 12 transistors (MBA-12T). In addition to reduced transition activity and charge recycling capability, this circuit has no direct connections to the power-supply nodes, leading to a noticeable reduction in short-current power consumption. Intensive HSPICE simulation shows that the new adder has more than 26% in power savings over conventional 28-transistor CMOS adder and it consumes 23% less power than 10-transistor adders (SERF and 10T) and is 64% faster. [J286]

"High-performance FIR filter design based on sharing multiplication"

Finite impulse response (FIR) filtering can be expressed as multiplications of vectors by scalars. We present high-speed designs for FIR filters based on a computation sharing multiplier which specifically targets computation re-use in vector-scalar products. The performance of the proposed implementation is compared with implementations based on carry-save and Wallace tree multipliers in 0.35-μm technology. We show that sharing multiplier scheme improves speed by approximately 52 and 33% with respect to the FIR filter implementations based on the carry-save multiplier and Wallace tree multiplier, respectively. In addition, sharing multiplier scheme has a relatively small power delay product than other multiplier schemes. Using voltage scaling, power consumption of the FIR filter based on computation sharing multiplier can be reduced to 41% of the FIR filter based on the Wallace tree multiplier for the same frequency of operation. [J287]

"A novel coefficient ordering based low power pipelined radix-4 FFT processor for wireless LAN applications"

The FFT processor is a critical block in all multicarrier systems used primarily in the mobile environment. The portability requirement of these systems is mainly responsible for the need of low power FFT architectures. This paper proposes a technique to reduce the power consumption of a popular low power radix-4 pipelined FFT processor by modifying its operation sequence. The complex multiplier is one of the most power consuming blocks in the FFT processor. The switching activity at its fixed coefficient input, and hence its power consumption, can be drastically reduced by coefficient ordering. Coefficient ordering requires a novel commutator architecture which can handle the corresponding data sequencing as per new coefficient ordering. The resulting power saving is around 23% and 9%, respectively, for the 16-point and 64-point radix-4 pipelined FFT processor. This approach is very attractive for orthogonal frequency division multiplexing (OFDM) based wireless LAN (IEEE 802.11) requiring short FFTs but it can also be applied to the penultimate stage of longer FFTs used in digital audio and video broadcasting. [J288]

"Scheduling with dynamic voltage/speed adjustment using slack reclamation in multiprocessor real-time systems"

The high power consumption of modern processors becomes a major concern because it leads to decreased mission duration (for battery-operated systems), increased heat dissipation, and decreased reliability. While many techniques have been proposed to reduce power consumption for uniprocessor systems, there has been considerably less work on multiprocessor systems. In this paper, based on the concept of slack sharing among processors, we propose two novel power-aware scheduling algorithms for task sets with and without precedence constraints executing on multiprocessor systems. These scheduling techniques reclaim the time unused by a task to reduce the execution speed of future tasks and, thus, reduce the total energy consumption of the system. We also study the effect of discrete voltage/speed levels on the energy savings for multiprocessor systems and propose a new scheme of slack reservation to incorporate voltage/speed adjustment overhead in the scheduling algorithms. Simulation and trace-based results indicate that our algorithms achieve substantial energy savings on systems with variable voltage processors. Moreover, processors with a few discrete voltage/speed levels obtain nearly the same energy savings as processors with continuous voltage/speed, and the effect of voltage/speed adjustment overhead on the energy savings is relatively small. [J289]

"Cryogenic cooling temperature of HTS transformers for compactness and efficiency"

A comprehensive thermal design to optimize the cryogenic cooling temperature of HTS transformer is presented,

aiming simultaneously at compactness and efficiency. As small size and low power consumption are conflicting in determining the operating temperature, we develop a general and systematic model to quantify the effects of the temperature on compactness and efficiency. The procedure includes modeling of the critical property of HTS and the winding size, a heat transfer analysis for cooling load estimate, and a thermodynamic evaluation for cryogenic refrigeration. We demonstrate that there exists an optimum for the operating temperature that minimizes the overall power consumption, while taking into account the size effect of HTS windings. The optimal temperature turns out to be slightly above 77 K for two specific systems considered here: liquid-cooled pancake and conduction-cooled solenoid. The operation at temperatures well below 77 K can be justified, if the amount of ac loss is substantially reduced or the saving in capital investment earned by the compactness is significant in comparison with the operational cost. [J290]

"A low-power precomputation-based fully parallel content-addressable memory"

This paper presents a novel VLSI architecture for a fully parallel precomputation-based content-addressable memory (PB-CAM) with low-power, low-cost, and low-voltage features. This design is based on a precomputation approach that saves not only power consumption of the CAM system, but also reduces transistor count and operating voltage of the CAM cell. In addition, the proposed PB-CAM word structure adopts the static pseudo-nMOS circuit design to improve system performance. The whole design was fabricated with the TSMC 0.35-μm single-poly quadruple-metal CMOS process. With a 128 words by 30 bits CAM size, the measurement results indicate that the proposed circuit works up to 100 MHz with power consumption of 33 mW at 3.3-V supply voltage and works up to 30 MHz under 1.5-V supply voltage. [J291]

"Application-specific instruction memory customizations for power-efficient embedded processors"

An encoding technique exploits application information to reduce power consumption along the instruction memory communication path in embedded processors. Microarchitectural support enables reprogrammability of the encoding transformations to track specific code effectively, and the restriction to functional transformations delivers major power savings. Having reprogrammable hardware also allows flexible, inexpensive switches between transformations. [J292]

"High-speed and low-power split-radix FFT"

This paper presents a novel split-radix fast Fourier transform (SRFFT) pipeline architecture design. A mapping methodology has been developed to obtain regular and modular pipeline for split-radix algorithm. The pipeline is repartitioned to balance the latency between complex multiplication and butterfly operation by using carry-save addition. The number of complex multiplier is minimized via a bit-inverse and bit-reverse data scheduling scheme. One can also apply the design methodology described here to obtain regular and modular pipeline for the other Cooley-Tukey-based algorithms. For an N(= 2n)-point FFT, the requirements are log4N-1 multipliers, 4log4N complex adders, and memory of size N-1 complex words for data reordering. The initial latency is N + 2 · log2N clock cycles. On the average, it completes an N-point FFT in N clock cycles. From post-layout simulations, the maximum clock rate is 150 MHz (75 MHz) at 3.3 V (2.7 V), 25°C (100°C) using a 0.35-μm cell library from Avant!. A 64-point SRFFT pipeline design has been implemented and consumes 507 mW at 100 MHz, 3.3 v, and 25°C. Compared with a radix-22FFT implementation, the power consumption is reduced by an amount of 15%, whereas the speed is improved by 14.5%. [J293]

"Adaptive Miller capacitor multiplier for compact on-chip PLL filter"

An adaptive Miller capacitor multiplier is proposed to reduce on-chip phase-locked loop (PLL) capacitor area and improve lock speed. Fabricated in 0.5 μm standard CMOS, an effective capacitance of 576 pF is achieved with a polycapacitor of only 192 pF (62% die area saving) and 0.43 mA current consumption. The lock time is reduced by 36% due to the adaptive loop bandwidth control during PLL settling. [J294]

"A unified approach to reduce SOC test data volume, scan power and testing time"

We present a test resource partitioning (TRP) technique that simultaneously reduces test data volume, test application time, and scan power. The proposed approach is based on the use of alternating run-length codes for test data compression. We present a formal analysis of the amount of data compression obtained using alternating run-length codes. We show that a careful mapping of the don't-cares in precomputed test sets to 1's and 0's leads to significant savings in peak and average power, without requiring either a slower scan clock or blocking logic in the scan cells. We present a rigorous analysis to show that the proposed TRP technique reduces testing time compared to a conventional scan-based scheme. We also improve upon prior work on run-length coding by showing that test sets that minimize switching activity during scan shifting can be more efficiently compressed using alternating run-length codes. Experimental results for the larger ISCAS89

benchmarks and an IBM production circuit show that reduced test data volume, test application time, and low power-scan testing can indeed be achieved in all cases. [J295]

"Minimal energy fixed-priority scheduling for variable voltage processors"

To fully exploit the benefit of variable voltage processors, voltage schedules must be designed in the context of work load requirement. In this paper, we present an approach to finding the least-energy voltage schedule for executing real-time jobs on such a processor according to a fixed priority, preemptive policy. The significance of our approach is that the theoretical limit in terms of energy saving for such systems is established, which can, thus, serve as the standard to evaluate the performance of various heuristic approaches. Two algorithms for deriving the optimal voltage schedule are provided. The first one explores fundamental properties of voltage schedules while the second one builds on the first one to further reduce the computational cost. Experimental results are shown to compare the results of this paper with previous ones. [J296]

"Reducing disk power consumption in servers with DRPM"

Although effective techniques exist for tackling disk power for laptops and workstations, applying them in a server environment presents a considerable challenge, especially under stringent performance requirements. Using a dynamic rotations per minute approach to speed control in server disk arrays can provide significant savings in I/O system power consumption without lessening performance. [J297]

"Dynamic sleep transistor and body bias for active leakage power control of microprocessors"

In order to manage the active power consumption of high-performance digital designs, active leakage control techniques are required to provide significant leakage power savings coupled with fast time constants for entering and exiting idle mode. In this paper, dynamic sleep transistors and body bias are used in conjunction with clock gating to control active leakage for a 32-bit integer execution core in 130-nm CMOS technology. Measurements on pMOS sleep transistor reveal that lowest-leakage state is reached in less than 1 μs, resulting in 37Ч reduction in leakage power, while reactivation of block is achieved in less than two clock cycles. PMOS body bias reduces leakage power by 2Ч with no performance penalty, and similar reactivation time. Power measurements at 4 GHz, 1.3 V, 75°C demonstrate 8% total power reduction using dynamic body bias and 15% power reduction using a pMOS sleep transistor, for a typical activity profile. [J298]

"Analysis of traffic flow with mixed manual and semiautomated vehicles"

The introduction of semiautomated vehicles designed to operate with manually driven vehicles is a realistic near-term objective. The purpose of this paper is to analyze the effects on traffic-flow characteristics and environment when semiautomated vehicles with automatic vehicle following capability (in the same lane) operate together with manually driven vehicles. We have shown that semiautomated vehicles do not contribute to the slinky effect phenomenon when the lead manual vehicle performs smooth acceleration maneuvers. We have demonstrated that semiautomated vehicles help smooth traffic flow by filtering the response of rapidly accelerating lead vehicles. The accurate speed tracking and the smooth response of the semiautomated vehicles designed for passenger comfort reduces fuel consumption and levels of pollutants of following vehicles. This reduction is significant when the lead manual vehicle performs rapid acceleration maneuvers. We have demonstrated using simulations that the fuel consumption and pollution levels present in manual traffic can be reduced during rapid acceleration transients by 28.5% and 1.5%-60.6%, respectively, due to the presence of 10% semiautomated vehicles. These environmental benefits are obtained without any adverse effects on the traffic-flow rates. Experiments with actual vehicles are used to validate the theoretical and simulation results. [J299]

"High-throughput LDPC decoders"

A high-throughput memory-efficient decoder architecture for low-density parity-check (LDPC) codes is proposed based on a novel turbo decoding algorithm. The architecture benefits from various optimizations performed at three levels of abstraction in system design-namely LDPC code design, decoding algorithm, and decoder architecture. First, the interconnect complexity problem of current decoder implementations is mitigated by designing architecture-aware LDPC codes having embedded structural regularity features that result in a regular and scalable message-transport network with reduced control overhead. Second, the memory overhead problem in current day decoders is reduced by more than 75% by employing a new turbo decoding algorithm for LDPC codes that removes the multiple checkto-bit message update bottleneck of the current algorithm. A new merged-schedule merge-passing algorithm is also proposed that reduces the memory overhead of the current algorithm for low to moderate-throughput decoders. Moreover, a parallel soft-input-soft-output (SISO) message update mechanism is proposed that implements the recursions of the Balh-Cocke-Jelinek-Raviv (BCJR) algorithm in terms of simple "max-quartet" operations that do not require lookup-tables and incur negligible loss in

performance compared to the ideal case. Finally, an efficient programmable architecture coupled with a scalable and dynamic transport network for storing and routing messages is proposed, and a full-decoder architecture is presented. Simulations demonstrate that the proposed architecture attains a throughput of 1.92 Gb/s for a frame length of 2304 bits, and achieves savings of 89.13% and 69.83% in power consumption and silicon area over state-of-the-art, with a reduction of 60.5% in interconnect length. [J300]

"An area-saving decoder structure for ROMs"

Read-only memories (ROMs) are widely used in both digital communication systems and daily consumer electronics. The major functions of ROMs are storage of data, programs, firmwares, etc. In this paper, a three-dimensional decoding structure for ROMs is proposed. The number of address decoding stages is drastically shortened. Hence, the delay is reduced, as well as the power consumption and area. The analysis of overall transistor count and delay is thoroughly derived. A real 256 Ч 8 ROM possessing the proposed decoder is physically fabricated by 0.5-μm two-poly two-metal (2P2M) CMOS technology. [J301]

"Fast and memory efficient text image compression with JBIG2"

We investigate ways to reduce encoding time, memory consumption and substitution errors for text image compression with JBIG2. We first look at page striping where the encoder splits the input image into horizontal stripes and processes one stripe at a time. We propose dynamic dictionary updating procedures for page striping to reduce the bit rate penalty it incurs. Experiments show that splitting the image into two stripes can save 30% of encoding time and 40% of physical memory with a small coding loss of about 1.5%. Using more stripes brings further savings in time and memory but the return diminishes. We also propose an adaptive way to update the dictionary only when it has become out-of-date. The adaptive updating scheme can resolve the time versus bit rate tradeoff and the memory versus bit rate tradeoff well simultaneously. We then propose three speedup techniques for pattern matching, the most time-consuming encoding activity in JBIG2. When combined together, these speedup techniques can save up to 75% of the total encoding time with at most 1.7% of bit rate penalty. Finally, we look at improving reconstructed image quality for lossy compression. We propose enhanced prescreening and feature monitored shape unifying to significantly reduce substitution errors in the reconstructed images. [J302]

"Customizing the branch predictor to reduce complexity and energy consumption"

To exploit instruction-level parallelism, high-end processors use branch predictors consisting of many large, often underutilized structures that cause unnecessary energy waste and high power consumption. By adapting the branch target buffer's size and dynamically disabling a hybrid predictor's components, the authors create a customized branch predictor that saves a significant amount of energy with little performance degradation. [J303]

"A low-power charge-recycling ROM architecture"

This paper describes a newly proposed low-power charge-recycling read-only memory (CR-ROM) architecture. The CR-ROM reduces the power consumption in bit lines, word lines, and precharge lines by recycling the previously used charge. In the proposed CR-ROM, bit-line swing voltage is lowered by the charge recycling between bit lines. When N bit lines recycle their charges, the swing voltage and the power of the bit lines become 1/N and 1/N2compared to the conventional ROMs, respectively. As the number of N increases, the power saving in bit lines becomes salient. Also, power consumption in word lines and precharge lines can be reduced theoretically to half by the proposed charge-recycling techniques. The simulation results show that the CR-ROM consumes 60% 85% of the conventional low-power ROMs with 1 K Ч 32 b. A CR-ROM with 32 Kb was implemented in a 0.35-μm CMOS process. The power dissipation is 6.60 mW at 100 MHz with 3.3 V and the maximum operating clock frequency is 150 MHz. [J304]

"Boosters for driving long onchip interconnects-design issues, interconnect synthesis, and comparison with repeaters"

Trends in complementary metal-oxide-semiconductor (CMOS) technology and very large scale integration architectures are causing interconnect to play an increasing role in overall performance, power consumption, and design effort. Traditionally, repeaters are used for driving long onchip interconnects. However, recent studies indicate that repeaters are using increasing area, power, and design resources and are inherently limited in how much they can improve the performance (Adler and Friedman, 1998), (Sylvester and Keutzer, 1999), (Cong and Pan, 1999). The unidirectionality of repeaters also limits their applicability in multisourced lines. This paper presents a new circuit called the Booster that compares favorably with repeaters for driving long lines in terms of area, performance, power, and placement sensitivity. Boosters also have the advantage of being bidirectional and providing a low impedance termination to improve signal integrity. Driver edge rates are reduced and peak

power is drastically reduced compared to repeaters, thus, improving signal integrity and mitigating inductive effects. Boosters are shown to be more than 20% faster for driving a variety of interconnect loads over conventional repeaters in a 0.16-µm CMOS technology. Boosters are typically inserted three times less frequently than repeaters for optimal performance, resulting in fewer boosters for driving the same interconnect lengths and, hence, saving on area, power, and placement effort. Computer-aided design tools for global interconnect synthesis need to support a wider variety of circuit techniques such as boosters. Other exotic circuit techniques such as differential, dynamic, or low-swing techniques require significantly more custom circuit design, noise analysis, extra timing signals, or extra power supplies and are, hence, cumbersome for automatic interconnect synthesis tools. In contrast, the proposed boosters can be inserted on lines in a straightforward manner much like repeaters. Based on analytical delay models, we derive rules for insertion and sizing of boosters that can easily be incorporated into an interconnect synthesis tool. We formulate design rules that determine: 1) the number of boosters needed; 2) their placements; and 3) device sizes for driving a given interconnect load. The primary objective function is minimizing delay and then area and power. Power analysis is slightly more complex than for repeaters so we present a systematic design approach. A placement sensitivity analysis comparing boosters and repeaters is used to study the effects of realistic placement constraints that arise in microprocessor floorplans. We conclude by discussing various design tradeoffs between repeater and booster-based interconnect designs. We then present other potential applications of boosters in domino logic designs, multisource/multisink buses, and field programmable gate array interconnection network designs in addition to conventional point-to-point interconnection lines [J305]

"VTH -hopping scheme to reduce subthreshold leakage for low-power processors"

In order to suppress the power consumption in low-voltage processors, a threshold voltage hopping (VTH-hopping) scheme is proposed where the threshold voltage is dynamically controlled through software depending on a workload. VTH-hopping is shown to reduce the power to 18 % of the fixed low-threshold voltage circuits in 0.5-V supply voltage regime for multimedia applications. A positive back-gate bias scheme with VTH-hopping is presented for the high-performance and low-voltage processors. In order to verify the effectiveness of VTH-hopping, a small-scale RISC processor with VTH-hopping capability and the positive back-gate bias scheme is fabricated in a 0.6-µm CMOS technology. MPEG4 encoding is simulated based on the measured data. The result shows that 86% power saving can be achieved by using VTH-hopping compared with the fixed positive back-gate bias scheme [J306]

"Optimizing sensor networks in the energy-latency-density design space"

In wireless sensor networks, energy efficiency is crucial to achieving satisfactory network lifetime. To reduce the energy consumption significantly, a node should turn off its radio most of the time, except when it has to participate in data forwarding. We propose a new technique, called sparse topology and energy management (STEM), which efficiently wakes up nodes from a deep sleep state without the need for an ultra low-power radio. The designer can trade the energy efficiency of this sleep state for the latency associated with waking up the node. In addition, we integrate STEM with approaches that also leverage excess network density. We show that our hybrid wakeup scheme results in energy savings of over two orders of magnitude compared to sensor networks without topology management. Furthermore, the network designer is offered full flexibility in exploiting the energy-latency-density design space by selecting the appropriate parameter settings of our protocol. [J307]

"Value-sensitive automatic code specialization for embedded software"

The objective of this work is to create a framework for the optimization of embedded software. We present algorithms and a tool flow to reduce the computational effort of programs, using value profiling and partial evaluation. Such a reduction translates into both energy savings and average-case performance improvement, while preserving a tolerable increase of worst case performance and code size. Our tool reduces the computational effort by specializing frequently executed procedures for the most common values of their parameters. The most effective specializations are automatically searched and identified, and the code is transformed through partial evaluation. Experimental results show that their technique improves both energy consumption and performance of the source code up to more than a factor of two, in average about 35% over the original program. Also, their automatic search engine greatly reduces code optimization time with respect to exhaustive search [J308]

"Feasibility test of an electromagnetically driven valve actuator for glaucoma treatment"

Although conventional glaucoma implants have a capability of pressure regulation, they cannot maintain the intraocular pressure (IOP) desired for different patients. In this paper, we present an analysis of the operation of a conventional implant using a bond graph and show its defects and the limitations of a conventional valve

analytically. On the basis of the analysis, the design and fabrication of an active valve actuator is performed considering actuation principles, resistance elements, and control methods. An electromagnetic actuator is used for realizing the active resistance element. A passive resistance element is also included in in order to reduce power consumption. A pulsewidth modulation (PWM) control method is used for enhancing the power consumption saving. Finally, we describe experiments and simulations with the fabricated valve actuator in an in vitro environment, and estimate the in vivo performance from the in vitro experimental results. [J309]

"Low-power scan testing and test data compression for system-on-a-chip"

Test data volume and power consumption for scan vectors are two major problems in system-on-a-chip testing. Since static compaction of scan vectors invariably leads to higher power for scan testing, the conflicting goals of low-power scan testing and reduced test data volume appear to be irreconcilable. We tackle this problem by using test data compression to reduce both test data volume and scan power. In particular, we show that Golomb coding of precomputed test sets leads to significant savings in peak and average power, without requiring either a slower scan clock or blocking logic in the scan cells. We also improve upon prior work on Golomb coding by showing that a separate cyclical scan register is not necessary for pattern decompression. Experimental results for the larger ISCAS 89 benchmarks show that reduced test data volume and low power scan testing can indeed be achieved in all cases [J310]

"Algorithm-based low-power VLSI architecture for 2D mesh video-object motion tracking"

The new VLSI architecture for video object (VO) motion tracking uses a novel hierarchical adaptive structured mesh topology. The structured mesh offers a significant reduction in the number of bits that describe the mesh topology. The motion of the mesh nodes represents the deformation of the VO. Motion compensation is performed using a multiplication-free algorithm for affine transformation, significantly reducing the decoder architecture complexity. Pipelining the affine unit contributes a considerable power saving. The VO motion-tracking architecture is based on a new algorithm. It consists of two main parts: a video object motion-estimation unit (VOME) and a video object motion-compensation unit (VOMC). The VOME processes two consequent frames to generate a hierarchical adaptive structured mesh and the motion vectors of the mesh nodes. It implements parallel block matching motion-estimation units to optimize the latency. The VOMC processes a reference frame, mesh nodes and motion vectors to predict a video frame. It implements parallel threads in which each thread implements a pipelined chain of scalable affine units. This motion-compensation algorithm allows the use of one simple warping unit to map a hierarchical structure. The affine unit warps the texture of a patch at any level of hierarchical mesh independently. The processor uses a memory serialization unit, which interfaces the memory to the parallel units. The architecture has been prototyped using top-down low-power design methodology. Performance analysis shows that this processor can be used in online object-based video applications such as MPEG-4 and VRML [J311]

"A low-swing clock double-edge triggered flip-flop"

A low-swing clock double-edge triggered flip-flop (LSDFF) is developed to reduce power consumption significantly compared to conventional flip-flops. The LSDFF avoids unnecessary internal node transitions to reduce power consumption. In addition, power consumption in the clock tree is reduced because LSDFF uses a double-edge triggered operation as well as a low-swing clock. To prevent performance degradation of the LSDFF due to low-swing clock, low-Vttransistors are used for the clocked transistors without significant leakage current problems. The power saving in flip-flop operation is estimated to be 28.6% to 49.6% with additional 78% power saving in the clock network [J312]

"Architectural energy optimization by bus splitting"

This paper proposes split shared-bus architecture to reduce the energy dissipation for global data exchange among a set of interconnected modules. The bus splitting problem for minimum energy is formulated as a minimum-exchange bus split problem, which is shown to be NP-complete. The problem is solved heuristically by using a maximum-weight matching algorithm and combinatorial search. Experimental results show that the energy saving of split-bus architecture compared to monolithic-bus architecture varies from 16% to 50%, depending on the characteristics of the data transfer among the modules and the configuration of the split-bus. The proposed split-bus architecture can be extended to multiway split-bus architecture when large numbers of modules are to be connected [J313]

"Power-aware operating systems for interactive systems"

Many portable systems deploy operating systems (OS) to support versatile functionality and to manage resources, including power. This paper presents a new approach for using OS to reduce the power consumption

of I/O devices in interactive systems. Low-power OS observes the relationship between hardware devices and processes. The OS kernel estimates the utilization of a device from each process. If a device is not used by any running process, the OS puts it into a low-power state. This paper also explains how scheduling can facilitate power management. When processes are properly scheduled, power reduction can be achieved without degrading performance. We implemented a prototype on Linux to control two devices; experimental results showed nearly 70% power saving on a network card and a hard disk drive [J314]

"Dynamic frequency scaling with buffer insertion for mixed workloads"

This paper presents a method to reduce the energy of interactive systems for mixed workloads: multimedia applications that require constant output rates and sporadic jobs that need prompt responses. The authors' method divides multimedia programs into stages and inserts data buffers between them. Data buffering has three purposes: (1) to support constant output rates; (2) to allow frequency scaling for energy reduction; and (3) to shorten the response times of sporadic jobs. The authors construct frequency-assignment graphs. Each vertex represents the current state of the buffers and the frequencies of the processor. The authors develop an efficient graph-walk algorithm that assigns frequencies to reduce energy. The same method. can be applied to perform voltage scaling and the combination of frequency and voltage scaling. The authors' experimental results on a Strong-ARM-based computer show that four discrete frequencies are sufficient to achieve nearly maximum energy saving. The method reduces the power consumption of an MPEG program by 46%. The authors also demonstrate a case that shortens the response time of a sporadic job by 55%. [J315]

"Energy advantages of microprocessor platforms with on-chip configurable logic"

System chips that incorporate configurable logic can reduce the energy consumed in executing software. The key is to use the configurable logic to execute performance-critical loops, producing average energy savings of 25% to 71% for embedded-system benchmarks. [J316]

"A low power VLSI architecture for mesh-based video motion tracking"

This paper proposes a low-power very large-scale integration (VLSI) architecture for motion tracking. It uses a hierarchical adaptive structured mesh that generates a content-based video representation. The proposed mesh is a coarse-to-fine hierarchical two-dimensional mesh that is formed by recursive triangulation of the initial coarse mesh geometry. The structured mesh offers a significant reduction in the number of bits that describe the mesh topology. The motion of the mesh nodes represents the deformation of the video object. The architecture consists of motion estimation and motion compensation units. The motion estimation architecture generates a progressive mesh code and the motion vectors of the mesh nodes. It reduces the power consumption, uses a simpler approach for mesh construction, approximates the mesh nodes motion vector by using the three step search algorithm and uses a parallel motion estimation core to evaluate the mesh nodes motion vectors. Moreover, it maximizes the lifetime of the internal buffers. The motion compensation architecture uses a multiplication-free algorithm for affine transformation, which significantly reduces the complexity of the motion compensation architecture. Moreover, using pipelined affine units contributes to the power savings. The video motion compensation architecture processes a reference frame, mesh nodes and motion vectors to predict a video frame. It implements parallel threads in which each thread implements a pipelined chain of scalable affine units. This motion compensation algorithm allows the use of one simple warping unit to map a hierarchical structure. The affine unit warps the texture of a patch at any level of hierarchical mesh independently. The processor uses a memory serialization unit, which interfaces the memory to the parallel units. The architecture has been prototyped using top-down low-power design methodology. The performance analysis shows that this processor can be used in online object-based video applications such as in MPEG and VRML. [J317]

"Memory accesses reordering for interconnect power reduction in sum-of-products computations"

Techniques for interconnect power consumption reduction in realizations of sum-of-products computations are presented. The proposed techniques reorder the sequence of accesses of the coefficient and data memories to minimize power-costly address and data bus bit switching. The reordering problem is systematically formulated by mapping into the traveling salesman's problem (TSP) for both single and multiple functional unit architectures. The cost function driving the memory accesses reordering procedure explicitly takes into consideration the static information related to algorithms' coefficients and storage addresses and data-related dynamic information. Experimental results from several typical digital signal-processing algorithms prove that the proposed techniques lead to significant bus switching activity savings. The power consumption in the data paths is reduced in most cases as well. [J318]

"Architectural strategies for low-power VLSI turbo decoders"

The use of "turbo codes" has been proposed for several applications, including the development of wireless systems, where highly reliable transmission is required at very low signal-to-noise ratios (SNR). The problem of extracting the best coding gains from these kind of codes has been deeply investigated in the last years. Also the hardware implementation of turbo codes is a very challenging topic, mainly due to the iterative nature of the decoding process, which demands an operating frequency much higher than the data rate; in the case of wireless applications, the design constraints became even more strict due to the low-cost and low-power requirements. This paper first presents a new architecture for the decoder core with improved area and power dissipation properties; then partitioning techniques are proposed to reduce the power consumption of the decoder memories. It is proven that most of the power is dissipated by the large RAM units required by the decoder, so the described technique is very efficient: an average power saving of 70% with an area overhead of 23% has been obtained on a set of analyzed architectures. [J319]

"An outband paging protocol for energy-efficient mobile communications"

A new protocol is proposed for reducing the power consumption of battery-powered terminals in a mobile computing environment. We exploit the fact that, in a mobile data network, mobile terminals do not continuously receive data and therefore they need not continuously operate their receivers. Nevertheless, they need to check their traffic condition periodically, that is, whether there are pending data for them or not. The proposed energy-efficient protocol is based on a paging procedure wherein a dedicated channel is used to alert (page) terminals with pending traffic. Each terminal may check its traffic condition whenever it decides to by monitoring the paging channel. The protocol is evaluated through an approximated theoretical model and through computer simulation. We focus on deriving approximate formulas for the mean message delay, the message delay variance and the power consumption. It is shown that the proposed protocol can achieve considerable power saving at a cost of increased message delivery delay. [J320]

"Code compression architecture for cache energy minimisation in embedded systems"

Energy consumption of the processor-to-memory path normally accounts for a large fraction of the total energy budget of modern embedded systems. A novel approach for reducing energy consumption in core processors used in systems with cache-based architectures is present. In this scheme, instructions are fetched and stored in the I-cache in compressed form. The beneficial effect is an increase of the cache hit ratio; therefore, the number of accesses to the main memory is reduced, and so is the energy required to fetch the instructions. Static code size reduction is achieved as a by-product. A hardware decompression unit performs fast low-energy on-the-fly instruction decompression at each cache look-up. The decompressor is placed outside the core boundaries: therefore, processor architecture does not need any modification, making the proposed compression approach suitable to JP-based designs. The viability and effectiveness of this solution is assessed through extensive benchmarking performed on a number of typical embedded programs. Beside code size, energy and performance optimisation results, the authors also report data regarding the synthesis and implementation of the decompression unit. The energy penalty it introduces is taken into account in the evaluation of the achieved energy savings [J321]

"Fuzzy-logic-based power control system for multifield electrostatic precipitators"

The power consumption of large precipitators can be in the range of 1 MW and above. Depending on the dust load properties, the electrical power may be reduced by up to 50% by applying fuzzy logic, without significantly increasing the dust emissions. The new approach uses fuzzy logic for optimization of existing electrostatic precipitators. The software runs on a standard personal computer platform under the Windows NT operating system. The controllers of the electrostatic precipitator power supplies are linked to the personal computer via an industrial network (e.g., PROFIBUS). The system determines online the differentials of emission versus electrical power of each field. This measurement is difficult because of overlaid events in the other zones, and process changes. The long response, time of the resultant dust emission due to electrical power changes in the precipitator is an additional complication. Rules were defined for a coarse, but fast-response power adaptation of all zones. Fine tuning the running system after the coarse optimization increased the accuracy and reliability. When installed on a 4Ч5 zone precipitator in a power station, significant results were obtained. The power savings over three months of operation were in the range of 40%-60% depending on the load and fuel characteristics. Data were recorded over the test period of three months. The results are presented. [J322]

"Cool-Fetch: Compiler-Enabled Power-Aware Fetch Throttling"

In this paper, we present an architecturecompiler based approach to reduce energy consumption inthe processor. While we mainly target the fetch unit, an importantside-effect of our approach i s that we obtain energysavings in many other parts in the processor. The explanationis that the fetch unit often runs substantially

ahead ofexecution, bringing in instructions to different stages in theprocessor that may never be executed. We have found, thatalthough the degree of Instruction Level Parallelism (ILP)of a program tends to vary over time, it can be staticallypredicted by the compiler with considerable accuracy. OurInstructions Per Clock (IPC) prediction scheme is using adependence-testing-based analysis and simple heuristics, toguide a front-end fetch-throttling mechanism. We developthe necessary architecture support and include its poweroverhead. We perform experiments over a wide number ofarchitectural configurations, using SPEC2000 applications.Our results are very encouraging: we obtain up to 15%total energy savings in the processor with generally littleperformance degradation. In fact, in some cases our intelligentthrottling scheme even tszcwases performance.Keywords- Low power design, compiler architecture interaction,instruction level parallelism, fetch-throttling [J323]

"ENPCO: an entropy-based partition-codec algorithm to reduce power for bipartition-codec architecture in pipelined circuits"

This work proposes a new algorithm to synthesize low power bipartition-codec architecture for pipelined circuits. The bipartition-codec architecture has been introduced as an effective power reduction technique for circuit design. The entropy-based partition-codec (ENPCO) algorithm extends this approach as it optimizes for both: power and area. It uses entropy as a criterion to balance between power and area. The ENPCO algorithm is composed of two phases: first, it clusters the output vectors with high occurrence into a group, moving all remaining output vectors into another group. The first group will be encoded in order to save power. Secondly, based on circuit entropy, output patterns are moved between both groups in order to balance power consumption and area overhead. A number of Microelectronic Center of North Carolina (MCNC) benchmarks were used to verify the effectiveness of our algorithm. Results demonstrate that ENPCO algorithm can achieve low power with less area overhead than the single-phase algorithm introduced previously by Shanq-Jang Ruan et al. (1999). [J324]

"Event-driven power management"

Energy consumption of electronic devices has become a serious concern in recent years. Power management (PM) algorithms aim at reducing energy consumption at the system-level by selectively placing components into low-power states. Formerly, two classes of heuristic algorithms have been proposed for PM: timeout and predictive. Later, a category of algorithms based on stochastic control was proposed for PM. These algorithms guarantee optimal results as long as the system that is power managed can be modeled well with exponential distributions. We show that there is a large mismatch between measurements and simulation results if the exponential distribution is used to model all user request arrivals. We develop two new approaches that better model system behavior for general user request distributions. Our approaches are event-driven and give optimal results verified by measurements. The first approach we present is based on renewal theory. This model assumes that the decision to transition to low-power state can be made in only one state. Another method we developed is based on the time-indexed semi-Markov decision process (TISMDP) model. This model has wider applicability because it assumes that a decision to transition into a lower-power state can be made upon each event occurrence from any number of states. This model allows for transitions into low-power states from any state, but it is also more complex than our other approach. It is important to note that the results obtained by renewal model are guaranteed to match results obtained by TISMDP model, as both approaches give globally optimal solutions. We implemented our PM algorithms on two different classes of devices: two different hard disks and client-server wireless local area network systems such as the SmartBadge or a laptop. The measurement results show power savings ranging from a factor of 1.7 up to 5.0 with insignificant variation in performance [J325]

"A design for high-speed low-power CMOS fully parallel content-addressable memory macros"

Described is a design for high-speed low-power-consumption fully parallel content-addressable memory (CAM) macros for CMOS ASIC applications. The design supports configurations ranging from 64 words by 8 bits to 2048 words by 64 bits and achieves around 7.5-ns search access times in CAM macros on a 0.35-μm 3.3-V standard CMOS ASIC technology. A new CAM cell with a pMOS match-line driver reduces search rush current and power consumption, allowing a NOR-type match-line structure suitable for high-speed search operations. It is also shown that the CAM cell has other advantages that lead to a simple high-speed current-saving architecture. A small signal on the match line is detected by a single-ended sense amplifier which has both high-speed and low-power characteristics and a latch function. The same type of sense amplifier is used for a fast read operation, realizing 5-ns access time under typical conditions. For further current savings in search operations, the precharging of the match line is controlled based on the valid bit status. Also, a dual bit switch with optimized size and control reduces the current. CAM macros of 256Ч54 configuration on test chips showed 7.3-ns search access time with a power-performance metric of 131 fJ/bit/search under typical conditions [J326]

"Comparing system level power management policies"

Reducing power consumption is a challenge to system designers. Portable systems, such as laptop computers and personal digital assistants (PDAs), draw power from batteries, so reducing power consumption extends their operating times. For desktop computers or servers, high power consumption raises temperature and deteriorates performance and reliability. Soaring energy prices and rising concern about the environmental impact of electronics systems further highlight the importance of low power consumption. Power reduction techniques can be classified as static and dynamic. Static techniques, such as synthesis and compilation for low power, are applied at design time. In contrast, dynamic techniques use runtime behavior to reduce power when systems are serving light workloads or are idle. These techniques are known as dynamic power management (DPM). DPM can be achieved in different ways; for example, dynamic voltage scaling (DVS) changes supply voltage at runtime as a method of power management. Here, we use DPM specifically for shutting down unused I/O devices. We built an experimental environment on a laptop computer running Microsoft Windows. We implemented existing power management policies and quantitatively compared their effects on power saving and performance degradation [J327]

"Stochastic modeling of a power-managed system-construction and optimization"

The goal of a dynamic power management policy is to reduce the power consumption of an electronic system by putting system components into different states, each representing a certain performance and power consumption level. The policy determines the type and timing of these transitions based on the system history, workload, and performance constraints. In this paper we propose a new abstract model of a power-managed electronic system. We formulate the problem of system-level power management as a controlled optimization problem based on the theories of continuous-time Markov derision processes and stochastic networks. This problem is solved exactly using linear programming or heuristically using “policy iteration.” Our method is compared with existing heuristic methods for different workload statistics. Experimental results show that the power management method based on a Markov decision process outperforms heuristic methods by as much as 44% in terms of power dissipation savings for a given level of system performance [J328]

"Conditional-capture flip-flop for statistical power reduction"

This paper describes a family of novel low-power flip-flops, collectively called conditional-capture flip-flops (CCFFs). They achieve statistical power reduction by eliminating redundant transitions of internal nodes. These flip-flops also have negative setup time and thus provide small data-to-output latency and attribute of soft-clock edge for overcoming clock skew-related cycle time loss. The simulation comparison indicates that the proposed differential flip-flop achieves power savings of up to 61% with no impact on latency while the single-ended structure provides the maximum power savings of around 67%, as compared to conventional flip-flops. With a typical switching activity of 0.33, the power consumption is reduced by as much as 23-30% with comparable minimum data-to-output latency. It is also indicated that the proposed single-ended structure provides power comparable to the fully static master-slave design with significantly reduced data-to-output latency. An eight-bit counter was fabricated using a 0.35-μm CMOS technology, and the experimental results indicate that the counter using the differential CCFF saves the overall power consumption by about 30% as compared to that using the conventional flip-flop [J329]

"Optimum voltage swing on on-chip and off-chip interconnect"

Reduced voltage swings are often used for saving power on interconnects. In this paper, we demonstrate the existence of an optimum voltage swing for minimum power consumption, for on-chip and off-chip interconnects. Actual values of optimum swings and corresponding power savings for high performance interconnects are estimated [J330]

СПИСОК ЛИТЕРАТУРЫ

J1. Xiaojun Ruan. A Message-Scheduling Scheme for Energy Conservation in Multimedia Wireless Systems. / Xiaojun Ruan, Shu Yin, Manzanares A., Alghamdi M., Xiao Qin. // IEEE Transactions on Systems, Man and Cybernetics, Part A: Systems and Humans. - 2011. - Vol. 41, No. 2. - P. 272-283. ↑

J2. Chien W.-B. Energy-Saving Cooperative Spectrum Sensing Processor for Cognitive Radio System. / Chien

W.-B., Yang C.-K., Huang Y.-H. // IEEE Transactions on Circuits and Systems I: Regular Papers. - 2011. - Vol. 58, No. 4. - P. 711-723.

J3. Xiaowen Dong. IP Over WDM Networks Employing Renewable Energy Sources. / Xiaowen Dong, El-Gorashi T., Elmirghani J.M.H. // Journal of Lightwave Technology. - 2011. - Vol. 29, No. 1. - P. 3-14.

J4. Myint Wai Phyu. Power-Efficient Explicit-Pulsed Dual-Edge Triggered Sense-Amplifier Flip-Flops. / Myint Wai Phyu, Kangkang Fu, Wang Ling Goh, Kiat-Seng Yeo. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2011. - Vol. 19, No. 1. - P. 1-9.

J5. Ziliang Zong. EAD and PEBD: Two Energy-Aware Duplication Scheduling Algorithms for Parallel Tasks on Homogeneous Clusters. / Ziliang Zong, Manzanares A., Xiaojun Ruan, Xiao Qin. // IEEE Transactions on Computers. - 2011. - Vol. 60, No. 3. - P. 360-374.

J6. Jae-sun Seo. A Robust Edge Encoding Technique for Energy-Efficient Multi-Cycle Interconnect. / Jae-sun Seo, Kaul H., Krishnamurthy R., Sylvester D., Blaauw D. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2011. - Vol. 19, No. 2. - P. 264-273.

J7. Andrei A. Quasi-Static Voltage Scaling for Energy Minimization With Time Constraints. / Andrei A., Eles P., Jovanovic O., Schmitz M., Ogniewski J., Zebo Peng. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2011. - Vol. 19, No. 1. - P. 10-23.

J8. Sundramoorthy V. Domesticating Energy-Monitoring Systems: Challenges and Design Concerns. / Sundramoorthy V., Cooper G., Linge N., Qi Liu. // IEEE Pervasive Computing. - 2011. - Vol. 10, No. 1. - P. 20-27.

J9. Pei-Yu Chen. Power-Efficient and Cost-Effective 2-D Symmetry Filter Architectures. / Pei-Yu Chen, Lan-Da Van, I-Hung Khoo, Reddy H.C., Chin-Teng Lin. // IEEE Transactions on Circuits and Systems I: Regular Papers. - 2011. - Vol. 58, No. 1. - P. 112-125.

J10. Ningde Xie. Using Lossless Data Compression in Data Storage Systems: Not for Saving Space. / Ningde Xie, Guiqiang Dong, Tong Zhang. // IEEE Transactions on Computers. - 2011. - Vol. 60, No. 3. - P. 335-345.

J11. Jae-Wan Jang. Energy Reduction in Consolidated Servers through Memory-Aware Virtual Machine Scheduling. / Jae-Wan Jang, Myeongjae Jeon, Hyo-Sil Kim, Heeseung Jo, Jin-Soo Kim, Seungryoul Maeng. // IEEE Transactions on Computers. - 2011. - Vol. 60, No. 4. - P. 552-564.

J12. Farrell T. Processing Continuous Range Queries with Spatiotemporal Tolerance. / Farrell T., Rothermel K., Cheng R. // IEEE Transactions on Mobile Computing. - 2011. - Vol. 10, No. 3. - P. 320-334.

J13. Sharangi S. Energy-Efficient Multicasting of Scalable Video Streams Over WiMAX Networks. / Sharangi S., Krishnamurti R., Hefeeda M. // IEEE Transactions on Multimedia. - 2011. - Vol. 13, No. 1. - P. 102-115.

J14. Qi Zhang. A 2.4-GHz Energy-Efficient Transmitter for Wireless Medical Applications. / Qi Zhang, Peng Feng, Zhiqing Geng, Xiaozhou Yan, Nanjian Wu. // IEEE Transactions on Biomedical Circuits and Systems. - 2011. - Vol. 5, No. 1. - P. 39-47.

J15. Jong-Woon Yoo. A Cooperative Clustering Protocol for Energy Saving of Mobile Devices with WLAN and Bluetooth Interfaces. / Jong-Woon Yoo, Kyu Ho Park. // IEEE Transactions on Mobile Computing. - 2011. - Vol. 10, No. 4. - P. 491-504.

J16. Apolloni R. Hybrid timing-address oriented load-store queue filtering for an x86 architecture. / Apolloni R., Chaver D., Rodriguez F.C., Pinuel L., Prieto M., Tirado F. // IET Computers & Digital Techniques. - 2011. - Vol. 5, No. 2. - P. 145-157.

J17. Ying-Wen Bai. Design and implementation of a home embedded surveillance system with ultra-low alert power. / Ying-Wen Bai, Zi-Li Xie, Zong-Han Li. // IEEE Transactions on Consumer Electronics. - 2011. - Vol. 57, No. 1. - P. 153-159.

J18. Skubic B. Evaluation of ONU power saving modes for gigabit-capable passive optical networks. / Skubic B., Hood D. // IEEE Network. - 2011. - Vol. 25, No. 2. - P. 20-24.

J19. Jinsoo Han. More efficient home energy management system based on ZigBee communication and infrared remote controls. / Jinsoo Han, Chang-Sic Choi, Ilwoo Lee. // IEEE Transactions on Consumer Electronics. - 2011. - Vol. 57, No. 1. - P. 85-89.

J20. Humar I. Rethinking energy efficiency models of cellular networks with embodied energy. / Humar I., Ge X., Xiang L., Jo M., Chen M., Zhang J. // IEEE Network. - 2011. - Vol. 25, No. 2. - P. 40-49.

J21. Ericson Chua. Mixed bio-signal lossless data compressor for portable brain-heart monitoring systems. / Ericson Chua, Wai-Chi Fang. // IEEE Transactions on Consumer Electronics. - 2011. - Vol. 57, No. 1. - P. 267-273.

J22. Arroyo-Valles R. Optimal Selective Forwarding for Energy Saving in Wireless Sensor Networks. / Arroyo-Valles R., Marques A.G., Cid-Sueiro J. // IEEE Transactions on Wireless Communications. - 2011. - Vol. 10, No. 1. - P. 164-175.

J23. Majzoub S.S. Energy Optimization for Many-Core Platforms: Communication and PVT Aware Voltage-Island Formation and Voltage Selection Algorithm. / Majzoub S.S., Saleh R.A., Wilton S.J.E., Ward R.K. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2010. - Vol. 29, No. 5. - P. 816-829.

J24. Bachir A. MAC Essentials for Wireless Sensor Networks. / Bachir A., Dohler M., Watteyne T., Leung K.K. // IEEE Communications Surveys & Tutorials. - 2010. - Vol. 12, No. 2. - P. 222-248.

J25. Musoll E. Hardware-Based Load Balancing for Massive Multicore Architectures Implementing Power Gating. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2010. - Vol. 29, No. 3. - P. 493-497.

J26. Fang-Cheng Lin. Color Filter-Less LCDs in Achieving High Contrast and Low Power Consumption by Stencil Field-Sequential-Color Method. / Fang-Cheng Lin, Yi-Pai Huang, Ching-Ming Wei, Shieh H.-P.D. // Journal of Display Technology. - 2010. - Vol. 6, No. 3. - P. 98-106.

J27. Chowdhury P. Building a Green Wireless-Optical Broadband Access Network (WOBAN). / Chowdhury P., Tornatore M., Sarkar S., Mukherjee B. // Journal of Lightwave Technology. - 2010. - Vol. 28, No. 16. - P. 2219-2229.

J28. Uluagac A.S. VEBEK: Virtual Energy-Based Encryption and Keying for Wireless Sensor Networks. / Uluagac A.S., Beyah R.A., Yingshu Li, Copeland J.A. // IEEE Transactions on Mobile Computing. - 2010. - Vol. 9, No. 7. - P. 994-1007.

J29. Cicconetti C. Reducing Power Consumption with QoS Constraints in IEEE 802.16e Wireless Networks. / Cicconetti C., Lenzini L., Mingozzi E., Vallati C. // IEEE Transactions on Mobile Computing. - 2010. - Vol. 9, No. 7. - P. 1008-1021.

J30. Wan-Ki Park. Energy efficient multi-function home gateway in always-on home environment. / Wan-Ki Park, Chang-sic Choi, Il-woo Lee, Jonghyun Jang. // IEEE Transactions on Consumer Electronics. - 2010. - Vol. 56, No. 1. - P. 106-111.

J31. Qiang Ma. Multivoltage Floorplan Design. / Qiang Ma, Young E. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2010. - Vol. 29, No. 4. - P. 607-617.

J32. Rakvic R. Energy efficiency via thread fusion and value reuse. / Rakvic R., Gonzalez J., Cai Q., Chaparro P., Magklis G., Gonzalez A. // IET Computers & Digital Techniques. - 2010. - Vol. 4, No. 2. - P. 114-125.

J33. Reviriego P. Burst Transmission for Energy-Efficient Ethernet. / Reviriego P., Maestro J.A., Herna,ndez J.A., Larrabeiti D. // IEEE Internet Computing. - 2010. - Vol. 14, No. 4. - P. 50-57.

J34. Jong-Ju Hong. A clipping reduction algorithm using backlight luminance compensation for local dimming liquid crystal displays. / Jong-Ju Hong, Seong-Eun Kim, Woo-Jin Song. // IEEE Transactions on Consumer Electronics. - 2010. - Vol. 56, No. 1. - P. 240-246.

J35. Sang-Wook Kwon. Enhanced power saving through increasing unavailability interval in the IEEE 802.16e systems. / Sang-Wook Kwon, Dong-Ho Cho. // IEEE Communications Letters. - 2010. - Vol. 14, No. 1. - P. 24-

26.

J36. Namboodiri V. Energy-Efficient VoIP over Wireless LANs. / Namboodiri V., Lixin Gao. // IEEE Transactions on Mobile Computing. - 2010. - Vol. 9, No. 4. - P. 566-581.

J37. Dreslinski R.G. Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits. / Dreslinski R.G., Wieckowski M., Blaauw D., Sylvester D., Mudge T. // Proceedings of the IEEE. - 2010. - Vol. 98, No. 2. - P. 253-266.

J38. Ningde Xie. Using Embedded Dynamic Random Access Memory to Reduce Energy Consumption of Magnetic Recording Read Channel. / Ningde Xie, Tong Zhang, Haratsch E.F. // IEEE Transactions on Magnetics. - 2010. - Vol. 46, No. 1. - P. 87-91.

J39. Xuan Guan. Register File Partitioning and Compiler Support for Reducing Embedded Processor Power Consumption. / Xuan Guan, Yunsi Fei. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2010. - Vol. 18, No. 8. - P. 1248-1252.

J40. Eunju Hwang. The Power-Saving Mechanism With Periodic Traffic Indications in the IEEE 802.16e/m. / Eunju Hwang, Kyung Jae Kim, Jung Je Son, Bong Dae Choi. // IEEE Transactions on Vehicular Technology. - 2010. - Vol. 59, No. 1. - P. 319-334.

J41. Merlin C.J. Schedule Adaptation of Low-Power-Listening Protocols for Wireless Sensor Networks. / Merlin C.J., Heinzelman W.B. // IEEE Transactions on Mobile Computing. - 2010. - Vol. 9, No. 5. - P. 672-685.

J42. Alimadadi M. A 4 GHz Non-Resonant Clock Driver With Inductor-Assisted Energy Return to Power Grid. / Alimadadi M., Sheikhaei S., Lemieux G., Mirabbasi S., Dunford W., Palmer P. // IEEE Transactions on Circuits and Systems I: Regular Papers. - 2010. - Vol. 57, No. 8. - P. 2099-2108.

J43. Ik Joon Chang. Exploring Asynchronous Design Techniques for Process-Tolerant and Energy-Efficient Subthreshold Operation. / Ik Joon Chang, Sang Phill Park, Roy K. // IEEE Journal of Solid-State Circuits. - 2010. - Vol. 45, No. 2. - P. 401-410.

J44. Seok-Hoon Kim. A 116 fps/74 mW Heterogeneous 3D-Media Processor for 3-D Display Applications. / Seok-Hoon Kim, Hong-Yun Kim, Young-Jun Kim, Kyusik Chung, Donghyun Kim, Lee-Sup Kim. // IEEE Journal of Solid-State Circuits. - 2010. - Vol. 45, No. 3. - P. 652-667.

J45. Shiann-Rong Kuang. Design of Power-Efficient Configurable Booth Multiplier. / Shiann-Rong Kuang, Jiun-Ping Wang. // IEEE Transactions on Circuits and Systems I: Regular Papers. - 2010. - Vol. 57, No. 3. - P. 568-580.

J46. Jongsun Park. Dynamic Bit-Width Adaptation in DCT: An Approach to Trade Off Image Quality and Computation Energy. / Jongsun Park, Jung Hwan Choi, Roy K. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2010. - Vol. 18, No. 5. - P. 787-793.

J47. Yang Liu. Computation Error Analysis in Digital Signal Processing Systems With Overscaled Supply Voltage. / Yang Liu, Tong Zhang, Parhi K.K. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2010. - Vol. 18, No. 4. - P. 517-526.

J48. Namboodiri V. Energy-Aware Tag Anticollision Protocols for RFID Systems. / Namboodiri V., Lixin Gao. // IEEE Transactions on Mobile Computing. - 2010. - Vol. 9, No. 1. - P. 44-59.

J49. Braithwait S. Behavior Modification. IEEE Power and Energy Magazine. - 2010. - Vol. 8, No. 3. - P. 36-45.

J50. Seunghyun Park. Concurrent simulation platform for energy-aware smart metering systems. / Seunghyun Park, Hanjoo Kim, Hichan Moon, Jun Heo, Sungroh Yoon. // IEEE Transactions on Consumer Electronics. - 2010. - Vol. 56, No. 3. - P. 1918-1926.

J51. Zhen Fang. Boomerang: Reducing Power Consumption of Response Packets in NoCs with Minimal Performance Impact. / Zhen Fang, Hallnor E.G., Bin Li, Leddige M., Donglai Dai, Seung Eun Lee, Makineni S., Iyer R. // Computer Architecture Letters. - 2010. - Vol. 9, No. 2. - P. 49-52.

J52. Christensen K. IEEE 802.3az: the road to energy efficient ethernet. / Christensen K., Reviriego P., Nordman B., Bennett M., Mostowfi M., Maestro J.A. // IEEE Communications Magazine. - 2010. - Vol. 48, No. 11. - P. 50-56.

J53. Yeong-Kang Lai. A reconfigurable IDCT architecture for universal video decoders. / Yeong-Kang Lai, Yu-Fan Lai. // IEEE Transactions on Consumer Electronics. - 2010. - Vol. 56, No. 3. - P. 1872-1879.

J54. Huang Bo. DRX-Aware Scheduling Method for Delay-Sensitive Traffic. / Huang Bo, Tian Hui, Chen Lan, Zhu Jianchi. // IEEE Communications Letters. - 2010. - Vol. 14, No. 12. - P. 1113-1115.

J55. Young-Sung Son. Home energy management system based on power line communication. / Young-Sung Son, Pulkkinen T., Kyeong-Deok Moon, Chaekyu Kim. // IEEE Transactions on Consumer Electronics. - 2010. - Vol. 56, No. 3. - P. 1380-1386.

J56. An He. Energy consumption minimization for mobile and wireless devices-a cognitive approach. / An He, Srikanteswara S., Bae K.K., Reed J.H., Tranter W.H. // IEEE Transactions on Consumer Electronics. - 2010. - Vol. 56, No. 3. - P. 1814-1821.

J57. Dong-Sun Kim. A wireless sensor node SoC with a profiled power management unit for IR controllable digital consumer devices. / Dong-Sun Kim, Byung-Soo Kim, Kwang-Ho Won, Min-Soo Kang. // IEEE Transactions on Consumer Electronics. - 2010. - Vol. 56, No. 4. - P. 2282-2287.

J58. Wanhyung Ryu. Design and implementation of a disk energy saving scheme for media players which use hybrid disks. / Wanhyung Ryu, Minseok Song. // IEEE Transactions on Consumer Electronics. - 2010. - Vol. 56, No. 4. - P. 2382-2386.

J59. Hyoungsik Nam. A color compensation algorithm to avoid color distortion in active dimming liquid crystal displays. IEEE Transactions on Consumer Electronics. - 2010. - Vol. 56, No. 4. - P. 2569-2576.

J60. Hyunsuk Cho. A local dimming algorithm for low power LCD TVs using edge-type LED backlight. / Hyunsuk Cho, Oh-Kyong Kwon. // IEEE Transactions on Consumer Electronics. - 2010. - Vol. 56, No. 4. - P. 2054-2060.

J61. Correia L.M. Challenges and enabling technologies for energy aware mobile radio networks. / Correia L.M., Zeller D., Blume O., Ferling D., Jading Y., Go,dor I., Auer G., Van Der Perre L. // IEEE Communications Magazine. - 2010. - Vol. 48, No. 11. - P. 66-72.

J62. Zhisheng Niu. Cell zooming for cost-efficient green cellular networks. / Zhisheng Niu, Yiqun Wu, Jie Gong, Zexi Yang. // IEEE Communications Magazine. - 2010. - Vol. 48, No. 11. - P. 74-79.

J63. Sartor D. Money for Research, Not Energy Bills: Finding Energy and Cost Savings in High-Performance Computer Facility Designs. / Sartor D., Wilson M. // Computing in Science & Engineering. - 2010. - Vol. 12, No. 6. - P. 11-19.

J64. Kubo R. Study and Demonstration of Sleep and Adaptive Link Rate Control Mechanisms for Energy Efficient 10G-EPON. / Kubo R., Kani J.-i., Ujikawa H., Sakamoto T., Fujimoto Y., Yoshimoto N., Hadama H. // IEEE/OSA Journal of Optical Communications and Networking. - 2010. - Vol. 2, No. 9. - P. 716-729.

J65. Hsu C.-H. Performance enhancement and analysis for IEEE 802.16e/m sleep mode operations with unsolicited grant service/real-time variable-rate connections. / Hsu C.-H., Feng K.-T. // IET Communications. - 2010. - Vol. 4, No. 9. - P. 1083-1094.

J66. Azam T. Efficient sensor for robust low-power design in nano-CMOS technologies. / Azam T., Cumming D.R.S. // Electronics Letters. - 2010. - Vol. 46, No. 11. - P. 773-775.

J67. Merlin C.J. Duty Cycle Control for Low-Power-Listening MAC Protocols. / Merlin C.J., Heinzelman W.B. // IEEE Transactions on Mobile Computing. - 2010. - Vol. 9, No. 11. - P. 1508-1521.

J68. Donghwa Shin. Energy-Optimal Dynamic Thermal Management: Computation and Cooling Power Co-Optimization. / Donghwa Shin, Sung Woo Chung, Eui-Young Chung, Naehyuck Chang. // IEEE Transactions on Industrial Informatics. - 2010. - Vol. 6, No. 3. - P. 340-351.

J69. Hyungjun Kim. Leveraging Unused Cache Block Words to Reduce Power in CMP Interconnect. / Hyungjun Kim, Gratz P. // Computer Architecture Letters. - 2010. - Vol. 9, No. 1. - P. 33-36.

J70. Bartram L. Chasing the Negawatt: Visualization for Sustainable Living. / Bartram L., Rodgers J., Muise K. // IEEE Computer Graphics and Applications. - 2010. - Vol. 30, No. 3. - P. 8-14.

J71. Luiz S.O.D. Multisize Sliding Window in Workload Estimation for Dynamic Power Management. / Luiz S.O.D., Perkusich A., Lima A.M.N. // IEEE Transactions on Computers. - 2010. - Vol. 59, No. 12. - P. 1625-1639.

J72. Ming-Hsin Huang. Energy-Recycling (ER) Technique for a Direct-Lit Intelligent Power Management Backlight Unit (BLU). / Ming-Hsin Huang, Yueh-Chang Tsai, Ke-Horng Chen. // IEEE Transactions on Power Electronics. - 2010. - Vol. 25, No. 10. - P. 2588-2598.

J73. Grass N. Electrostatic Precipitator Control Systems. / Grass N., Zintl A., Hoffmann E. // IEEE Industry Applications Magazine. - 2010. - Vol. 16, No. 4. - P. 28-33.

J74. Se Hun Kim. System-Level Energy Optimization for Error-Tolerant Image Compression. / Se Hun Kim, Mukohopadhyay S., Wolf M. // IEEE Embedded Systems Letters. - 2010. - Vol. 2, No. 3. - P. 81-84.

J75. Zhu Yi-hua. Efficient Power Management for Infrastructure IEEE 802.11 WLANs. / Zhu Yi-hua, Leung Victor C.M. // IEEE Transactions on Wireless Communications. - 2010. - Vol. 9, No. 7. - P. 2196-2205.

J76. Chung-Hsien Hsu. Statistical Control Approach for Sleep-Mode Operations in IEEE 802.16m Systems. / Chung-Hsien Hsu, Kai-Ten Feng, Chung-Ju Chang. // IEEE Transactions on Vehicular Technology. - 2010. - Vol. 59, No. 9. - P. 4453-4466.

J77. Lee M.J. IEEE 802.15.5 WPAN mesh standard-low rate part: Meshing the wireless sensor networks. / Lee M.J., Rui Zhang, Jianliang Zheng, Gahng-Seop Ahn, Chunhui Zhu, Tae Rim Park, Sung Rae Cho, Chang Sub Shin, Jun Sun Ryu. // IEEE Journal on Selected Areas in Communications. - 2010. - Vol. 28, No. 7. - P. 973-983.

J78. Beraldi R. A Biased Random Walk Routing Protocol for Wireless Sensor Networks: The Lukewarm Potato Protocol. / Beraldi R., Baldoni R., Prakash R. // IEEE Transactions on Mobile Computing. - 2010. - Vol. 9, No. 11. - P. 1649-1661.

J79. Jinsoo Han. Remote-controllable and energy-saving room architecture based on ZigBee communication. / Jinsoo Han, Haeryong Lee, Kwang-Roh Park. // IEEE Transactions on Consumer Electronics. - 2009. - Vol. 55, No. 1. - P. 264-268.

J80. Sasaki H. Energy-Efficient Dynamic Instruction Scheduling Logic Through Instruction Grouping. / Sasaki H., Kondo M., Nakamura H. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2009. - Vol. 17, No. 6. - P. 848-852.

J81. Azevedo I.L. The Transition to Solid-State Lighting. / Azevedo I.L., Morgan M.G., Morgan F. // Proceedings of the IEEE. - 2009. - Vol. 97, No. 3. - P. 481-510.

J82. Yong He. A Novel Scheduled Power Saving Mechanism for 802.11 Wireless LANs. / Yong He, Ruixi Yuan. // IEEE Transactions on Mobile Computing. - 2009. - Vol. 8, No. 10. - P. 1368-1383.

J83. Ye Li. Energy-Efficient Video Transmission Over a Wireless Link. / Ye Li, Reisslein M., Chakrabarti C. // IEEE Transactions on Vehicular Technology. - 2009. - Vol. 58, No. 3. - P. 1229-1244.

J84. Rui Zhang. Joint Beamforming and Power Control for Multiantenna Relay Broadcast Channel With QoS Constraints. / Rui Zhang, Chin Choy Chai, Ying-Chang Liang. // IEEE Transactions on Signal Processing. - 2009. - Vol. 57, No. 2. - P. 726-737.

J85. Khargharia B. An Adaptive Interleaving Technique for Memory Performance-per-Watt Management. / Khargharia B., Hariri S., Yousif M.S. // IEEE Transactions on Parallel and Distributed Systems. - 2009. - Vol. 20, No. 7. - P. 1011-1022.

J86. Bwo-Ren Ke. Block-Layout Design Using MAX-MIN Ant System for Saving Energy on Mass Rapid

Transit Systems. / Bwo-Ren Ke, Meng-Chieh Chen, Chun-Liang Lin. // IEEE Transactions on Intelligent Transportation Systems. - 2009. - Vol. 10, No. 2. - P. 226-235.

J87. Tolentino M.E. Memory MISER: Improving Main Memory Energy Efficiency in Servers. / Tolentino M.E., Turner J., Cameron K.W. // IEEE Transactions on Computers. - 2009. - Vol. 58, No. 3. - P. 336-350.

J88. Tuan-Che Chen. Extended maximizing unavailability interval (eMUI): maximizing energy saving in IEEE 802.16e for mixing type I and type II PSCs. / Tuan-Che Chen, Jyh-Cheng Chen. // IEEE Communications Letters. - 2009. - Vol. 13, No. 2. - P. 151-153.

J89. Yong Ding. An Adaptive Partitioning Scheme for Sleep Scheduling and Topology Control in Wireless Sensor Networks. / Yong Ding, Chen Wang, Li Xiao. // IEEE Transactions on Parallel and Distributed Systems. - 2009. - Vol. 20, No. 9. - P. 1352-1365.

J90. Abbey C. A Stochastic Optimization Approach to Rating of Energy Storage Systems in Wind-Diesel Isolated Grids. / Abbey C., Joos G. // IEEE Transactions on Power Systems. - 2009. - Vol. 24, No. 1. - P. 418-426.

J91. Molina M.C. Frequent-Pattern-Guided Multilevel Decomposition of Behavioral Specifications. / Molina M.C., Ruiz-Sautua R., Garcia-Repetto P., Hermida R. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2009. - Vol. 28, No. 1. - P. 60-73.

J92. Chih-Chi Cheng. iVisual: An Intelligent Visual Sensor SoC With 2790 fps CMOS Image Sensor and 205 GOPS/W Vision Processor. / Chih-Chi Cheng, Chia-Hua Lin, Chung-Te Li, Liang-Gee Chen. // IEEE Journal of Solid-State Circuits. - 2009. - Vol. 44, No. 1. - P. 127-135.

J93. Shuenn-Yuh Lee. Systematic Design and Modeling of a OTA-C Filter for Portable ECG Detection. / Shuenn-Yuh Lee, Chih-Jen Cheng. // IEEE Transactions on Biomedical Circuits and Systems. - 2009. - Vol. 3, No. 1. - P. 53-64.

J94. Gordon-Ross A. Fast Configurable-Cache Tuning With a Unified Second-Level Cache. / Gordon-Ross A., Vahid F., Dutt N.D. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2009. - Vol. 17, No. 1. - P. 80-91.

J95. Yan Zhang. Energy Management Analysis and Enhancement in IEEE 802.16e WirelessMAN. / Yan Zhang, Yang Xiao, Leung V.C.M. // IEEE Transactions on Vehicular Technology. - 2009. - Vol. 58, No. 7. - P. 3738-3752.

J96. Sunho Lim. RandomCast: An Energy-Efficient Communication Scheme for Mobile Ad Hoc Networks. / Sunho Lim, Chansu Yu, Das C.R. // IEEE Transactions on Mobile Computing. - 2009. - Vol. 8, No. 8. - P. 1039-1051.

J97. Onel T. Information Content-Based Sensor Selection and Transmission Power Adjustment for Collaborative Target Tracking. / Onel T., Ersoy C., Delic H. // IEEE Transactions on Mobile Computing. - 2009. - Vol. 8, No. 8. - P. 1103-1116.

J98. Czaplewski D.A. Nanomechanical switches for power saving in CMOS applications. / Czaplewski D.A., Kraus G.M., Nordquist C.D. // Electronics Letters. - 2009. - Vol. 45, No. 11. - P. 550-551.

J99. Lee M. Intelligent power management device with middleware based living pattern learning for power reduction. / Lee M., Uhm Y., Kim Y., Kim G., Park S. // IEEE Transactions on Consumer Electronics. - 2009. - Vol. 55, No. 4. - P. 2081-2089.

J100. Lei Kong. Performance study and system optimization on sleep mode operation in IEEE 802.16e. / Lei Kong, Wong G., Tsang D. // IEEE Transactions on Wireless Communications. - 2009. - Vol. 8, No. 9. - P. 4518-4528.

J101. Lopez-Gomez M.A. A lightweight and energy-efficient architecture for wireless sensor networks. / Lopez-Gomez M.A., Tejero-Calado J.C. // IEEE Transactions on Consumer Electronics. - 2009. - Vol. 55, No. 3. - P. 1408-1416.

J102. Finchelstein D.F. Multicore Processing and Efficient On-Chip Caching for H.264 and Future Video

Decoders. / Finchelstein D.F., Sze V., Chandrakasan A.P. // IEEE Transactions on Circuits and Systems for Video Technology. - 2009. - Vol. 19, No. 11. - P. 1704-1713.

J103. Ya-Chun Lai. Resilient Self-V -Tuning Scheme With Speed-Margining for Low-Power SRAM. / Ya-Chun Lai, Shi-Yu Huang, Hsuan-Jung Hsu. // IEEE Journal of Solid-State Circuits. - 2009. - Vol. 44, No. 10. - P. 2817-2823.

J104. Seung-Ku Kim. Tiny module-linking for energy-efficient reprogramming in wireless sensor networks. / Seung-Ku Kim, Jae-Ho Lee, Kyeong Hur, Kwang-il Hwang, Doo-Seop Eom. // IEEE Transactions on Consumer Electronics. - 2009. - Vol. 55, No. 4. - P. 1914-1920.

J105. Kim J. Exploiting flash memory for reducing disk power consumption in portable media players. / Kim J., Yang A., Song M. // IEEE Transactions on Consumer Electronics. - 2009. - Vol. 55, No. 4. - P. 1997-2004.

J106. Rodriguez M.G. TelecomI+D09: Dynamic management of ICT service infrastructures for energy efficiency optimization. / Rodriguez M.G., Ferrera D.P., de la Iglesia Medina F., Mateos E.J.T. // IEEE (Revista IEEE America Latina) Latin America Transactions. - 2009. - Vol. 7, No. 3. - P. 429-434.

J107. Chouhan S. Integrated energy analysis of error correcting codes and modulation for energy efficient wireless sensor nodes. / Chouhan S., Bose R., Balakrishnan M. // IEEE Transactions on Wireless Communications. - 2009. - Vol. 8, No. 10. - P. 5348-5355.

J108. Chu E.T.-H. An Optimal Solution for the Heterogeneous Multiprocessor Single-Level Voltage-Setup Problem. / Chu E.T.-H., Tai-Yi Huang, Yu-Che Tsai. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2009. - Vol. 28, No. 11. - P. 1705-1718.

J109. Jahinuzzaman S.M. Design and Analysis of A 5.3-pJ 64-kb Gated Ground SRAM With Multiword ECC. / Jahinuzzaman S.M., Shah J.S., Rennie D.J., Sachdev M. // IEEE Journal of Solid-State Circuits. - 2009. - Vol. 44, No. 9. - P. 2543-2553.

J110. Thonnart Y. Power Reduction of Asynchronous Logic Circuits Using Activity Detection. / Thonnart Y., Beigne E., Valentian A., Vivet P. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2009. - Vol. 17, No. 7. - P. 893-906.

J111. Hyunsuk Cho. A backlight dimming algorithm for low power and high image quality LCD applications. / Hyunsuk Cho, Oh-Kyong Kwon. // IEEE Transactions on Consumer Electronics. - 2009. - Vol. 55, No. 2. - P. 839-844.

J112. Arm C. Low-Power 32-bit Dual-MAC 120 W/MHz 1.0 V icyflex1 DSP/MCU Core. / Arm C., Gyger S., Masgonty J.-M., Morgan M., Nagel J.-L., Piguet C., Rampogna F., Volet P. // IEEE Journal of Solid-State Circuits. - 2009. - Vol. 44, No. 7. - P. 2055-2064.

J113. Kuo-Chang Ting. An idle listening-aware energy efficient scheme for the DCF of 802.11n. / Kuo-Chang Ting, Hung-Chang Lee, Hsiu-Hui Lee, Feipei Lai. // IEEE Transactions on Consumer Electronics. - 2009. - Vol. 55, No. 2. - P. 447-454.

J114. Kyung-Hoae Koo. Compact Performance Models and Comparisons for Gigascale On-Chip Global Interconnect Technologies. / Kyung-Hoae Koo, Kapur P., Saraswat K.C. // IEEE Transactions on Electron Devices. - 2009. - Vol. 56, No. 9. - P. 1787-1798.

J115. Sung-Yong Bang. Run-Time Adaptive Workload Estimation for Dynamic Voltage Scaling. / Sung-Yong Bang, Kwanhu Bang, Sungroh Yoon, Eui-Young Chung. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2009. - Vol. 28, No. 9. - P. 1334-1347.

J116. Leverich J. Power Management of Datacenter Workloads Using Per-Core Power Gating. / Leverich J., Monchiero M., Talwar V., Ranganathan P., Kozyrakis C. // Computer Architecture Letters. - 2009. - Vol. 8, No. 2. - P. 48-51.

J117. Fan Zhu. Delay analysis for sleep-based power saving mechanisms with downlink and uplink traffic. / Fan Zhu, Yiqun Wu, Zhisheng Niu. // IEEE Communications Letters. - 2009. - Vol. 13, No. 8. - P. 615-617.

J118. Casson A.J. Toward Online Data Reduction for Portable Electroencephalography Systems in Epilepsy. /

Casson A.J., Rodriguez-Villegas E. // IEEE Transactions on Biomedical Engineering. - 2009. - Vol. 56, No. 12. - P. 2816-2825.

J119. Zhihai He. Energy Minimization of Portable Video Communication Devices Based on Power-Rate-Distortion Optimization. / Zhihai He, Wenye Cheng, Xi Chen. // IEEE Transactions on Circuits and Systems for Video Technology. - 2008. - Vol. 18, No. 5. - P. 596-608.

J120. Keejong Kim. A Low-Power SRAM Using Bit-Line Charge-Recycling. / Keejong Kim, Mahmoodi H., Roy K. // IEEE Journal of Solid-State Circuits. - 2008. - Vol. 43, No. 2. - P. 446-459.

J121. Tao Xie. SEA: A Striping-Based Energy-Aware Strategy for Data Placement in RAID-Structured Storage Systems. IEEE Transactions on Computers. - 2008. - Vol. 57, No. 6. - P. 748-761.

J122. Chua-Chin Wang. A Mini-Invasive Long-Term Bladder Urine Pressure Measurement ASIC and System. / Chua-Chin Wang, Chi-Chun Huang, Jian-Sing Liou, Yan-Jhin Ciou, I-Yu Huang, Chih-Peng Li, Yung-Chin Lee, Weng-Jeng Wu. // IEEE Transactions on Biomedical Circuits and Systems. - 2008. - Vol. 2, No. 1. - P. 44-49.

J123. Sasaki T. Evaluation of low-energy and high-performance processor using variable stages pipeline technique. / Sasaki T., Ichikawa Y., Hironaka T., Kitamura T., Kondo T. // IET Computers & Digital Techniques. - 2008. - Vol. 2, No. 3. - P. 230-238.

J124. Kodi A.K. Adaptive Channel Buffers in On-Chip Interconnection Networks— A Power and Performance Analysis. / Kodi A.K., Sarathy A., Louri A. // IEEE Transactions on Computers. - 2008. - Vol. 57, No. 9. - P. 1169-1181.

J125. Joon Heo. Design and Implementation of Control Mechanism for Standby Power Reduction. / Joon Heo, Choong Seon Hong, Seok Bong Kang, Sang Soo Jeon. // IEEE Transactions on Consumer Electronics. - 2008. - Vol. 54, No. 1. - P. 179-185.

J126. Evans B.D. Test Results for Energy Savings. / Evans B.D., Crissman J., Gobert J. // IEEE Industry Applications Magazine. - 2008. - Vol. 14, No. 1. - P. 44-49.

J127. Lotfinezhad M. Adaptive Cluster-Based Data Collection in Sensor Networks with Direct Sink Access. / Lotfinezhad M., Ben Liang, Sousa E.S. // IEEE Transactions on Mobile Computing. - 2008. - Vol. 7, No. 7. - P. 884-897.

J128. Yong-Sheng Yan. An Efficient Motion-Resistant Method for Wearable Pulse Oximeter. / Yong-Sheng Yan, Yuan-Ting Zhang. // IEEE Transactions on Information Technology in Biomedicine. - 2008. - Vol. 12, No. 3. - P. 399-405.

J129. Shah A.J. Optimization of Global Data Center Thermal Management Workload for Minimal Environmental and Economic Burden. / Shah A.J., Krishnan N. // IEEE Transactions on Components and Packaging Technologies. - 2008. - Vol. 31, No. 1. - P. 39-45.

J130. Xiaotao Liu. Chameleon: Application-Level Power Management. / Xiaotao Liu, Shenoy P., Corner M.D. // IEEE Transactions on Mobile Computing. - 2008. - Vol. 7, No. 8. - P. 995-1010.

J131. Gunaratne C. Reducing the Energy Consumption of Ethernet with Adaptive Link Rate (ALR). / Gunaratne C., Christensen K., Nordman B., Suen S. // IEEE Transactions on Computers. - 2008. - Vol. 57, No. 4. - P. 448-461.

J132. Jun-Young Lee. Picture-Based Address Power Saving Method for High Resolution Plasma Display Panel (PDP). IEEE Transactions on Industrial Electronics. - 2008. - Vol. 55, No. 1. - P. 49-58.

J133. Goth G. The Net's Going Green: Multipronged Approach Might Save Costs, Energy — and the Climate. IEEE Internet Computing. - 2008. - Vol. 12, No. 1. - P. 7-9.

J134. Sheng-Yu Tseng. Wide Pulse Combined With Narrow-Pulse Generator for Food Sterilization. / Sheng-Yu Tseng, Tsai-Fu Wu, Yaow-Ming Chen. // IEEE Transactions on Industrial Electronics. - 2008. - Vol. 55, No. 2. - P. 741-748.

J135. Curtis-Maury M. Prediction-Based Power-Performance Adaptation of Multithreaded Scientific Codes. /

Curtis-Maury M., Blagojevic F., Antonopoulos C.D., Nikolopoulos D.S. // IEEE Transactions on Parallel and Distributed Systems. - 2008. - Vol. 19, No. 10. - P. 1396-1410.

J136. Jian-Wei Zhang. A Current-Recycling Technique for Shadow-Match-Line Sensing in Content-Addressable Memories. / Jian-Wei Zhang, Yi-Zheng Ye, Bin-Da Liu. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2008. - Vol. 16, No. 6. - P. 677-682.

J137. Varatkar G.V. Error-Resilient Motion Estimation Architecture. / Varatkar G.V., Shanbhag N.R. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2008. - Vol. 16, No. 10. - P. 1399-1412.

J138. Tuan-Che Chen. An efficient energy saving mechanism for IEEE 802.16e wireless MANs. / Tuan-Che Chen, Ying-Yu Chen, Jyh-Cheng Chen. // IEEE Transactions on Wireless Communications. - 2008. - Vol. 7, No. 10. - P. 3708-3712.

J139. Tyshchenko O. Match Sensing Using Match-Line Stability in Content-Addressable Memories (CAM). / Tyshchenko O., Sheikholeslami A. // IEEE Journal of Solid-State Circuits. - 2008. - Vol. 43, No. 9. - P. 1972-1981.

J140. Dabiri F. General Methodology for Soft-Error-Aware Power Optimization Using Gate Sizing. / Dabiri F., Nahapetian A., Massey T., Potkonjak M., Sarrafzadeh M. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2008. - Vol. 27, No. 10. - P. 1788-1797.

J141. Min-Gon Kim. Scheduled power-saving mechanism to minimize energy consumption in IEEE 802.16e systems. / Min-Gon Kim, Jungyul Choi, Minho Kang. // IEEE Communications Letters. - 2008. - Vol. 12, No. 12. - P. 874-876.

J142. Villar J.R. IWPAAMS2007-05: Energy Saving By Means Of Multiagent Systems And Fuzzy Systems. / Villar J.R., Cal E., Sedano J. // IEEE (Revista IEEE America Latina) Latin America Transactions. - 2008. - Vol. 6, No. 6. - P. 517-523.

J143. Yim R. Progressive Accumulative Routing: Fundamental Concepts and Protocol. / Yim R., Mehta N., Molisch A., Jinyun Zhang. // IEEE Transactions on Wireless Communications. - 2008. - Vol. 7, No. 11. - P. 4142-4154.

J144. Jaedoo Go. Adaptive disk power management for portable media players. / Jaedoo Go, Minseok Song. // IEEE Transactions on Consumer Electronics. - 2008. - Vol. 54, No. 4. - P. 1755-1760.

J145. SungWon Chung. Energy-Efficient Digital Predistortion With Lookup Table Training Using Analog Cartesian Feedback. / SungWon Chung, Holloway J.W., Dawson J.L. // IEEE Transactions on Microwave Theory and Techniques. - 2008. - Vol. 56, No. 10. - P. 2248-2258.

J146. Euiseong Seo. Energy Efficient Scheduling of Real-Time Tasks on Multicore Processors. / Euiseong Seo, Jinkyu Jeong, Seonyeong Park, Joonwon Lee. // IEEE Transactions on Parallel and Distributed Systems. - 2008. - Vol. 19, No. 11. - P. 1540-1552.

J147. Chih-Chang Lai. Backlight power reduction and image contrast enhancement using adaptive dimming for global backlight applications. / Chih-Chang Lai, Ching-Chih Tsai. // IEEE Transactions on Consumer Electronics. - 2008. - Vol. 54, No. 2. - P. 669-674.

J148. Marcelloni F. A Simple Algorithm for Data Compression in Wireless Sensor Networks. / Marcelloni F., Vecchio M. // IEEE Communications Letters. - 2008. - Vol. 12, No. 6. - P. 411-413.

J149. Ahmed I. A High Bandwidth Power Scalable Sub-Sampling 10-Bit Pipelined ADC With Embedded Sample and Hold. / Ahmed I., Johns D.A. // IEEE Journal of Solid-State Circuits. - 2008. - Vol. 43, No. 7. - P. 1638-1647.

J150. Lin Zhang. Injection-Locked Clocking: A Low-Power Clock Distribution Scheme for High-Performance Microprocessors. / Lin Zhang, Carpenter A., Ciftcioglu B., Garg A., Huang M., Hui Wu. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2008. - Vol. 16, No. 9. - P. 1251-1256.

J151. Flynn M.M. Saving energy using flywheels. / Flynn M.M., Mcmullen P., Solis O. // IEEE Industry Applications Magazine. - 2008. - Vol. 14, No. 6. - P. 69-76.

J152. Jae Eun Jang. A Nanogripper Employing Aligned Multiwall Carbon Nanotubes. / Jae Eun Jang, Seung Nam Cha, Youngjin Choi, Dae Joon Kang, Hasko D.G., Jae Eun Jung, Jong Min Kim, Amaratunga G.A.J. // IEEE Transactions on Nanotechnology. - 2008. - Vol. 7, No. 4. - P. 389-393.

J153. Elyada A. Low-Complexity Policies for Energy-Performance Tradeoff in Chip-Multi-Processors. / Elyada A., Ginosar R., Weiser U. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2008. - Vol. 16, No. 9. - P. 1243-1248.

J154. Tung-Chien Chen. Fast Algorithm and Architecture Design of Low-Power Integer Motion Estimation for H.264/AVC. / Tung-Chien Chen, Yu-Han Chen, Sung-Fang Tsai, Shao-Yi Chien, Liang-Gee Chen. // IEEE Transactions on Circuits and Systems for Video Technology. - 2007. - Vol. 17, No. 5. - P. 568-577.

J155. Freeh V.W. Analyzing the Energy-Time Trade-Off in High-Performance Computing Applications. / Freeh V.W., Lowenthal D.K., Pan F., Kappiah N., Springer R., Rountree B.L., Femal M.E. // IEEE Transactions on Parallel and Distributed Systems. - 2007. - Vol. 18, No. 6. - P. 835-848.

J156. Yuke Wang. Novel Memory Reference Reduction Methods for FFT Implementations on DSP Processors. / Yuke Wang, Yiyan Tang, Yingtao Jiang, Jin-Gyun Chung, Sang-Seob Song, Myoung-Seob Lim. // IEEE Transactions on Signal Processing. - 2007. - Vol. 55, No. 5. - P. 2338-2349.

J157. Jian Ma. Energy-Efficient Localized Topology Control Algorithms in IEEE 802.15.4-Based Sensor Networks. / Jian Ma, Min Gao, Qian Zhang, Ni L.M. // IEEE Transactions on Parallel and Distributed Systems. - 2007. - Vol. 18, No. 5. - P. 711-720.

J158. Hyun-Ho Choi. Hybrid Power Saving Mechanism for VoIP Services with Silence Suppression in IEEE 802.16e Systems. / Hyun-Ho Choi, Jung-Ryun Lee, Dong-Ho Cho. // IEEE Communications Letters. - 2007. - Vol. 11, No. 5. - P. 455-457.

J159. Jun Cheng Chi. Gate Level Multiple Supply Voltage Assignment Algorithm for Power Optimization Under Timing Constraint. / Jun Cheng Chi, Hung Hsie Lee, Sung Han Tsai, Mely Chen Chi. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2007. - Vol. 15, No. 6. - P. 637-648.

J160. Dinh Thi Thuy Nga. Delay-guaranteed Energy Saving Algorithm for the Delay-sensitive Applications in IEEE 802.16e Systems. / Dinh Thi Thuy Nga, Min-Gon Kim, Minho Kang. // IEEE Transactions on Consumer Electronics. - 2007. - Vol. 53, No. 4. - P. 1339-1347.

J161. Xiaoan Lu. Total Power Minimization for Multiuser Video Communications Over CDMA Networks. / Xiaoan Lu, Yao Wang, Erkip E., Goodman D.J. // IEEE Transactions on Circuits and Systems for Video Technology. - 2007. - Vol. 17, No. 6. - P. 674-685.

J162. Yong Ho Moon. A New Coeff-Token Decoding Method With Efficient Memory Access in H.264/AVC Video Coding Standard. IEEE Transactions on Circuits and Systems for Video Technology. - 2007. - Vol. 17, No. 6. - P. 729-736.

J163. Kadayif I. Reducing Data TLB Power via Compiler-Directed Address Generation. / Kadayif I., Nath P., Kandemir M., Sivasubramaniam A. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2007. - Vol. 26, No. 2. - P. 312-324.

J164. Jason Ridenour. Low-Power Buffer Management for Streaming Data. / Jason Ridenour, Jianghai Hu, Nathaniel Pettis, Yung-Hsing Lu. // IEEE Transactions on Circuits and Systems for Video Technology. - 2007. - Vol. 17, No. 2. - P. 143-157.

J165. Xiaolei Shi. SyncWUF: An Ultra Low-Power MAC Protocol for Wireless Sensor Networks. / Xiaolei Shi, Stromberg G. // IEEE Transactions on Mobile Computing. - 2007. - Vol. 6, No. 1. - P. 115-125.

J166. Catalin Drula. Adaptive energy conserving algorithms for neighbor discovery in opportunistic Bluetooth networks. / Catalin Drula, Cristiana Amza, Franck Rousseau, Andrzej Duda. // IEEE Journal on Selected Areas in Communications. - 2007. - Vol. 25, No. 1. - P. 96-107.

J167. W. Pam Siriwongpairat. Power controlled channel allocation for multiuser multiband UWB systems. / W. Pam Siriwongpairat, Zhu Han, K. J. Ray Liu. // IEEE Transactions on Wireless Communications. - 2007. - Vol. 6, No. 2. - P. 583-592.

J168. Tong Zhao. Distributed Sequential Bayesian Estimation of a Diffusive Source in Wireless Sensor Networks. / Tong Zhao, Nehorai A. // IEEE Transactions on Signal Processing. - 2007. - Vol. 55, No. 4. - P. 1511-1524.

J169. Aly R.E. Low-Power Cache Design Using 7T SRAM Cell. / Aly R.E., Bayoumi M.A. // IEEE Transactions on Circuits and Systems II: Express Briefs. - 2007. - Vol. 54, No. 4. - P. 318-322.

J170. Chih-Cheng Tseng. Organizing an optimal cluster-based ad hoc network architecture by the modified Quine-McCluskey algorithm. / Chih-Cheng Tseng, Kwang-Cheng Chen. // IEEE Communications Letters. - 2007. - Vol. 11, No. 1. - P. 43-45.

J171. Kyungtae Kang. Energy-Efficient MAC-Layer Error Recovery for Mobile Multimedia Applications in 3GPP2 BCMCS. / Kyungtae Kang, Yongwoo Cho, Heonshik Shin. // IEEE Transactions on Broadcasting. - 2007. - Vol. 53, No. 1. - P. 338-349.

J172. Khandelwal V. Leakage Control Through Fine-Grained Placement and Sizing of Sleep Transistors. / Khandelwal V., Srivastava A. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2007. - Vol. 26, No. 7. - P. 1246-1255.

J173. Singh H. Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating. / Singh H., Agarwal K., Sylvester D., Nowka K.J. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2007. - Vol. 15, No. 11. - P. 1215-1224.

J174. Huayong Yang. New Investigation in Energy Regeneration of Hydraulic Elevators. / Huayong Yang, Wei Sun, Bing Xu. // IEEE/ASME Transactions on Mechatronics. - 2007. - Vol. 12, No. 5. - P. 519-526.

J175. Fan-Min Li. On the New Stopping Criteria of Iterative Turbo Decoding by Using Decoding Threshold. / Fan-Min Li, An-Yeu Wu. // IEEE Transactions on Signal Processing. - 2007. - Vol. 55, No. 11. - P. 5506-5516.

J176. Niyato D. Wireless sensor networks with energy harvesting technologies: a game-theoretic approach to optimal energy management. / Niyato D., Hossain E., Rashid M.M., Bhargava V.K. // IEEE Wireless Communications. - 2007. - Vol. 14, No. 4. - P. 90-96.

J177. Shun-Ren Yang. Modeling UMTS Power Saving with Bursty Packet Data Traffic. / Shun-Ren Yang, Sheng-Ying Yan, Hui-Nien Hung. // IEEE Transactions on Mobile Computing. - 2007. - Vol. 6, No. 12. - P. 1398-1409.

J178. Fei Sun. Quasi-Reduced-State Soft-Output Viterbi Detector for Magnetic Recording Read Channel. / Fei Sun, Tong Zhang. // IEEE Transactions on Magnetics. - 2007. - Vol. 43, No. 10. - P. 3921-3924.

J179. Jie Lian. Gradient Boundary Detection for Time Series Snapshot Construction in Sensor Networks. / Jie Lian, Lei Chen, Naik K., Yunhao Liu, Agnew G.B. // IEEE Transactions on Parallel and Distributed Systems. - 2007. - Vol. 18, No. 10. - P. 1462-1475.

J180. Ramo E.P. Memory hierarchy for high-performance and energyaware reconfigurable systems. / Ramo E.P., Resano J., Mozos D., Catthoor F. // IET Computers & Digital Techniques. - 2007. - Vol. 1, No. 5. - P. 565-571.

J181. Chung-Ho Chen. Scalable Dynamic Instruction Scheduler through Wake-Up Spatial Locality. / Chung-Ho Chen, Kuo-Su Hsiao. // IEEE Transactions on Computers. - 2007. - Vol. 56, No. 11. - P. 1534-1548.

J182. AbouGhazaleh N. Near-Memory Caching for Improved Energy Consumption. / AbouGhazaleh N., Childers B.R., Mosse D., Melhem R.G. // IEEE Transactions on Computers. - 2007. - Vol. 56, No. 11. - P. 1441-1455.

J183. Farbod A. Resource Allocation and Outage Control for Solar-Powered WLAN Mesh Networks. / Farbod A., Todd T.D. // IEEE Transactions on Mobile Computing. - 2007. - Vol. 6, No. 8. - P. 960-970.

J184. Safdar G.A. Improved power-saving medium-access protocol for IEEE 802.11e QoS-enabled wireless networks. / Safdar G.A., Scanlon W.G. // IET Communications. - 2007. - Vol. 1, No. 4. - P. 718-725.

J185. Ka-Ming Keung. A Novel Charge Recycling Design Scheme Based on Adiabatic Charge Pump. / Ka-Ming Keung, Manne V., Tyagi A. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2007. - Vol. 15, No. 7. - P. 733-745.

J186. Cho Y. Energy-Aware Clock-Frequency Assignment in Microprocessors and Memory Devices for Dynamic Voltage Scaling. / Cho Y., Chang N. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2007. - Vol. 26, No. 6. - P. 1030-1040.

J187. Azizi N. Variations-Aware Low-Power Design and Block Clustering With Voltage Scaling. / Azizi N., Khellah M.M., De V.K., Najm F.N. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2007. - Vol. 15, No. 7. - P. 746-757.

J188. Zhiyu Liu. PMOS-Only Sleep Switch Dual-Threshold Voltage Domino Logic in Sub-65-nm CMOS Technologies. / Zhiyu Liu, Kursun V. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2007. - Vol. 15, No. 12. - P. 1311-1319.

J189. Won-Jun Choe. A Single-Pair Serial Link for Mobile Displays With Clock Edge Modulation Scheme. / Won-Jun Choe, Bong-Joon Lee, Jaeha Kim, Deog-Kyoon Jeong, Gyudong Kim. // IEEE Journal of Solid-State Circuits. - 2007. - Vol. 42, No. 9. - P. 2012-2020.

J190. Seung Woo Son. Compiler-Directed Energy Optimization for Parallel Disk Based Systems. / Seung Woo Son, Guangyu Chen, Ozturk O., Kandemir M., Choudhary A. // IEEE Transactions on Parallel and Distributed Systems. - 2007. - Vol. 18, No. 9. - P. 1241-1257.

J191. Yu-Kuang Tu. Efficient rate-distortion estimation for H.264/AVC coders. / Yu-Kuang Tu, Jar-Ferr Yang, Ming-Ting Sun. // IEEE Transactions on Circuits and Systems for Video Technology. - 2006. - Vol. 16, No. 5. - P. 600-611.

J192. Daji Qiao. New 802.11h mechanisms can reduce power consumption. / Daji Qiao, Sunghyun Choi. // IT Professional. - 2006. - Vol. 8, No. 2. - P. 43-48.

J193. Ching-Yeh Chen. Level C+ data reuse scheme for motion estimation with corresponding coding orders. / Ching-Yeh Chen, Chao-Tsung Huang, Yi-Hau Chen, Liang-Gee Chen. // IEEE Transactions on Circuits and Systems for Video Technology. - 2006. - Vol. 16, No. 4. - P. 553-558.

J194. Wei Yu. Efficient rate control for JPEG-2000. / Wei Yu, Fangting Sun, Fritts J.E. // IEEE Transactions on Circuits and Systems for Video Technology. - 2006. - Vol. 16, No. 5. - P. 577-589.

J195. Gniady C. Program counter-based prediction techniques for dynamic power management. / Gniady C., Butt A.R., Hu Y.C., Yung-Hsiang Lu. // IEEE Transactions on Computers. - 2006. - Vol. 55, No. 6. - P. 641-658.

J196. Ejlali A. Combined time and information redundancy for SEU-tolerance in energy-efficient real-time systems. / Ejlali A., Al-Hashimi B.M., Schmitz M.T., Rosinger P., Miremadi S.G. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2006. - Vol. 14, No. 4. - P. 323-335.

J197. Byung-Do Yang. A low-power ROM using single charge-sharing capacitor and hierarchical bit line. / Byung-Do Yang, Lee-Sup Kim. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2006. - Vol. 14, No. 4. - P. 313-322.

J198. Frosini L. Linear and neural dynamic models: shared benefits between the industrial customer and the ESCo from the energy services' perspective. / Frosini L., Anglani N. // IEEE Transactions on Systems, Man, and Cybernetics, Part C: Applications and Reviews. - 2006. - Vol. 36, No. 4. - P. 524-529.

J199. Yiqiang Chen. Power-efficient access-point selection for indoor location estimation. / Yiqiang Chen, Qiang Yang, Jie Yin, Xiaoyong Chai. // IEEE Transactions on Knowledge and Data Engineering. - 2006. - Vol. 18, No. 7. - P. 877-888.

J200. Chih-Min Chao. An adaptive quorum-based energy conserving protocol for IEEE 802.11 ad hoc networks. / Chih-Min Chao, Jang-Ping Sheu, I-Cheng Chou. // IEEE Transactions on Mobile Computing. - 2006. - Vol. 5, No. 5. - P. 560-570.

J201. Calhoun B.H. Ultra-dynamic Voltage scaling (UDVS) using sub-threshold operation and local Voltage

dithering. / Calhoun B.H., Chandrakasan A.P. // IEEE Journal of Solid-State Circuits. - 2006. - Vol. 41, No. 1. - P. 238-245.

J202. Ponomarev D. Dynamic resizing of superscalar datapath components for energy efficiency. / Ponomarev D., Kucuk G., Ghose K. // IEEE Transactions on Computers. - 2006. - Vol. 55, No. 2. - P. 199-213.

J203. Chakraborty S. On the effectiveness of movement prediction to reduce energy consumption in wireless communication. / Chakraborty S., Yu Dong, Yau D.K.Y., Lui J.C.S. // IEEE Transactions on Mobile Computing. - 2006. - Vol. 5, No. 2. - P. 157-169.

J204. Ying Zhang. A unified approach for fault tolerance and dynamic power management in fixed-priority real-time embedded systems. / Ying Zhang, Chakrabarty K. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2006. - Vol. 25, No. 1. - P. 111-125.

J205. Lyuh C.-G. Memory access scheduling and binding considering energy minimisation in multi-bank memory systems: integrated approach. / Lyuh C.-G., Kim T. // IEE Proceedings - Computers and Digital Techniques. - 2006. - Vol. 153, No. 1. - P. 59-68.

J206. Choi J. Memory-aware dynamic voltage scaling for multimedia applications. / Choi J., Cha H. // IEE Proceedings - Computers and Digital Techniques. - 2006. - Vol. 153, No. 2. - P. 130-136.

J207. Narula H.S. A time-based VLSI potentiostat for ion current measurements. / Narula H.S., Harris J.G. // IEEE Sensors Journal. - 2006. - Vol. 6, No. 2. - P. 239-247.

J208. Dongkun Shin. Dynamic voltage scaling of mixed task sets in priority-driven systems. / Dongkun Shin, Jihong Kim. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2006. - Vol. 25, No. 3. - P. 438-453.

J209. Kalla P. Distance-based recent use (DRU): an enhancement to instruction cache replacement policies for transition energy reduction. / Kalla P., Xiaobo Sharon Hu, Henkel J. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2006. - Vol. 14, No. 1. - P. 69-80.

J210. Lodi A. Low leakage techniques for FPGAs. / Lodi A., Ciccarelli L., Guerrieri R. // IEEE Journal of Solid-State Circuits. - 2006. - Vol. 41, No. 7. - P. 1662-1672.

J211. Chang N.Y.-C. Combined Frame Memory Motion Compensation for Video Coding. / Chang N.Y.-C., Tian-Sheuan Chang. // IEEE Transactions on Circuits and Systems for Video Technology. - 2006. - Vol. 16, No. 10. - P. 1280-1285.

J212. Alioto M. Exploiting Hysteresys in MCML Circuits. / Alioto M., Pancioni L., Rocchi S., Vignoli V. // IEEE Transactions on Circuits and Systems II: Express Briefs. - 2006. - Vol. 53, No. 11. - P. 1170-1174.

J213. Safdar G.A. Performance analysis of an improved power-saving medium access protocol for IEEE 802.11 point coordination function WLAN. / Safdar G.A., Scanlon W.G. // IEE Proceedings- Communications. - 2006. - Vol. 153, No. 5. - P. 697-704.

J214. Kuo-Su Hsiao. Wake-Up Logic Optimizations Through Selective Match and Wakeup Range Limitation. / Kuo-Su Hsiao, Chung-Ho Chen. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2006. - Vol. 14, No. 10. - P. 1089-1102.

J215. Le Cai. Joint Power Management of Memory and Disk Under Performance Constraints. / Le Cai, Nathaniel Pettis, Yung-Hsiang Lu. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2006. - Vol. 25, No. 12. - P. 2697-2711.

J216. Knights M. The power black hole-The cost of power and the security of supply is a growing concern, but many data centre managers are neglecting this important issue.. Power Engineer. - 2006. - Vol. 20, No. 6. - P. 30-33.

J217. Cho Y. Energy-Aware Clock-Frequency Assignment in Microprocessors and Memory Devices for Dynamic Voltage Scaling. / Cho Y., Chang N. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2006. - Vol. 26, No. 6. - P. 1030-1040.

J218. Limniotis K. A Design Technique for Energy Reduction in NORA CMOS Logic. / Limniotis K., Tsiatouhas Y., Haniotakis T., Arapoyanni A. // IEEE Transactions on Circuits and Systems I: Regular Papers. - 2006. - Vol. 53, No. 12. - P. 2647-2655.

J219. Edwards C. Aviation-Less of a drag-Researchers may only need to look skin-deep to cut aircraft fuel. Engineering & Technology. - 2006. - Vol. 1, No. 9. - P. 42-45.

J220. Yan H. Client-Centered, Energy-Efficient Wireless Communication on IEEE 802.11b Networks. / Yan H., Watterson S.A., Lowenthal D.K., Li K., Krishnan R., Peterson L.L. // IEEE Transactions on Mobile Computing. - 2006. - Vol. 5, No. 11. - P. 1575-1590.

J221. Lee S.-W. Throttling-Based Resource Management in High Performance Multithreaded Architectures. / Lee S.-W., Gaudiot J.-L. // IEEE Transactions on Computers. - 2006. - Vol. 55, No. 9. - P. 1142-1152.

J222. De La Luz V. Reducing memory energy consumption of embedded applications that process dynamically allocated data. / De La Luz V., Kandemir M., Kolcu I. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2006. - Vol. 25, No. 9. - P. 1855-1860.

J223. Ozer E. Multiple-valued logic buses for reducing bus energy in low-power systems. / Ozer E., Sendag R., Gregg D. // IEE Proceedings - Computers and Digital Techniques. - 2006. - Vol. 153, No. 4. - P. 270-282.

J224. Boyer F.R. Embedded power-aware cycle by cycle variable speed processor. / Boyer F.R., Epassa H.G., Savaria Y. // IEE Proceedings - Computers and Digital Techniques. - 2006. - Vol. 153, No. 4. - P. 283-290.

J225. Sang-Min Kim. Control of Rubber Tyred Gantry Crane With Energy Storage Based on Supercapacitor Bank. / Sang-Min Kim, Seung-Ki Sul. // IEEE Transactions on Power Electronics. - 2006. - Vol. 21, No. 5. - P. 1420-1427.

J226. Yao Gang. An Efficient Pre-Traceback Architecture for the Viterbi Decoder Targeting Wireless Communication Applications. / Yao Gang, Erdogan A.T., Arslan T. // IEEE Transactions on Circuits and Systems I: Regular Papers. - 2006. - Vol. 53, No. 9. - P. 1918-1927.

J227. Zhiyu Liu. Leakage Power Characteristics of Dynamic Circuits in Nanometer CMOS Technologies. / Zhiyu Liu, Kursun V. // IEEE Transactions on Circuits and Systems II: Express Briefs. - 2006. - Vol. 53, No. 8. - P. 692-696.

J228. Kulkarni S. An address-light, integrated MAC and routing protocol for wireless sensor networks. / Kulkarni S., Iyer A., Rosenberg C. // IEEE/ACM Transactions on Networking. - 2006. - Vol. 14, No. 4. - P. 793-806.

J229. Zheng Ma. On the complexity reduction of turbo decoding for wideband CDMA. / Zheng Ma, Wai Ho Mow, Pingzhi Fan. // IEEE Transactions on Wireless Communications. - 2005. - Vol. 4, No. 2. - P. 353-356.

J230. Kadayif I. Optimizing array-intensive applications for on-chip multiprocessors. / Kadayif I., Kandemir M., Chen G., Ozturk O., Karakoy M., Sezer U. // IEEE Transactions on Parallel and Distributed Systems. - 2005. - Vol. 16, No. 5. - P. 396-411.

J231. Zhu Q. Power-aware storage cache management. / Zhu Q., Zhou Y. // IEEE Transactions on Computers. - 2005. - Vol. 54, No. 5. - P. 587-602.

J232. Hai Li. Combined circuit and architectural level variable supply-voltage scaling for low power. / Hai Li, Chen-Yong Cher, Roy K., Vijaykumar T.N. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2005. - Vol. 13, No. 5. - P. 564-576.

J233. Byung-Do Yang. A low-power SRAM using hierarchical bit line and local sense amplifiers. / Byung-Do Yang, Lee-Sup Kim. // IEEE Journal of Solid-State Circuits. - 2005. - Vol. 40, No. 6. - P. 1366-1376.

J234. Wen-Chih Peng. Query processing in a mobile computing environment: exploiting the features of asymmetry. / Wen-Chih Peng, Ming-Syan Chen. // IEEE Transactions on Knowledge and Data Engineering. - 2005. - Vol. 17, No. 7. - P. 982-996.

J235. Jinn-Shyan Wang. Design techniques for single-low-VDD CMOS systems. / Jinn-Shyan Wang, Hung-Yu

Li, Chingwei Yeh, Tien-Fu Chen. // IEEE Journal of Solid-State Circuits. - 2005. - Vol. 40, No. 5. - P. 1157-1165.

J236. Schmitz M.T. Cosynthesis of energy-efficient multimode embedded systems with consideration of mode-execution probabilities. / Schmitz M.T., Al-Hashimi B.M., Eles P. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2005. - Vol. 24, No. 2. - P. 153-169.

J237. Bougas P. Pipelined array-based FIR filter folding. / Bougas P., Kalivas P., Tsirikos A., Pekmestzi K.Z. // IEEE Transactions on Circuits and Systems I: Regular Papers. - 2005. - Vol. 52, No. 1. - P. 108-118.

J238. Talpes E. Execution cache-based microarchitecture for power-efficient superscalar processors. / Talpes E., Marculescu D. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2005. - Vol. 13, No. 1. - P. 14-26.

J239. Helmy A. Contact-extended zone-based transactions routing for energy-constrained wireless ad hoc networks. IEEE Transactions on Vehicular Technology. - 2005. - Vol. 54, No. 1. - P. 307-319.

J240. Chua-Chin Wang. A 2K/8K mode small-area FFT processor for OFDM demodulation of DVB-T receivers. / Chua-Chin Wang, Jian-Ming Huang, Hsian-Chang Cheng. // IEEE Transactions on Consumer Electronics. - 2005. - Vol. 51, No. 1. - P. 28-32.

J241. Muruganathan S.D. A centralized energy-efficient routing protocol for wireless sensor networks. / Muruganathan S.D., Ma D.C.F., Bhasin R.I., Fapojuwo A.O. // IEEE Communications Magazine. - 2005. - Vol. 43, No. 3. - P. S8-13.

J242. Zeng H. Experiences in managing energy with ECOSystem. / Zeng H., Ellis C.S., Lebeck A.R. // IEEE Pervasive Computing. - 2005. - Vol. 4, No. 1. - P. 62-68.

J243. Hao Zhu. On supporting power-efficient streaming applications in wireless environments. / Hao Zhu, Guohong Cao. // IEEE Transactions on Mobile Computing. - 2005. - Vol. 4, No. 4. - P. 391-403.

J244. Reinman G. Using an operand file to save energy and to decouple commit resources. IEE Proceedings - Computers and Digital Techniques. - 2005. - Vol. 152, No. 5. - P. 666-678.

J245. Diril A.U. Level-shifter free design of low power dual supply voltage CMOS circuits using dual threshold voltages. / Diril A.U., Dhillon Y.S., Chatterjee A., Singh A.D. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2005. - Vol. 13, No. 9. - P. 1103-1107.

J246. Kaps J.-P. Energy scalable universal hashing. / Kaps J.-P., Yuksel K., Sunar B. // IEEE Transactions on Computers. - 2005. - Vol. 54, No. 12. - P. 1484-1495.

J247. McIver J.K. III. Reducing radiation-hardened DigitalCircuit power consumption. / McIver J.K. III, Clark L.T. // IEEE Transactions on Nuclear Science. - 2005. - Vol. 52, No. 6. - P. 2503-2509.

J248. Rodrigues J.N. Digital implementation of a wavelet-based event detector for cardiac pacemakers. / Rodrigues J.N., Olsson T., Sornmo L., Owall V. // IEEE Transactions on Circuits and Systems I: Regular Papers. - 2005. - Vol. 52, No. 12. - P. 2686-2698.

J249. O'Donnell I.D. An ultra-wideband transceiver architecture for low power, low rate, wireless systems. / O'Donnell I.D., Brodersen R.W. // IEEE Transactions on Vehicular Technology. - 2005. - Vol. 54, No. 5. - P. 1623-1631.

J250. Park S. Quality-adaptive requantization for low-energy MPEG-4 video decoding in mobile devices. / Park S., Lee Y., Lee J., Shin H. // IEEE Transactions on Consumer Electronics. - 2005. - Vol. 51, No. 3. - P. 999-1005.

J251. Kim E.J. A holistic approach to designing energy-efficient cluster interconnects. / Kim E.J., Link G.M., Yum K.H., Vijaykrishnan N., Kandemir M., Irwin M.J., Das C.R. // IEEE Transactions on Computers. - 2005. - Vol. 54, No. 6. - P. 660-671.

J252. Algrain M.C. Efficient idle: on the electrification of class-8 trucks. IEEE Industry Applications Magazine. - 2005. - Vol. 11, No. 4. - P. 29-38.

J253. Chien-Ching Lin. Design of a power-reduction Viterbi decoder for WLAN applications. / Chien-Ching Lin, Yen-Hsu Shih, Hsie-Chia Chang, Chen-Yi Lee. // IEEE Transactions on Circuits and Systems I: Regular Papers. - 2005. - Vol. 52, No. 6. - P. 1148-1156.

J254. Calhoun B.H. Modeling and sizing for minimum energy operation in subthreshold circuits. / Calhoun B.H., Wang A., Chandrakasan A. // IEEE Journal of Solid-State Circuits. - 2005. - Vol. 40, No. 9. - P. 1778-1786.

J255. Wang C.-C. Low-Power Small-Area Digital I/O Cell. / Wang C.-C., Lee C.-L., Tseng Y.-L., Chen C.-S., Hu R. // IEEE Transactions on Circuits and Systems II: Express Briefs. - 2005. - Vol. 52, No. 8. - P. 508-511.

J256. Cheng A.C. An energy efficient instruction set synthesis framework for low power embedded system designs. / Cheng A.C., Tyson G.S. // IEEE Transactions on Computers. - 2005. - Vol. 54, No. 6. - P. 698-713.

J257. Benini L. Memory energy minimization by data compression: algorithms, architectures and implementation. / Benini L., Bruni D., Macii A., Macii E. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2004. - Vol. 12, No. 3. - P. 255-268.

J258. Kamuf M. A simplified computational kernel for trellis-based decoding. / Kamuf M., Anderson J.B., Owall V. // IEEE Communications Letters. - 2004. - Vol. 8, No. 3. - P. 156-158.

J259. Wei-Chung Cheng. Chromatic encoding: a low power encoding technique for digital visual interface. / Wei-Chung Cheng, Pedram M. // IEEE Transactions on Consumer Electronics. - 2004. - Vol. 50, No. 1. - P. 320-328.

J260. Efthymiou A. A CAM with mixed serial-parallel comparison for use in low energy caches. / Efthymiou A., Garside J.D. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2004. - Vol. 12, No. 3. - P. 325-329.

J261. Haj Ali Asgari F. A low-power reduced swing global clocking methodology. / Haj Ali Asgari F., Sachdev M. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2004. - Vol. 12, No. 5. - P. 538-545.

J262. Kursun V. Sleep switch dual threshold Voltage domino logic with reduced standby leakage current. / Kursun V., Friedman E.G. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2004. - Vol. 12, No. 5. - P. 485-496.

J263. Pingshan Wang. Pulsed wave interconnect. / Pingshan Wang, Pei G., Kan E.C.-C. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2004. - Vol. 12, No. 5. - P. 453-463.

J264. Hyeonuk Jeong. Low-power multiplierless DCT architecture using image correlation. / Hyeonuk Jeong, Jinsang Kim, Won-kyung Cho. // IEEE Transactions on Consumer Electronics. - 2004. - Vol. 50, No. 1. - P. 262-267.

J265. Melhem R. The interplay of power management and fault recovery in real-time systems. / Melhem R., Mosse D., Elnozahy E. // IEEE Transactions on Computers. - 2004. - Vol. 53, No. 2. - P. 217-231.

J266. Parikh D. Power-aware branch prediction: characterization and design. / Parikh D., Skadron K., Zhang Y., Stan M. // IEEE Transactions on Computers. - 2004. - Vol. 53, No. 2. - P. 168-186.

J267. De La Luz V. Array regrouping and its use in compiling data-intensive, embedded applications. / De La Luz V., Kandemir M. // IEEE Transactions on Computers. - 2004. - Vol. 53, No. 1. - P. 1-19.

J268. Sirisantana N. Low-power design using multiple channel lengths and oxide thicknesses. / Sirisantana N., Kaushik Roy. // IEEE Design & Test of Computers. - 2004. - Vol. 21, No. 1. - P. 56-63.

J269. Wei-Chung Cheng. Power minimization in a backlit TFT-LCD display by concurrent brightness and contrast scaling. / Wei-Chung Cheng, Pedram M. // IEEE Transactions on Consumer Electronics. - 2004. - Vol. 50, No. 1. - P. 25-32.

J270. Alonso L. Automatic rate adaptation and energy-saving mechanisms based on cross-layer information for packet-switched data networks. / Alonso L., Agusti R. // IEEE Communications Magazine. - 2004. - Vol. 42, No. 3. - P. S15-S20.

J271. De La Luz V. Access pattern restructuring for memory energy. / De La Luz V., Kadayif I., Kandemir M., Sezer U. // IEEE Transactions on Parallel and Distributed Systems. - 2004. - Vol. 15, No. 4. - P. 289-303.

J272. Byung-Do Yang. An 800-MHz low-power direct digital frequency synthesizer with an on-chip D/a converter. / Byung-Do Yang, Choi J.-H., Seon-Ho Han, Lee-Sup Kim, Hyun-Kyu Yu. // IEEE Journal of Solid-State Circuits. - 2004. - Vol. 39, No. 5. - P. 761-774.

J273. Pagiamtzis K. A low-power content-addressable memory (CAM) using pipelined hierarchical search scheme. / Pagiamtzis K., Sheikholeslami A. // IEEE Journal of Solid-State Circuits. - 2004. - Vol. 39, No. 9. - P. 1512-1519.

J274. Changbo Long. Distributed sleep transistor network for power reduction. / Changbo Long, Lei He. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2004. - Vol. 12, No. 9. - P. 937-946.

J275. Rama Sangireddy. Low-power high-performance reconfigurable computing cache architectures. / Rama Sangireddy, Kim H., Somani A.K. // IEEE Transactions on Computers. - 2004. - Vol. 53, No. 10. - P. 1274-1290.

J276. Zhu D. Power-aware scheduling for AND/OR graphs in real-time systems. / Zhu D., Mosse D., Melhem R. // IEEE Transactions on Parallel and Distributed Systems. - 2004. - Vol. 15, No. 9. - P. 849-864.

J277. Janapsatya A. REMcode: relocating embedded code for improving system efficiency. / Janapsatya A., Parameswaran S., Henkel J. // IEE Proceedings - Computers and Digital Techniques. - 2004. - Vol. 151, No. 6. - P. 457-465.

J278. Yang Xiao. On optimizing energy consumption for mobile handsets. / Yang Xiao, Haizhon Li, Yi Pan, Kui Wu, Jie Li. // IEEE Transactions on Vehicular Technology. - 2004. - Vol. 53, No. 6. - P. 1927-1941.

J279. Zhipei Chi. On the better protection of short-frame turbo codes. / Zhipei Chi, Zhongfeng Wang, Parhi K.K. // IEEE Transactions on Communications. - 2004. - Vol. 52, No. 9. - P. 1435-1439.

J280. Wei Ye. Medium access control with coordinated adaptive sleeping for wireless sensor networks. / Wei Ye, Heidemann J., Estrin D. // IEEE/ACM Transactions on Networking. - 2004. - Vol. 12, No. 3. - P. 493-506.

J281. Kanda K. 90% write power-saving SRAM using sense-amplifying memory cell. / Kanda K., Sadaaki H., Sakurai T. // IEEE Journal of Solid-State Circuits. - 2004. - Vol. 39, No. 6. - P. 927-933.

J282. Weidong Wang. Input space adaptive design: a high-level methodology for optimizing energy and performance. / Weidong Wang, Raghunathan A., Lakshminarayana G., Jha N.K. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2004. - Vol. 12, No. 6. - P. 590-602.

J283. Lafruit G. View-dependent, scalable texture streaming in 3-D QoS with MPEG-4 visual texture coding. / Lafruit G., Delfosse E., Osorio R., van Raemdonck W., Ferentinos V., Bormans J. // IEEE Transactions on Circuits and Systems for Video Technology. - 2004. - Vol. 14, No. 7. - P. 1021-1031.

J284. Seung Jun Baek. Minimizing energy consumption in large-scale sensor networks through distributed data compression and hierarchical aggregation. / Seung Jun Baek, Gustavo de Veciana, Xun Su. // IEEE Journal on Selected Areas in Communications. - 2004. - Vol. 22, No. 6. - P. 1130-1140.

J285. Lorch J.R. PACE: a new approach to dynamic voltage scaling. / Lorch J.R., Smith A.J. // IEEE Transactions on Computers. - 2004. - Vol. 53, No. 7. - P. 856-869.

J286. Yingtao Jiang. A novel multiplexer-based low-power full adder. / Yingtao Jiang, Al-Sheraidah A., Yuke Wang, Sha E., Jin-Gyun Chung. // IEEE Transactions on Circuits and Systems II: Express Briefs. - 2004. - Vol. 51, No. 7. - P. 345-348.

J287. Jongsun Park. High-performance FIR filter design based on sharing multiplication. / Jongsun Park, Muhammad K., Roy K. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2003. - Vol. 11, No. 2. - P. 244-253.

J288. Hasan M. A novel coefficient ordering based low power pipelined radix-4 FFT processor for wireless LAN applications. / Hasan M., Arslan T., Thompson J.S. // IEEE Transactions on Consumer Electronics. - 2003.

- Vol. 49, No. 1. - P. 128-134.

J289. Zhu D. Scheduling with dynamic voltage/speed adjustment using slack reclamation in multiprocessor real-time systems. / Zhu D., Melhem R., Childers B.R. // IEEE Transactions on Parallel and Distributed Systems. - 2003. - Vol. 14, No. 7. - P. 686-700.

J290. Ho-Myung Chang. Cryogenic cooling temperature of HTS transformers for compactness and efficiency. / Ho-Myung Chang, Yeon Suk Choi, Van Sciver S.W., Baldwin T.L. // IEEE Transactions on Applied Superconductivity. - 2003. - Vol. 13, No. 2. - P. 2298-2301.

J291. Chi-Sheng Lin. A low-power precomputation-based fully parallel content-addressable memory. / Chi-Sheng Lin, Jui-Chuan Chang, Bin-Da Liu. // IEEE Journal of Solid-State Circuits. - 2003. - Vol. 38, No. 4. - P. 654-662.

J292. Petrov P. Application-specific instruction memory customizations for power-efficient embedded processors. / Petrov P., Orailoglu A. // IEEE Design & Test of Computers. - 2003. - Vol. 20, No. 1. - P. 18-25.

J293. Wen-Chang Yeh. High-speed and low-power split-radix FFT. / Wen-Chang Yeh, Chein-Wei Jen. // IEEE Transactions on Signal Processing. - 2003. - Vol. 51, No. 3. - P. 864-874.

J294. Tang Y. Adaptive Miller capacitor multiplier for compact on-chip PLL filter. / Tang Y., Ismail M., Bibyk S. // Electronics Letters. - 2003. - Vol. 39, No. 1. - P. 43-45.

J295. Chandra A. A unified approach to reduce SOC test data volume, scan power and testing time. / Chandra A., Chakrabarty K. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2003. - Vol. 22, No. 3. - P. 352-363.

J296. Gang Quan. Minimal energy fixed-priority scheduling for variable voltage processors. / Gang Quan, Xiaobo Sharon Hu. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2003. - Vol. 22, No. 8. - P. 1062-1071.

J297. Gurumurthi S. Reducing disk power consumption in servers with DRPM. / Gurumurthi S., Sivasubramaniam A., Kandemir M., Franke H. // Computer. - 2003. - Vol. 36, No. 12. - P. 59-66.

J298. Tschanz J.W. Dynamic sleep transistor and body bias for active leakage power control of microprocessors. / Tschanz J.W., Narendra S.G., Ye Y., Bloechel B.A., Borkar S., De V. // IEEE Journal of Solid-State Circuits. - 2003. - Vol. 38, No. 11. - P. 1838-1845.

J299. Bose A. Analysis of traffic flow with mixed manual and semiautomated vehicles. / Bose A., Ioannou P.A. // IEEE Transactions on Intelligent Transportation Systems. - 2003. - Vol. 4, No. 4. - P. 173-188.

J300. Mansour M.M. High-throughput LDPC decoders. / Mansour M.M., Shanbhag N.R. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2003. - Vol. 11, No. 6. - P. 976-996.

J301. Chua-Chin Wang. An area-saving decoder structure for ROMs. / Chua-Chin Wang, Ya-Hsin Hsueh, Ying-Pei Chen. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2003. - Vol. 11, No. 4. - P. 581-589.

J302. Yan Ye. Fast and memory efficient text image compression with JBIG2. / Yan Ye, Cosman P. // IEEE Transactions on Image Processing. - 2003. - Vol. 12, No. 8. - P. 944-956.

J303. Huang M.C. Customizing the branch predictor to reduce complexity and energy consumption. / Huang M.C., Chaver D., Pinuel L., Prieto M., Tirado F. // IEEE Micro. - 2003. - Vol. 23, No. 5. - P. 12-25.

J304. Byung-Do Yang. A low-power charge-recycling ROM architecture. / Byung-Do Yang, Lee-Sup Kim. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2003. - Vol. 11, No. 4. - P. 590-600.

J305. Nalamalpu A. Boosters for driving long onchip interconnects-design issues, interconnect synthesis, and comparison with repeaters. / Nalamalpu A., Srinivasan S., Burleson W.P. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2002. - Vol. 21, No. 1. - P. 50-62.

J306. Nose K. VTH -hopping scheme to reduce subthreshold leakage for low-power processors. / Nose K.,

Hirabayashi M., Kawaguchi H., Seongsoo Lee, Sakurai T. // IEEE Journal of Solid-State Circuits. - 2002. - Vol. 37, No. 3. - P. 413-419.

J307. Schurgers C. Optimizing sensor networks in the energy-latency-density design space. / Schurgers C., Tsiatsis V., Ganeriwal S., Srivastava M. // IEEE Transactions on Mobile Computing. - 2002. - Vol. 1, No. 1. - P. 70-80.

J308. Eui-Young Chung. Value-sensitive automatic code specialization for embedded software. / Eui-Young Chung, Luca B., DeMicheli G., Luculli G., Carilli M. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2002. - Vol. 21, No. 9. - P. 1051-1067.

J309. Byunghoon Bae. Feasibility test of an electromagnetically driven valve actuator for glaucoma treatment. / Byunghoon Bae, Nakhoon Kim, Hongseok Kee, Seon-Ho Kim, Yeon Lee, Sangho Lee, Kyihwan Park. // Journal of Microelectromechanical Systems. - 2002. - Vol. 11, No. 4. - P. 344-354.

J310. Chandra A. Low-power scan testing and test data compression for system-on-a-chip. / Chandra A., Chakrabarty K. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2002. - Vol. 21, No. 5. - P. 597-604.

J311. Badawy W. Algorithm-based low-power VLSI architecture for 2D mesh video-object motion tracking. / Badawy W., Bayoumi M. // IEEE Transactions on Circuits and Systems for Video Technology. - 2002. - Vol. 12, No. 4. - P. 227-237.

J312. Chulwoo Kim. A low-swing clock double-edge triggered flip-flop. / Chulwoo Kim, Sung-Mo Kang. // IEEE Journal of Solid-State Circuits. - 2002. - Vol. 37, No. 5. - P. 648-652.

J313. Cheng-Ta Hsieh. Architectural energy optimization by bus splitting. / Cheng-Ta Hsieh, Pedram M. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2002. - Vol. 21, No. 4. - P. 408-414.

J314. Yung-Hsiang Lu. Power-aware operating systems for interactive systems. / Yung-Hsiang Lu, Benini L., De Micheli G. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2002. - Vol. 10, No. 2. - P. 119-134.

J315. Yung-Hsiang Lu. Dynamic frequency scaling with buffer insertion for mixed workloads. / Yung-Hsiang Lu, Benini L., De Micheli G. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2002. - Vol. 21, No. 11. - P. 1284-1305.

J316. Stitt G. Energy advantages of microprocessor platforms with on-chip configurable logic. / Stitt G., Vahid F. // IEEE Design & Test of Computers. - 2002. - Vol. 19, No. 6. - P. 36-43.

J317. Badawy W. A low power VLSI architecture for mesh-based video motion tracking. / Badawy W., Bayoumi M.A. // IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing. - 2002. - Vol. 49, No. 7. - P. 488-504.

J318. Masselos K. Memory accesses reordering for interconnect power reduction in sum-of-products computations. / Masselos K., Theoharis S., Merakos P., Stouraitis T., Goutis C.E. // IEEE Transactions on Signal Processing. - 2002. - Vol. 50, No. 11. - P. 2889-2899.

J319. Masera G. Architectural strategies for low-power VLSI turbo decoders. / Masera G., Mazza M., Piccinini G., Viglione F., Zamboni M. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2002. - Vol. 10, No. 3. - P. 279-285.

J320. Salkintzis A.K. An outband paging protocol for energy-efficient mobile communications. / Salkintzis A.K., Chamzas C. // IEEE Transactions on Broadcasting. - 2002. - Vol. 48, No. 3. - P. 246-256.

J321. Benini L. Code compression architecture for cache energy minimisation in embedded systems. / Benini L., Macii A., Nannarelli A. // IEE Proceedings - Computers and Digital Techniques. - 2002. - Vol. 149, No. 4. - P. 157-163.

J322. Grass N. Fuzzy-logic-based power control system for multifield electrostatic precipitators. IEEE Transactions on Industry Applications. - 2002. - Vol. 38, No. 5. - P. 1190-1195.

J323. Unsal O.S. Cool-Fetch: Compiler-Enabled Power-Aware Fetch Throttling. / Unsal O.S., Krishna C.M., Mositz C.A. // Computer Architecture Letters. - 2002. - Vol. 1, No. 1. - P. 5.

J324. Shanq-Jang Ruan. ENPCO: an entropy-based partition-codec algorithm to reduce power for bipartition-codec architecture in pipelined circuits. / Shanq-Jang Ruan, Naroska E., Yen-Jen Chang, Lai F., Schwiegelshohn U. // IEEE Transactions on Very Large Scale Integration (VLSI) Systems. - 2002. - Vol. 10, No. 6. - P. 942-949.

J325. Simunic T. Event-driven power management. / Simunic T., Benini L., Glynn P., De Micheli G. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2001. - Vol. 20, No. 7. - P. 840-857.

J326. Miyatake H. A design for high-speed low-power CMOS fully parallel content-addressable memory macros. / Miyatake H., Tanaka M., Mori Y. // IEEE Journal of Solid-State Circuits. - 2001. - Vol. 36, No. 6. - P. 956-968.

J327. Yung-Hsiang Lu. Comparing system level power management policies. / Yung-Hsiang Lu, De Micheli G. // IEEE Design & Test of Computers. - 2001. - Vol. 18, No. 2. - P. 10-19.

J328. Qiu Q. Stochastic modeling of a power-managed system-construction and optimization. / Qiu Q., Qu Q., Pedram M. // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. - 2001. - Vol. 20, No. 10. - P. 1200-1217.

J329. Bai-Sun Kong. Conditional-capture flip-flop for statistical power reduction. / Bai-Sun Kong, Sam-Soo Kim, Young-Hyun Jun. // IEEE Journal of Solid-State Circuits. - 2001. - Vol. 36, No. 8. - P. 1263-1271.

J330. Svensson C. Optimum voltage swing on on-chip and off-chip interconnect. IEEE Journal of Solid-State Circuits. - 2001. - Vol. 36, No. 7. - P. 1108-1112.
