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ТЕМАТИЧЕСКИЙ РЕФЕРАТИВНЫЙ СБОРНИК № 50-2/2

“Energy Saving and Consumption Reducing”
(«Энергосбережение»)

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"Heuristic Approaches to Energy-Efficient Network Design Problem"

Energy management remains a critical problem in wireless networks since battery technology cannot keep up with rising communication expectations. Current approaches to energy conservation reduce the energy consumption of the wireless interface either for a given communication task or during idling. However, a complete solution requires minimizing the energy spent for both communication (i.e., for data and control overhead) and idling. This problem can be expressed as an energy-efficient network design problem, which is, not surprisingly, NP-hard. Therefore, in this paper, we study three heuristic approaches. Our study shows that the first approach that prioritizes communication energy conservation does not save energy. The second approach, which tries to reduce energy used for both data and in idling, becomes cost-prohibitive due to its high control overhead. Hence, we propose a third approach that prioritizes idling energy conservation. Due to its low control overhead, this approach meets the challenge of operating the network with low energy cost. [C960]

"Exact Forwarding Table Partitioning for Efficient TCAM Power Savings"

Excessive power consumption is deemed one of the major drawbacks of TCAM-based IP search engines. This paper proposes a simple and yet efficient forwarding table partitioning algorithm aiming to achieve significant TCAM power savings. Our algorithm partitions the IP address space into a set of adjoining but non-overlapping search ranges comprising an exactly identical number of prefixes to be accommodated in a TCAM segment, dubbed exact table partitioning (ETAP). During a search operation, only one single range is examined to reduce overall TCAM power consumption substantially. [C961]

"Dynamic Power Management and Dynamic Voltage Scaling in Real-time CMP Systems"

Real-time embedded systems need reducing power consumption while still maintaining high performance. Dynamic power management (DPM) and dynamic voltage scaling (DVS) are effective control techniques to reduce the energy consumption. We present a real-time energy saving scheduling (RESS) algorithm using DPM and DVS to reduce the energy cost for chip multiprocessor (CMP) systems. The simulating experiment results indicate that our algorithm can save system energy cost with little system performance degradation. [C962]

"Search Area Selective Reuse Algorithm in Motion Estimation"

Motion estimation has been widely studied and used to improve coding efficiency with small data access for power-saving. Conventional search area reuse algorithm requires small memory access by reuse of search area, but, suffers from coding efficiency degradation in fast motion video sequence. In this paper, we propose a search area selective reuse algorithm. The proposed algorithm well selects search center for reducing memory access in slow motion region and for tracking real motion in fast motion region according to the motion vector and search center information of the neighbor block. Compared to the conventional reuse algorithm, our experimental results show that the proposed algorithm prevents the coding efficiency degradation with small memory access overhead by tracking real motion in fast motion frames. [C963]

"Application Specific VLIW Processors with Power-Saving Mode Via Variable Arithmetic Accuracy"

This paper discusses an idea for power-saving mode in application specific processors in the domain of digital signal processing. This idea is based on a multiple (in practice double) accumulator model, which is used in order to obtain high accuracy in a series of floating-point additions. The goal is to introduce a possibility of reducing the power consumption without reducing the functionality. In the case of low power, instead of decreasing the performance of the system or shutting down the system, as it is done in other approaches, in our concept merely the accuracy of the floating point accumulation is reduced. Therefore although the quality of service is reduced, the performance is not. [C964]

"Energy-Efficient Scheduling Optimization in Wireless Sensor Networks with Delay Constraints"

Energy-efficiency in wireless sensor networks is a very critical design issue, because they usually operate with tiny batteries and take a long time for replacement. In this context, we analyze the optimized scheduling strategy to minimize the energy consumed by data fusion in wireless sensor network. For implementation purpose, a low-complexity fractional-inverse- log scheduling (FILS) algorithm is presented to reduce extra significant amount of energy consumption compared to previously designed protocols. Next, in order to eliminate the communication overhead in centralized scheduling protocols, the simplified distributed fractional-inverse-log scheduling is also provided, which is shown to be very efficient in energy saving especially for a large-scale wireless sensor network. With consideration of the peak power constraint in real circuit design, we update FILS to further constrict the transmission time. Simulation results show that with peak transmission power limitation, energy consumption is still substantially reduced by FILS, and it yields more energy saving for the system with high peak-to-average power ratio (PAPR). [C965]

"An Efficient Energy Conserving Scheme for IEEE 802.11 ADHOC Networks"

Battery power is one of the major and limited resources in wireless communication. In the distributed coordination function (DCF) of IEEE 802.11 power saving mechanism (PSM), energy consumption can be reduced by turning off the radio during idle times. However, IEEE 802.11 PSM is known to cause unnecessary energy consumption due to the problems of an overhearing, a back-off time delay and possible packet collisions. To overcome these problems, we present a new MAC protocol called 'slot based PSM (static and dynamic)' for IEEE 802.11 WLANs. In our proposed scheme, the beyond-ATIM window is divided into a number of time slots, and any node that participates in communication wakes up in its slot times only and other nodes can enter to doze mode during the slot times. [C966]

"AMAC: Traffic-Adaptive Sensor Network MAC Protocol through Variable Duty-Cycle Operations"

Sensor network MAC protocols usually employ periodic sleep and wakeup, achieving low duty-cycle to save energy and to increase the lifetime of battery-powered sensor devices. However, existing protocols require all the sensor nodes to operate on the same static schedule, waking up all the nodes at the same fixed interval periodically. This paper proposes a new media access control protocol called AMAC that can achieve significant energy savings by dynamically changing the schedule of each node depending on the traffic. In AMAC, each node can adjust the duration of the periodic interval as well as the duration of the active period depending on the traffic. Thus, busy nodes can operate with a high duty-cycle while idle nodes can operate with a low duty-cycle at the same time, achieving both low-energy and high-performance. The results of our detailed simulations confirm that AMAC can reduce the average energy consumption by a factor of up to 6.8 compared to an existing fixed duty-cycle MAC protocol while it can also improve the network performance for burst traffic patterns. [C967]

"Multi-Vth Level Conversion Circuits for Multi-VDD Systems"

Employing multiple supply voltages (multi-VDD) is attractive for reducing the power consumption without sacrificing the speed of an integrated circuit (IC). In order to transfer signals among the circuits operating at different voltage levels specialized voltage interface circuits are required. Two novel multi-threshold voltage (multi-Vth) level converters are proposed in this paper. The proposed level converters are compared with the previously published circuits for different values of the lower supply voltage. When the circuits are individually optimized for minimum power consumption in a 0.18mum CMOS technology, the proposed level converters offer significant power savings of up to 70% as compared to the previously published circuits. Alternatively, when the circuits are individually optimized for minimum propagation delay, speed is enhanced by up to 78% with the proposed circuits. [C968]

"Asymmetric clock driver for improved power and noise performances"

One of the most important sources of switching noise and power consumption in large VLSI circuits is the clock generation and distribution tree. This paper analyzes how the use of an asymmetric clock can be an important solution to reduce the switching noise generated by the global clock, with a very reduced degradation in performances and reliability. The suited sizing of clock generators and the design of asymmetric clock tree cells, show the benefits of the proposed technique, validated through a design example where a 50% of noise reduction is achieved with 10% of loss in operation frequency and no penalty, even saving, in power consumption. [C969]

"Breaking the Power-Delay Tradeoff: Design of Low-Power High-Speed MOS Current-Mode Logic Circuits Operating with Reduced Supply Voltage"

In this paper, the authors study the operation of MOS current-mode logic (MCML) gates at lower-than-nominal supply voltages. The authors show that power can be traded for speed by reducing the supply voltage below the nominal value, while the power-delay product stays nearly constant. The authors propose a negative bias strategy that enables the gates to operate at maximum speed with a reduced supply voltage, thus achieving a power saving of up to 35% at no cost for speed. Comparison with CMOS logic style are presented for three different technology nodes (0.25mum, 0.18mum and 0.13mum CMOS). [C970]

"Architecture Level Power-Performance Tradeoffs for Pipelined Designs"

This paper presents a method to investigate power-performance tradeoffs in digital pipelined designs. The method is applied at the architectural level of the design. It is shown that addressing the tradeoffs at this level results in significant savings in power consumption without impacting the performance. The reduction in power is obtained through reducing the number of registers used in implementing the pipeline stages. The method has been validated by synthesizing a floating-point unit with different pipeline stages and power consumption of the designs were obtained using industry standard tools. It is shown that it is possible to obtain up to 18% reduction in power without affecting the clock period and with less area. [C971]

"On-Chip VDC Circuit for SRAM Power Management"

Leakage current becomes the dominant factor for contributing to the static power consumption. Power management technique is then required to bring down the power consumption. One of the most effective methods is to reduce the power supply voltage in the standby mode or in the power down active mode. In this paper, a simple on-chip voltage down converter is proposed. By designing an internal reference voltage that is proportional to the device threshold voltage, the SRAM cell circuit states can be preserved within a broad range of power supply and temperature. For the 1V-to-0.6V dc-dc conversion, this on-chip VDC only consumes 156 muW standby power and is within 2 mV output voltage variation for load current varying from 1 mu A to 10 mA. By comparing with other power management techniques, the on-chip VDC method is excellent in the static power saving, overall design simplicity and small layout area. [C972]

"A Power-Saved 1Gbps Irregular LDPC Decoder based on Simplified Min-Sum Algorithm"

In this paper we proposed a fully-parallel irregular LDPC decoder which uses only registers to store the temporary intrinsic messages. Our decoder adopts a simplified min-sum algorithm to reduce the hardware implementation complexity and area, and due to the factor modification we achieve a negligible performance loss compared with the general min-sum algorithm. Considering reducing the power consumption, we also propose a power-saved strategy according to which the message evolution will halt as the parity-check condition is satisfied. This strategy will save us higher than 50% power under good channel condition. The synthesis result in 0.18 mum CMOS technology shows our decoder for (648,540) irregular LDPC code achieves high throughput (1 Gbps) with 9.0 ns latency. [C973]

"Adaptive Low/High Voltage Swing CMOS Driver for On-Chip Interconnects"

This paper reports the design of a high performance, adaptive low/high swing CMOS driver circuit (mj-driver) suitable for driving of global interconnects with large capacitive load. When implemented on 0.13mum CMOS technology, mj-driver performs 16% faster, reduces the power consumption by 3%, and energy delay product by 19% when compared with a counterpart driver in diode-connected configuration. On the other hand, mj-driver has 47% lower active area and only requires one set of sizing for optimum performance at 1 and 0.8V. Furthermore, unlike its counter part which exhibits 30% variation in output swing voltage with variation in the load, the output voltage swing for the proposed driver remains unchanged with the output load. Comparisons of the proposed driver with conventional full swing CMOS driver are presented as well, indicating a significant saving in energy, due to the reduced swing voltage. The proposed driver has the ability to switch from a low swing to high swing mode, through a line monitoring mechanism [C974]

"Switch Controlled Source Amplifier for Low Power Mobile TFT-LCD Driver IC"

Switch controlled source amplifier (SCSA) is proposed for low power mobile TFT-LCD driver ICs (T-LDIs). In SCSA scheme, the operation of the source drivers in a T-LDI is determined by the source line load of TFT-LCD. That is, output stage current of source buffers is reduced when the source line load is separated for current saving operation such as charge sharing between VCOM and source lines. With SCSA scheme, all the static current of source buffers can be reduced as far as phase margin of the output buffers is permitted. A test chip was fabricated in a 5-V/0.8-mum triple-metal CMOS process with QVGA resolution, and the experimental results show that the power consumption of 11%~16% was saved with die size overhead less than 1%. [C975]

"An Adaptive Sleep Transistor Biasing Scheme for Low Leakage SRAM"

Reducing the leakage power in embedded SRAM memories is critical for low-power applications. Raising the source voltage of SRAM cells in standby mode reduces the leakage currents effectively. However, in order to preserve the state of the cell in standby mode, source voltage cannot be raised beyond a certain level. The maximum source voltage of an SRAM cell is determined by its hold stability in a particular process corner. Hence, in order to achieve the maximum leakage reduction, the source voltage of each individual cell must be raised up to its maximum safe level. However, any cell-based technique realizing this would be practically not feasible. In this paper, we propose an SRAM leakage reduction technique, referred to as adaptive sleep transistor biasing, which automatically fine-tunes the source voltage of individual memory blocks to their optimum level. Thus, maximum leakage savings can be expected while data is safely retained during standby mode. Preliminary study shows that the proposed scheme has the potential of providing substantial saving in leakage power over those by using the conventional techniques. [C976]

"Voltage-Frequency Island Partitioning for GALS-based Networks-on-Chip"

Due to high levels of integration and complexity, the design of multi-core SoCs has become increasingly challenging. In particular, energy consumption and distributing a single global clock signal throughout a chip have become major design bottlenecks. To deal with these issues, a globally asynchronous, locally synchronous (GALS) design is considered for achieving low power consumption and modular design. Such a design style fits nicely with the concept of voltage-frequency islands (VFIs) which has been recently introduced for achieving fine-grain system-level power management. This paper proposes a design methodology for partitioning an NoC architecture into multiple VFIs and assigning supply and threshold voltage levels to each VFI Simulation results show about 40% savings for a real video application and demonstrate the effectiveness of our approach in reducing the overall system energy consumption. The results and functional correctness are validated using an FPGA prototype for an NoC with multiple VFIs. [C977]

"A Hold Friendly Flip-Flop For Area Recovery"

In this paper a new family of scan flip-flops is introduced whose scan pin hold characteristic has improved while data pin timing is left intact. This characteristic helps to alleviate scan chain hold problem while meeting the maximum frequency in data path. This solution can reduce the number of buffers inserted in the scan chain to fix hold violations. The new flip-flop can save up to 29% area as compared to the usage of normal flip-flop combined with hold-fixing buffers. [C978]

"Balancing Resistance and Capacitance of Signal Interconnects for Power Saving"

This paper presents the results of a study on the trade-off between resistance and capacitance of signal interconnects in a low-power circuit to further reduce power consumption without sacrificing speed performance. Simulation and experimental results show that by simply thinning down the interconnect height by half; the power consumption and frequency of a test interconnect-loaded ring- oscillator are improved by 12.7% and 3.5%, respectively. The combination of thin-interconnect with low-operational-power (LOP) transistors, which are designed to have low threshold voltage and to operate at lower supply voltage, results in a 50% reduction in power consumption without penalty in frequency. By thinning down the interconnect height, the RC time constant of the interconnect is increased. However, this increment does not have negative impact on circuit performance until the length of interconnect is above few hundred micrometers. This indicates thin interconnect is suitable for intermediate interconnect levels where the majority of shorter interconnects are located. Reliability study of thin-interconnect shows no sign of electro-migration resistance degradation. Furthermore, only a small impact of process variations on timing of a critical path, which uses thin-interconnects, was observed. [C979]

"Reducing Off-Chip Memory Access Costs Using Data Recomputation in Embedded Chip Multi-processors"

There have been numerous efforts on Scratch-Pad Memory (SPM) management in the context of single CPU systems and, more recently, multi-processor architectures. This paper presents a novel SPM space utilization strategy, for embedded chip multi-processor systems, based on recomputing the value of an off-chip data element using on-chip (SPM resident) data elements. In doing so, our goal is to eliminate the corresponding off-chip memory access that would otherwise be performed, and save execution cycles and power. This paper presents the details of a compiler algorithm that implements this approach and reports the experimental data we collected using six data-intensive applications. Our results indicate that, on a four processor chip multiprocessor, the average performance improvement our approach brings is about 11.8%, over a state-of-the-art SPM management scheme. We also observed that there is a specific range of total SPM size/total data size ratios, for

which our approach generates the best results. Finally, our results also show that the proposed approach brings consistent improvements when the number of CPUs is varied between 2 and 16. [C980]

"Low-power design technique for flash A/D converters based on reduction of the number of comparators"

This paper proposes a low-power, small chip area design technique for flash analog-to-digital converters (A/D converters). The proposed technique reduces power consumption of flash A/D converters by 50 % reduction of the number of comparators. Because output signals of flash A/D converters are thermometer code, only a few comparators whose reference voltages are around the input signal are significant and the other comparators can be removed. A novel track and hold circuit (T/H circuit) which can exchange its two balanced output signals is introduced. Thanks to the T/H circuit, the required input range of the comparator is limited to half of that of conventional one. The proposed A/D converter using the proposed T/H circuit can realize the same accuracy with the conventional one. The proposed technique is applied to a 6-bit 528 Msamples/s A/D converter realization. Its power consumption is evaluated by HSPICE simulations. It is confirmed that the proposed technique can save 34% of power consumption compared with conventional one. [C981]

"A Multiplier Structure Based on a Novel Real-time CSD Recoding"

Implementation of digital signal processing (DSP) algorithms in hardware, such as field programmable gate arrays (FPGAs), requires a large number of multiplications. In this paper, we introduce a novel multiplier structure that converts from 2's complement to canonical signed digit (CSD) representation in real time. The proposed algorithm increases the number of zero partial products (which can be simplified by shift operations) to approximately 66.7% compared with 50% for modified Booth's recoding. Also, the proposed hardware structure reduces the non-zero partial products to a minimum, and consequently the number of arithmetic operations in the carry-save structure is reduced. So, our proposed hardware decreases both the time required for multiplication and the power consumption of the multiplier. Furthermore, because the proposed structure uses real time CSD recoding, and does not require a fixed value for the multiplier input to be known a priori, the proposed multiplier can be used to implement digital filters with non-fixed filter coefficients, such as adaptive filters. [C982]

"A Dual-Threshold FPGA Routing Design for Subthreshold Leakage Reduction"

Field-programmable gate arrays are attractive candidates for wireless applications due to their reconfiguration capability and high performance development. However, sub-threshold leakage power in modern FPGAs has become a critical obstacle for these devices in entering to this application domain. Subthreshold leakage current of programmable interconnections is responsible for most of the static power dissipation. This work proposes and evaluates ten routing designs based on the dual-threshold technique to reduce leakage power. Alternating between buffers and pass transistors, we analyze the percentage constitution of low-Vthand high-Vthtransistors as a function of the leakage reduction and delay increment tradeoff. By routing a suite of MCNC benchmark circuits, we show that an average savings of about 28.83% (as high as 48.46%) in total interconnect leakage can be obtained with 8.73% worst case average delay penalty. [C983]

"Reducing Test-bus Power Consumption in Huffman Coding Based Test Data Compression for SOCs"

This paper highlights the problem of test-bus power reduction in system-on-chip testing. It has been shown that while the cores are fitted with IEEE 1500 wrapper, transitions occurring within test bus and bypass registers can be comparable to those in the scan-chain. Unlike bus encoding the proposed solution does not use any extra hardware and neither affects the compression ratio, nor test application time. Experimental results on ISCAS89 benchmark circuits show up to 87% saving of transitions occurring in test bus in a Huffman coding based test data compression mechanism. A trade-off mechanism has also been shown between compression and test-bus power consumption. [C984]

"Energy Management in Solar Powered WLAN Mesh Nodes Using Online Meteorological Data"

Solar powered WLAN mesh nodes are assigned a solar panel and battery size based on power consumption profiles. If future loading exceeds the design target, then a node may not be able to achieve the outage performance for which it was configured. To prevent this from happening, forced power saving can be used to reduce node power consumption to acceptable levels. However, forced power saving generates a deficit in offered capacity which should be minimized as much as possible. In this paper we first formulate this as a non-linear control problem. An efficient linear programming approximation is then defined and solved based on an

offline optimization where future solar insolation is known in advance. This provides a bound on the performance of any real control algorithm. We show that the LP solution is accurate in that it comes very close to achieving a no-control capacity deficit lower bound. A control algorithm is then proposed whose operation uses dynamic access to publicly available on-line meteorological data. The proposed approach uses this on-line data but could also benefit from on-line weather forecasting. Our results show that the proposed algorithm minimizes node outage and performs favorably compared to the offline and no-control lower bounds. [C985]

"Energy-saving unit in the wind-cooling system of the transformer"

In view of the existing problem in wind-cooling system of the power transformer, this paper puts forward a design of wind-cooling energy-saving unit composed of the converter. It also introduces the components and function of the unit's hardware and the designing of the software. Simulation tests have proved that this unit can greatly reduce the power consumption of blower fans. [C986]

"Reducing Energy Consumption of On-Chip Networks Through a Hybrid Compiler-Runtime Approach"

This paper investigates a compiler-runtime approach for reducing power consumption in the context of the network-on-chip (NoC) based chip multiprocessor (CMP) architectures. Our proposed approach is based on the observation that the same communication patterns across the nodes of a mesh based CMP repeat themselves in successive iterations of a loop nest. The approach collects the link usage statistics during the execution of the first few iterations of a given loop nest and computes the slack (allowable delay) for each communication transaction. This information is subsequently utilized in selecting the most appropriate voltage levels for the communication links (and the corresponding frequencies) in executing the remaining iterations of the loop nest. The results with the benchmarks from the MediaBench suite show that, not only this hybrid approach generates better energy savings than a pure hardware-directed voltage scaling scheme, but it also leads to much less performance degradation than the latter. Specifically, the average energy savings achieved by the pure hardware based scheme and our approach are 24.9% and 38.1%, respectively, and the corresponding performance overhead numbers are 8.3% and 2.1%. Our results also show that the hybrid approach generates much better savings than two proposed pure compiler based schemes. In addition, our experimental evaluation indicates that the energy savings obtained through the proposed approach are very close to optimal savings (within 3%) under the same performance bound. [C987]

"Mobility-Sensitive Clustering Algorithm to Balance Power Consumption for Mobile Ad Hoc Networks"

Energy efficiency is very important in mobile ad hoc networks (MANETs). Most clustering algorithms save energy by limiting the maximum size of the cluster, by reducing control overhead for maintaining clusters, or by reducing power consumption of intra-cluster communication. These algorithms usually update the intra-cluster routing information and maintain clusters by periodically sending out beacons. This paper proposes to save energy not only by reducing the unnecessary flooding used to update the intra-cluster routing information, but also by balancing power consumption among nodes and clusters throughout the network. We first propose a method to assess the mobility rate of the nodes by sensing the difference in node ID records in a CH between two successive beacons. The beacons will then be adaptively sent out to update the intra-cluster routing information according to these assessed mobility rates, so that the unnecessary flooding is significantly reduced, thereby, resulting in higher energy efficiency. Furthermore, the cluster sizes are adaptively maintained between the maximum and the minimum sizes according to the mobility rates to better balance power consumption among the clusters. Preliminary simulation results show that the proposed algorithm indeed sends out beacon messages adaptively and balances power consumption among clusters. [C988]

"A Novel Disk Layout Optimization for Networked Storage Systems"

To achieve energy-conservation and prompt responses simultaneously, in this paper we propose a novel energy-saving data placement strategy, called striping-based energy-aware (SEA), which can be applied to RAID-structured storage systems to noticeably save energy while providing quick responses. Further, to illustrate the effectiveness of SEA, we implement two SEA-powered RAID-based data placement algorithms, SEA0 and SEA5, by incorporating the SEA strategy into RAID-0 and RAID-5, respectively. Extensive experimental results demonstrate that compared with three well-known data placement algorithms greedy, SP, and HP, SEAO and SEA5 reduce mean response time on average at least 52.15% and 48.04% while saving energy on average no less than 10.12% and 9.35%, respectively. [C989]

"A Design and Implementation of Low Power Management for Personal Multimedia Systems"

To reduce the power consumption of portable devices, many researches have been conducted on the dynamic voltage scaling(DVS) and dynamic power management(DPM). Embedded systems such as DMBs, PMPs and PDAs require long battery life without reducing their performance. Also, power consumption is the most important factor in ubiquitous environment. Most researches are focused on power saving methods by hardware circuits. One of them is DVS, which has proven as a highly effective technique to reduce dynamic power consumption. But, software design and control should be considered to minimize the total energy consumption. This paper presents a power management design and implementation for embedded multimedia systems by guaranteeing QoS. The implemented results show that the system saves the total power consumption up to 5% compared with the DVS on the experiment board. [C990]

"An Error-aware and Energy Efficient Routing Protocol in MANETs"

The network lifetime is a key design factor of mobile ad-hoc networks (MANETs). To prolong the lifetime of MANETs, one is forced to attain the tradeoff of minimizing the energy consumption and load balancing. In MANETs, energy waste resulting from retransmission due to high frame error rate (FER) of wireless channel is significant. In this paper, we propose a novel protocol termed error-aware candidate set routing protocol (ECSRP). ECSRP chooses a route in a candidate subset in the route cache in which all the nodes have enough residual battery power. This approach avoids overusing certain routes. If multiple routes exist in the candidate set, ECSRP employs a metric achieving the tradeoff between energy-efficiency and load balancing to select the optimal route. It also takes channel condition into consideration by incorporating packet loss probability in the computation of energy consumption. This helps to reduce the number of retransmissions and save energy. We evaluate the performance of ECSRP under the Gilbert error model. Simulation results demonstrate that ECSRP outperforms the representative protocol conditional min-max battery cost routing (CMMBCR) protocol in terms of total energy consumption and load balancing. [C991]

"An Energy-Efficient Scheduling Algorithm Using Dynamic Voltage Scaling for Parallel Applications on Clusters"

In the past decade cluster computing platforms have been widely applied to support a variety of scientific and commercial applications, many of which are parallel in nature. However, scheduling parallel applications on large scale clusters is technically challenging due to significant communication latencies and high energy consumption. As such, shortening schedule length and conserving energy consumption are two major concerns in designing economical and environmentally friendly clusters. In this paper, we propose an energy-efficient scheduling algorithm (TDVAS) using the dynamic voltage scaling technique to provide significant energy savings for clusters. The TDVAS algorithm aims at judiciously leveraging processor idle times to lower processor voltages (i.e., the dynamic voltage scaling technique or DVS), thereby reducing energy consumption experienced by parallel applications running on clusters. Reducing processor voltages, however, can inevitably lead to increased execution times of parallel task. The salient feature of the TDVAS algorithm is to tackle this problem by exploiting tasks precedence constraints. Thus, TDVAS applies the DVS technique to parallel tasks followed by idle processor times to conserve energy consumption without increasing schedule lengths of parallel applications. Experimental results clearly show that the TDVAS algorithm is conducive to reducing energy dissipation in large-scale clusters without adversely affecting system performance. [C992]

"A Novel MAC Approach to Combating Fading Channel for Wireless Sensor Networks"

Networking together hundreds or thousands of small and cheap wireless sensor nodes requires highly energy-aware communication protocols at each layer, and much research work has been done to address this issue. However, the time-varying nature of the wireless channel also has a significant influence on the communication energy consumption, and this has long been ignored in most existing state-of-the-art energy saving protocols, thus resulting in unnecessary waste of precious battery energy. Due to this, to judiciously handle the energy management, we propose a channel adaptive energy management protocol, namely, CAEM, that can exploit this time-varying property of the wireless link, by leveraging on the synergistically cross-layer interaction between physical and MAC layers. Specifically, in CAEM, by using a previously proposed adaptive channel coding and modulation scheme, which allows a sensor terminal to dynamically adjust the data throughput via changing the amount of error protection incorporated, sensor node can intelligently access the wireless medium, according the current wireless link quality, estimated available bandwidth, and the traffic load, to realize an efficient utilization of the energy. Thus through a jointly cross layer design across the MAC layer and physical layer, CAEM can reduce the energy consumption as much as 30%, compared with traditional protocols without channel adaptation. Moreover, extensive simulation shows that CAEM is more efficient in channel utilization, in that higher network throughput is realized under heavy traffic load. [C993]

"Energy-Aware Scheduling Tasks on Chip Multiprocessor"

This paper presents a two-stage energy-aware schedule strategy to solve the problem of effective scheduling task set with interdependence on chip multiprocessor (CMP) system while saving energy. We propose a tri-dimensional coding based hybrid genetic algorithm (TCH) to allocate the task set on processor cores to minimize the execution time. Compared with traditional genetic algorithm, TCH uses the tri-dimensional coding scheme to match the architectural characteristics of CMP. We represent a heuristic algorithm using dynamic voltage scaling (DVS) method to reduce the system energy consumption. The simulation experimental results demonstrate that the strategy proposed in this paper efficiently allocates and schedules the tasks on CMP system. [C994]

"Power Management of Multicore Multiple Voltage Embedded Systems by Task Scheduling"

We study the role of task-level scheduling in power management on multicore multiple voltage embedded systems. Multicore on-a- chip, in particular DSP systems, can greatly improve performance through parallelism. On the other hand, dynamic voltage scaling (DVS) has been shown to be one of the most effective low power design techniques and multiple supply voltage system is among the most practical and well-studied DVS systems. The integration of multiple cores/processors on a chip naturally makes the system suitable for DVS with new innovations such as voltage island. In this paper, we discuss how to reduce multicore system's power consumption by utilizing multiple supply voltages. We first formulate the power management problem for multicore multi-voltage embedded systems and show that the problem is NP-hard, but the NP- hardness can be removed for several real life applications. More specific, we develop polynomial algorithms to find the optimal solutions for two special cases. The first case is when preemption is allowed, and the second one is when the system uses the first-come-first-serve (FCFS) service strategy. We prove both algorithms' optimality and analyze their run-time complexity. Simulation on real- life and randomly generated tasks show that the optimal preemption scheduler provides significant energy saving. Our goal in this paper is to build a solid foundation for the power management problem on multicore multiple voltage systems and to study real life applications where the problem can be solved optimally. [C995]

"ESTREL: Transmission and Reception Energy Saving Model for Wireless Ad Hoc Networks"

Multimedia streaming over ad hoc networks forms a continuous progress domain due to users' growing needs and wireless devices incessant evolution. Our objective, in this study, is to increase individual wireless nodes lifetime by a saving energy model based on video transmission/reception which allows increasing the ad hoc network lifetime. When arriving at a predefined threshold, we reduce the number of multimedia transmitted/received packets by exploiting the MPEG4 enhancement layers. In our proposal we optimize the tradeoff between the energy consumption and the perceived video quality. Simulation results show that we outperform the conventional approach by increasing the overall network lifetime. [C996]

"CPU MISER: A Performance-Directed, Run-Time System for Power-Aware Clusters"

Performance and power are critical design constraints in today's high-end computing systems. Reducing power consumption without impacting system performance is a challenge for the HPC community. We present a runtime system (CPU MISER) and an integrated performance model for performance-directed, power-aware cluster computing. CPU MISER supports system-wide, application-independent, fine-grain, dynamic voltage and frequency scaling (DVFS) based power management for a generic power-aware cluster. Experimental results show that CPU MISER can achieve as much as 20% energy savings for the NAS parallel benchmarks. In addition to energy savings, CPU MISER is able to constrain performance loss for most applications within user-specified limits. These constraints are achieved through accurate performance modeling and prediction, coupled with advanced control techniques. [C997]

"An Adaptive Energy-Efficient and Low-Latency Mac Protocol for Wireless Sensor Networks"

In this paper, an adaptive energy-efficient and low-latency MAC (L-MAC) protocol for wireless sensor networks is proposed. In this protocol, nodes have three modes-sleeping, receiving and sending. Each node goes to sleep periodically to save energy. L-MAC delays the receiving and sending period hop by hop, so that when one node is in sending mode, its lower-hop node is in receiving mode. After receiving a message from upper- hop node, each node can transmit it to lower-hop node in the sequent sending period. Therefore, the multi-hop end-to-end delay due to periodical sleeping is reduced greatly. Furthermore, an adaptive sleeping scheme which makes the nodes with lower traffic have longer time to sleep is adopted to save more energy. Simulation results show that L-MAC achieves lower energy consumption and latency than traditional contention-based protocols. [C998]

"Energy Conservation in Large-Scale Sensor Networks through Wakeup Mechanism and

Clustering Aggregation"

To lengthen the lifetime of the sensor network significantly, a node should turn off its radio most of the time, expect when it has to participate in data forwarding. We propose an asynchronous wakeup mechanism, which efficiently wakes up nodes while transmission or monitoring the channels based on the concept of the grid-based quorum (GQMA). Next, we consider a simplified clustering mode for a sensor network integrated GQMA. All the nodes are in the power-saving modes following the wakeup mechanism discussed above except getting the TDMA schedule from a clusterhead (CH). Compared with other hierarchical clustering algorithms, our protocol can achieve more power conservation on the phases of cluster formation and routing tree setup by reducing idle listening time and does not demand clock synchronization between the nodes. Simulation results show that the proposed protocols have good performances in the aspects of energy conservation and efficiency. [C999]

"FlexFetch: A History-Aware Scheme for I/O Energy Saving in Mobile Computing"

Extension of battery lifetime has always been a major issue for mobile computing. While more and more data are involved in mobile computing, energy consumption caused by I/O operations becomes increasingly large. In a pervasive computing environment, the requested data can be stored both on the local disk of a mobile computer by using the hoarding technique, and on the remote server, where data are accessible via wireless communication. Based on the current operational states of local disk (active or standby), the amount of data to be requested (small or large), and currently available wireless bandwidth (strong or weak reception), data access source can be adaptively selected to achieve maximum energy reduction. To this end, we propose a profile-based I/O management scheme, FlexFetch, that is aware of access history and adaptive to current access environment. Our simulation experiments driven by real-life traces demonstrate that the scheme can significantly reduce energy consumption in a mobile computer compared with existing representative schemes. [C1000]

"ALT-DVS: Dynamic Voltage Scaling with Awareness of Leakage and Temperature for Real-Time Systems"

The increasing leakage power and chip temperature in microprocessors are adversely affecting the performance and power consumption in real-time embedded systems. However, the traditional dynamic voltage scaling (DVS) technique, a popular and effective low-power design method, does not include the leakage and temperature impacts. In this work, we consider these two impacts when designing DVS-enabled real-time systems. We study the following problems: how to achieve the maximum computation and how to achieve a given amount of computation with the minimum total energy with the leakage and temperature variance available. The enhanced DVS technique ALT-DVS we proposed leverages the on-chip temperature sensor and the established system-level thermal model to determine the appropriate operating voltage and frequency for a given task, such that each task can be completed before its deadline while the system does not overheat. Our simulation results show that ALT-DVS not only saves more than 20% total energy over pure DVS technique, but also reduces the number of tasks that cannot be completed by DVS due to system overheat. [C1001]

"Proposal of VLIW Architecture for Application Specific Processors with Built-in-Self-Repair facility via Variable Accuracy Arithmetic"

A new proposal of a very long instruction word (VLIW) architecture for application specific processors with the built-in-self-repair (BISR) facility realized by means of the variable accuracy arithmetic has been described in this paper. The proposed idea, which is particularly interesting for the portable embedded systems, is based on a novel two accumulator model, which is used in order to obtain high accuracy of the result of a series of floating-point additions. The goal of the proposed approach consists in ensuring the functionality of the system even in case of permanent faults of particular building blocks, e.g., of one of the floating point adders. Instead of decreasing the performance of the system or providing redundant hardware, as it is typically done in other approaches, in our present concept merely the accuracy of the floating point accumulation is reduced. Therefore, although the quality of service is reduced, the performance and the overall functionality of the system may remain unchanged. By this means we can also control the power consumption, saving the power with the cost of the somehow reduced signal processing accuracy. [C1002]

"An Efficient Message Distribution Scheme for Data Query in Sensor Networks"

In sensor networks, a data query can be named according to the physical attributes, and is generally diffused throughout the network to retrieve sensor data. However, the direct distributions of queries into the network will cause a large traffic overhead and high energy consumption. In this paper, we propose a localized query forwarding scheme based on the processing of query's name. In contrast to the conventional distributions of data query message, a query's name is resolved into the IDs of corresponding group of sensor nodes before being distributed to the network. Therefore, the query is efficiently forwarded into the network within a localized area.

The proposed approaches highly reduce the query overhead in the network and save the energy consumption of sensor nodes. [C1003]

"Investigation of Reconfigurability for the Digital Backend of Ultra Wideband Receiver"

The next generation Wireless Personal Area Network and Wireless Sensor Network applications demand portability and ultra low power operation. Ultra Wideband communication has the potential to achieve these requirements due to possibility of digital implementation. The mostly digital UWB radio is designed to cope up with worst case channel condition and uses heavy parallelism in the digital backend leading to high power consumption during acquisition and synchronisation mode. However, for UWB pulse propagation, the wireless channel and time delay may vary due to various factors. This paper analyses the effect of different channel impulses and time delays on the required parallel hardware for receiver processing. This analysis is performed in order to investigate the real time reconfigurability approach for the digital UWB receiver in order to save power. The analysis shows that introduction of reconfigurability has a potential to reduce power consumption. [C1004]

"Shared Infrastructure Power Saving for Solar Powered IEEE 802.11 WLAN Mesh Networks"

Solar powered WLAN infrastructure is a cost effective option in outdoor deployments where continuous power sources are not practical. In these nodes the cost of the solar panel and battery can be a significant fraction of the total, and therefore reducing access point power consumption is very important. In this type of network, peak bandwidth requirements may not be satisfied by a single access point radio, even though long term average bandwidth requirements may be very low. In this case multiple radio APs or overlapped AP coverage deployment is required to meet this peak demand. When this happens the long term power consumption of the nodes can be reduced by implementing shared dynamic power saving between the WLAN mesh nodes. In this paper we propose and evaluate two algorithms for efficiently activating the solar powered infrastructure when additional bandwidth is needed. The algorithms are designed to be compatible with the existing IEEE 802.11 standard and include conventional load balancing when more than one AP is active in a given coverage area. We demonstrate that the proposed algorithms can significantly reduce the power consumption of the shared solar powered infrastructure. [C1005]

"Hybrid Energy-Saving Algorithm Considering Silent Periods of VoIP Traffic for Mobile WiMAX"

Recent broadband wireless access systems apply voice over Internet protocol (VoIP) for their voice services, so a mobile station (MS) requires an efficient energy-saving algorithm for VoIP services to prolong its battery lifetime. The IEEE 802.16e system called MobileWiMAXprovides the power saving class (PSC) of type II as an energy-saving algorithm for VoIP service, but it is not originally designed to consider silent periods of VoIP traffic. Therefore, we propose a new hybrid energy-saving algorithm suitable for VoIP services with silence suppression, which basically follows PSC II during talk-spurt periods, but uses the truncated binary exponential algorithm of PSC I during silent periods. The analysis and simulation results show that the proposed hybrid scheme reduces power consumption effectively during silent periods while satisfying the maximum allowable end-to-end delay and low packet drop probability constraints with respect to the quality of service (QoS) of VoIP. [C1006]

"A Location Independent and Coverage Efficient Protocol for Wireless Sensor Networks"

In wireless sensor networks (WSN), sensor nodes are powered by batteries. To make efficient use of battery energy is critical to sensor network lifetime. When targets are redundantly covered by multiple sensors, especially in randomly deployed sensor networks, it is possible to save battery energy by organizing sensors into mutually exclusive subsets and alternatively activating only one subset at a time. To solve this problem, the relationship between the desired QoS requirement and the minimum number of active nodes is analyzed in the randomly deployed sensor networks. We propose a location independent and coverage efficient (LICE) protocol for WSN based on our analytical results. The protocol selects the minimum number of active nodes based on their energy and previous working status without using any location information. Simulation and analysis demonstrate that our LICE protocol not only reduces the energy consumption of sensor nodes and increases the network lifetime, but also balances the energy dissipation among nodes. [C1007]

"Real-Time Loop Scheduling with Leakage Energy Minimization for Embedded VLIW DSP Processors"

In this paper, we develop a novel real-time instruction-level loop scheduling technique to reduce leakage energy consumption for applications with loops on VLIW architecture. We first prove that the scheduling problem with the minimum leakage energy consumption within a timing constraint is NP-complete. Then, LEMLS (leakage energy minimization loop scheduling) algorithm is designed to repeatedly regroup a loop based on rotation

scheduling (Chao et al., 1997), and decrease leakage energy integrating with leakage power reduction mechanism. We conduct experiments on a set of DSP benchmarks based on the power model of the VLIW processors in (Liao et al., 2002). The results show that our algorithm achieves significant leakage energy saving compared with list scheduling and the algorithm in (You et al., 2006). [C1008]

"A Protocol Enhancement for IEEE 802.11 Distributed Power Saving Mechanisms No Data Acknowledgement"

Mobile devices including wireless LAN functionality are becoming increasingly popular in society. The wide range of products available in the market target different customer needs but most of them should meet two main requirements: QoS support for differentiating real-time services from non real-time and power saving functionality to achieve an operating time according to users' expectations. The devices presenting the most challenging technical issues to meet these two requirements are dual-mode handsets (cellular/WLAN) because of their mandatory support of a strict QoS demanding application, VoIP, and their small device size which severely limits the battery capacity. The focus of our work in this paper is the design and evaluation of an enhancement of the distributed wireless LAN power saving mechanisms defined in the IEEE 802.11 and 802.11e standards, no data acknowledgment (NDACK). The objective of NDAck is to increase the battery lifetime of wireless LAN mobile devices while providing the required QoS. The protocol improvement designed has been implemented in OPNET to evaluate the performance enhancements obtained. Our results show that (i) NDAck significantly reduces the power consumption of stations running real-time applications, (ii) the larger the power consumption due to the congestion in the wireless channel the larger the power consumption reduction with NDAck and (iii) NDAck results in a considerable QoS improvement for real-time applications. [C1009]

"Energy Effective Time Synchronization inWireless Sensor Network"

Advance in processor, memory and wireless communication technique have led to an increase of economical and small wireless sensor nodes. To provide the right responses quickly for the diverse events, wireless sensor nodes have cooperation with together. For successful cooperation, the time synchronization among sensor nodes is an important requirement for application execution. In wireless sensor networks, message packets are used for the time synchronization. However, the transmission of message packets dissipates the battery energy of wireless sensor nodes. Since wireless sensor nodes works on the limited battery capacity, the excessive use of message packets has a negative impact upon their lifetime. In this paper, reference interpolation protocol is proposed for reducing the number of message packets for the time synchronization. The proposed method performs time interpolation between the time of reference packets and the global time of the base station. The proposed method completes the synchronization operation with only two message packets. Due to the simple synchronization procedure, our method greatly reduces the number of synchronization messages. From the decrease in the transmission of message packets, the convergence time among wireless sensor nodes is shortened and the lifetime of wireless sensor nodes is also prolonged as much as the amount of saved battery energy. [C1010]

"Branch Prediction and Power Reduction Techniques in the Clustered Loop Buffer VLIW Architecture"

The clustered loop buffer VLIW processor has been developed to enhance the performance of multimedia applications in which loop intensive codes are used. In this paper, we employ a dynamic branch predictor in the clustered loop buffer VLIW architecture to handle branch instructions in loop-rich codes, such as multimedia applications, via dynamic speculation. To reduce the energy consumption we map two power reduction techniques, which are hint instruction method and pipeline gating method, on the architecture and analyze their performances using MediaBench applications. In our experiment, we observed that the hint instruction method helps reducing the dynamic branch predictor usage for all the applications tested, by at least 70%. The pipeline gating method was observed to be beneficial to only a subset of the applications with up to 20% of savings. [C1011]

"Empirical Analysis of Transmission Power Control Algorithms for Wireless Sensor Networks"

Previously, many researchers sought to optimize the throughput and power consumption by radio transmission power control, but the experimental platforms and the workloads did not reflect the reality of WSNs. We present a dynamic transmission-power-control algorithm based on previous studies and evaluate the algorithm using realistic multi-hop WSN workloads and a large Mica2dot-based testbed. We have found that potential gains of dynamic transmission-power control are much smaller than what is indicated by prior research. Compared to the fixed transmission-power control, the dynamic transmission-power control improves the power consumption up to 16% for convergence traffic, but no noticeable performance improvements for aggregation traffic. The effect of

dynamic transmission-power control becomes larger as we reduce the radio duty cycle, with 37% power savings at a 10% duty cycle. This result suggests that dynamic transmission-power control is most useful in combination of low-power MAC protocols which implement radio low duty cycling. [C1012]

"Critical-Path based Low-Energy Scheduling Algorithms for Body Area Network Systems"

In this paper, we propose novel low-energy scheduling algorithms with low computational complexities for the heterogeneous body area network (BAN) systems, considering task graphs with deadlines (timing constraints) and precedence relationships to satisfy. Our proposed novel scheme, referred to as "critical-path information track-and-update", analyses the critical-paths, identifies the slack and distributes it over tasks such that the overall energy consumption is minimised. Our dynamic scheduling algorithm utilises the results from the static scheduling algorithm and attempts to aggressively reduce the energy consumption. Simulations for the task graph for a typical BAN application show that our static and dynamic scheduling algorithms deliver 25% and 15% more energy savings respectively compared to typical slack reclamation based scheduling algorithms. [C1013]

"Multi-Speed DVS Algorithms for Periodic Tasks with Non-Preemptible Sections"

Reducing energy consumption is important for mobile embedded systems and one of its solutions is dynamic voltage scaling (DVS). In this paper, we examine how to achieve further energy saving for periodic real-time tasks with non-preemptible sections on EDF algorithm by using DVS. Previous algorithms use two speed levels to deal with run-time blocking situation. However, this paper proposes a multi-speed algorithm that exploits various speed levels depending on specific blocking situation to minimize energy consumption. Moreover, it also presents an enhanced multi-speed algorithm that further reduces the energy dissipation by dropping the speed level early and considering only remaining blocking time to compute a lower speed. We induced feasibility conditions for our algorithms and proved them. The experiments show that proposed algorithms achieve up to 70.8% energy saving compared to previous algorithms. [C1014]

"Hierarchical Node Clustering Approach for Energy Savings in WSNs"

This paper proposes an energy efficient clustering algorithm for self-organizing and self-managing WSNs, called SNOW cluster. It introduces region node selection as well as cluster head election based on the residual battery capacity of nodes to reduce the costs of managing sensor nodes and of the communication among them. SNOW cluster clusters periodically to select cluster heads that are richer in residual energy level, compared to the other nodes to achieve load balancing and extend the lifetime of every individual sensor nodes. After the cluster heads are selected, SNOW cluster selects the region nodes in the cluster heads based on the energy level of them and chooses gateway nodes between clusters based on their location information. The effectiveness of the proposed SNOW cluster algorithm is validated through actual implementation and simulation using ns-2. The simulation results reveal that the proposed framework allows smaller energy consumption for network management and longer network lifetime than the existing schemes such as LEACH and LEACH-C for practical size networks. [C1015]

"A 256Γ́B—128 Energy-Efficient TCAM with Novel Low Power Schemes"

Novel low power schemes for energy-efficient ternary content-addressable memory (TCAM) are presented in this paper. The butterfly match-line scheme is based on the pseudo-footless clock-data pre-charged architecture. It connects each pipelined stage in a butterfly style which significantly decreases both search time and power consumption. For applications like IP-address forwarding in a network router, a new don't-care based power gating and don't-care based hierarchical (DCBH) search-line scheme are proposed. The search-line is divided into global search-line (GSL) and local search-line (LSL) which is controlled by don't-care state in DCBH search-line scheme. Therefore, the power consumption on search line is reduced without any search time overhead. Besides, the power saving of the standby power is achieved by power gating technique. The proposed 256 times 128 bit TCAM has been implemented with TSMC 0.13 um CMOS technology. It shows 0.55 ns of match evaluation time on search operation with 0.29 fJ/bit/search of energy efficiency. [C1016]

"A 65-nm pulsed latch with a single clocked transistor"

This paper discusses the technology limits placed on the clock switching energy in sequential elements. It proposes a novel pulsed latch that uses a single clocked transistor and consumes close to ten times less clock power than a conventional latch using six clocked transistors. It describes how the new circuit enables additional power savings when virtual grounds, instead of a regular clock, are locally distributed to a group of latches. Finally, the paper discusses how to further reduce the dynamic clock power consumption of the new latch without degrading its timing by feeding it a low-swing clock. [C1017]

"Mobility Aware Transmission Power Control in Mobile Ad-hoc Network"

The energy efficient algorithm which saves network energy consumption by reducing transmission range in static networks cannot maintain the energy efficiency in dynamic networks because of link failure by node mobility and asymmetric links. So we present MATPC which keeps 20% better energy efficiency compare to other approaches in dynamic networks [C1018]

"Noise-Direct: A Technique for Power Supply Noise Aware Floorplanning Using Microarchitecture Profiling"

This paper proposes noise-direct, a design methodology for power integrity aware floorplanning, using microarchitectural feedback to guide module placement. Stringent power constraints have led microprocessor designers to incorporate aggressive power saving techniques such as clock-gating, that place a significant burden on the power delivery network. While the application of extensive clock-gating can effectively reduce power consumption, unfortunately, it can also induce large inductive noise (di/dt), resulting in signal integrity and reliability issues. To combat these problems, processors are usually designed for the worst-case current consumption scenario using adequate supply voltage and decoupling capacitances. To tackle high-frequency inductive noise and potential IR drops, we propose a novel design methodology that integrates microarchitectural profiling feedback into the floorplanning process. We present two microarchitectural metrics to quantify the noise susceptibility of a module:self weighting and correlation weighting. By using these metrics in a force-directed floorplanning algorithm to assign power pin affinity to modules, we can quickly converge to a design for average-case current consumption. By designing for the average-case and employing dynamic di/dt control for the worst-case, we can ensure that a chip is noise-tolerant without exceeding decap budget constraints. Our observations showed that certain functional modules in a processor exhibit consistent and highly correlated switching activity, that can be used to guide module placement distance from power pins. The experimental results demonstrate that the force-directed floorplanning technique can effectively suppress supply noise experienced by modules, reduce the total number of supply-noise margin violations, and achieve a floor-plan with considerably lower IR drop, as compared to a wire-length driven floorplan. [C1019]

"Energy-efficient and performance-enhanced disks using flash-memory cache"

This work explores the unique characteristics of flash memory in serving as a cache layer for disks. The experiments show that the proposed management scheme could save up to 20% energy consumption while reduce the read response time by the two third and the write response time by the five sixth of their counterparts. The estimated lifetime of the flash-memory cache is significantly improved as well. [C1020]

"Lookup Table-Based Adaptive Body Biasing of Multiple Macros"

A reduced supply voltage must be accompanied by a reduced threshold voltage, which makes this approach to power saving susceptible to process variation in transistor parameters, as well as resulting in increased subthreshold leakage. The paper propose a new adaptive body biasing scheme, based on a lookup table for independent control of multiple functional blocks on a chip, which controls leakage and also compensates for process variation at the block level. An adaptive body bias is applied to blocks in active mode and a large reverse body bias is applied to blocks in standby mode. This is achieved by a central body bias controller, which has a low overhead in terms of area, delay, and power consumption. The problem of optimizing the required set of bias voltages is formulated and solved. A design methodology for semicustom design using standard-cell elements is developed and verified with benchmark circuits [C1021]

"Dynamic voltage frequency scaling for multi-tasking systems using online learning"

This paper presents an extremely lightweight dynamic voltage and frequency scaling technique targeted towards modern multi-tasking systems. The technique utilizes processors runtime statistics and an online learning algorithm to estimate the best suited voltage and frequency setting at any given point in time. We implemented the proposed technique in Linux 2.6.9 running on an Intel PXA27x platform and performed experiments in both single and multi-task environments. Our measurements show that we can achieve the maximum energy savings of 49% and reduce the implementation overhead by a factor of 2 when compared to state of the art techniques. [C1022]

"Minimizing power dissipation during write operation to register files"

This paper presents a power reduction mechanism for the write operation in register files (RegFiles), which adds a conditional charge-sharing structure to the pair of complementary bit-lines in each column of the RegFile.

Because the read and write ports for the RegFile are separately implemented, it is possible to avoid pre-charging the bit-line pair for consecutive writes. More precisely, when writing same values to some cells in the same column of the RegFile, it is possible to eliminate energy consumption due to precharging of the bit-line pair. At the same time, when writing opposite values to some cells in the same column of the RegFile, it is possible to reduce energy consumed in charging the bit-line pair thanks to charge-sharing. Motivated by these observations, we modify the bit-line structure of the write ports in the RegFile such that i) we remove per-cycle bitline pre-charging and ii) we employ conditional data dependent charge-sharing. Experimental results on a set of SPEC2000INT / MediaBench benchmarks show an average of 61.5% energy savings with 5.1% area overhead and 16.2% increase in write access delay. [C1023]

"Improving disk reuse for reducing power consumption"

Power consumption of disk systems is an important issue in scientific computing where data-intensive applications exercise disk storage extensively. While one can spin down idle disks when idleness is detected, spinning up them takes many cycles and consumes extra power. Therefore, it can be very useful in practice to improve disk reuse, that is, using the same set of disks as much as possible. If this can be achieved, unused disks can be held in the so called spin-down mode for longer durations of time, and this helps increase power savings. This paper proposes an approach for reducing disk power consumption by increasing disk reuse. The proposed approach restructures a given application code considering the disk layouts of the datasets it manipulates. We implemented this disk layout-conscious approach within a publicly-available compilation framework and compared it against a conventional data reuse optimization approach (which is also implemented using the same compiler) using six scientific applications that perform disk I/O. The results collected so far indicate that our layout-conscious approach and the conventional data reuse optimization approach reduce the disk energy consumption by 25.3% and 10.3%, respectively, on average, over the case where no disk power optimization is applied. The corresponding savings in total energy consumption (including CPU, memory and network energies) are 6.5% for the conventional approach and 16.5% for our disk layout-conscious approach. Our experimental evaluation also shows that the savings obtained are consistent with varying number of disks and alternate disk layouts. [C1024]

"A reusability-aware cache memory sharing technique for high-performance low-power CMPs with private L2 caches"

Chip multiprocessors (CMPs) emerge as a dominant architectural alternative in high-end embedded systems. Since off-chip accesses require a long latency and consume a large amount of power, CMPs are typically based on multiple levels of on-chip cache memories. To meet the performance demand and power budget, an efficient support for memory hierarchy is important. We propose an on-chip L2 cache organization which takes advantage of both a private L2 cache and a shared L2 cache to improve the performance and reduce energy consumption. Our L2 cache organization is based on a private L2 cache organization which has the short access latency. When a cache block in the private L2 cache is selected for an eviction, our proposed organization first evaluates the reusability of the cache block. If the cache block is likely to be reused, we save the evicted cache block in one of peer L2 caches which may have efficiently invalid blocks. By selectively writing evicted cache blocks to peer L2 caches, the proposed L2 cache organization can effectively simulate a shared L2 cache. Experimental results using a CMP simulator showed that the proposed L2 cache organization improved the average memory latency by up to 27% and reduced energy consumption by up to 16.6% over a 256KB private L2 cache organization for the SPLASH2 benchmark programs.. [C1025]

"Optimising calciner burners: Theoretical treatment of turbulent diffusion jets in cross flow"

For the cement industry one of the ways of reducing specific fuel consumption, which, is the major cost component in cement production, is the flame control. Controlling the flames in a precise manner results not only in specific fuel consumption savings, but also in maintaining longer refractory life and better quality. An understanding of the aerodynamic aspect of the flames is important in controlling the shape and length of the flame, achieving good fuel/air mixing and recirculation, which are essential in preventing a poor flame and inefficient combustion. Energy losses can occur as a result of incomplete combustion, which manifests itself as CO presence in exhaust gases due to poor fuel/air mixing, as well as long flames. Positioning of the flames in a symmetrical manner both in the rotary kiln and the secondary firing units/calciners is also essential for uniform distribution of heat transfer which results in better heat transfer between the material and hot gas, as well as prevention of flame impingement on the refractory. Flames encountered in cement manufacturing processes are of the turbulent diffusion type. Rotary kiln flame can be described as a long enclosed turbulent jet passing into a turbulent co-flowing stream constrained by a circular duct. The flames in the secondary firing units or calciners are mostly described as short semi-free turbulent diffusion jets in cross flow. In order to study the properties and behaviour of the auxiliary or calciner flames, which are short, impinging, semi-free, turbulent diffusion jet flames

in cross flow, the theory and isothermal modelling of the turbulent jets injected at an angle into the main stream can be applied. An empirical equation was developed to describe the behaviour of the turbulent jets in cross flow which can be used to predict the position of the axis of such jets, which, are the flames in calciners or riser ducts of the cement kilns. By modifying the discharge conditions of the jet or mainstream p--roperties, the flames can be positioned in the desired configuration for better fuel/air mixing and heat transfer conditions. Calciner burners can be designed for optimum flame configuration and combustion conditions in the calciners and the secondary firing units where the turbulent jets in cross flow theory is applicable. The empirical equation developed was used to predict the jet paths of the auxiliary firing flames . The acid/alkali physical modelling technique was also used to simulate the same auxiliary flames under same conditions to check the accuracy and validity of the theoretical method. Results showed that both the theoretical method and the experimental method agreed well with each other in determining the jet axis of the turbulent diffusion flames in cross flow [C1026]

"Compiler-Directed Functional Unit Shutdown for Microarchitecture Power Optimization"

Leakage power is a major concern in current microarchitectures as it is increasing exponentially with decreasing transistor feature sizes. In this paper, we present a technique called functional unit shutdown to reduce the static leakage power consumption of a microprocessor by power gating functional units when not used. We use profile information to identify functional unit idle periods that is used by the compiler to issue corresponding OFF/ON instructions. The decision to power gate during idle periods is made based on the comparison between the energy consumed by leaving the units ON and the overhead and leakage energy involved in power cycling them. This comparison identifies short idle periods where less power is consumed if a functional unit is left ON rather than cycling the power during that period. The results show that this technique saves up to 18% of the total energy and between 4 and 11% on average with a performance degradation of 1%. [C1027]

"Integrating Power Management into Distributed Real-time Systems at Very Low Implementation Cost"

The development cost of low-power embedded systems can be significantly reduced by reusing legacy designs and applying proper modifications to meet the new power constraints. The proposed power management techniques in the literature for implementing distributed power managers in multi-processor systems are very costly in terms of hardware and software modifications. For example, extra software code for power management must be integrated into each component of the system. Furthermore, in order to turn on a component at a specific time/event, extra hardware timers and interrupt controllers must be added to each component along with proper software/device driver modifications. In this paper, we propose a new centralized power management technique that reduces the power consumption of distributed realtime systems at very low implementation cost. Our power manager does not need software and hardware modifications of each individual component. Instead, it uses the model of the system/application to compute the schedule of turning on/off commands by dynamically simulating the system for a given application scenario. The dynamic simulation can be conservative to reflect the jitter in arrival time of events and/or variation in execution delay of tasks. We applied our power management technique to a distributed software-defined radio system and achieved significant energy savings (60% to 87%) at the cost of 1% energy consumed by the power manager itself, as verified by actual hardware measurements. Furthermore, our power manager reacts to the changes in application scenario (referred to as mission) within milliseconds. [C1028]

"A Hybrid Disk-Aware Spin-Down Algorithm with I/O Subsystem Support"

To offset the significant power demands of hard disk drives in computer systems, drives are typically powered down during idle periods. This saves power, but accelerates duty cycle consumption, leading to earlier drive failure. Hybrid disks with a small amount of non-volatile flash memory (NVCache) are coming on the market. We present four I/O subsystem enhancements that exploit the characteristics of hybrid disks to improve system performance: 1) artificial idle periods, 2) a read-miss cache, 3) anticipatory spin-up, and 4) NVCache write-throttling. These enhancements reduce power consumption, duty cycling, NVCache block-erase impact, and the observed spinup latency of a hybrid disk, resulting in lower power consumption, greater reliability, and faster I/O. [C1029]

"Reducing ALU and Register File Energy by Dynamic Zero Detection"

Register files and ALU are dominant energy consumers in the datapath of typical pipelined processors. Reducing energy consumption of these components has a big impact on processor energy budget. Consequently, several techniques have been proposed at circuit and architectural levels. In contrast, we propose a dynamic zero detection technique for reducing energy in the register files and ALU in this paper. We find that zero is the most frequent value used in the register files and ALU. When a register value is determined to be zero before reading

a register file, an access to the register file is prevented to save energy and zero is directly provided to the datapath. When one of operand register values of an add instruction is zero, it is prevented from being executed on ALU since its result is just the value of the other operand register. Since adds/subs constitute most of arithmetic and logic instructions, this optimization saves large ALU energy. Our dynamic zero detection technique is demonstrated to save 9.0% and 20.2% of energy in the register files and the adder of ALU for SPEC2000 floating-point and integer benchmarks, respectively. [C1030]

"Compiler-Directed Code Restructuring for Operating with Compressed Arrays"

Memory system utilization is an important issue for many embedded systems that operate under tight memory limitations. This is a strong motivation for recent research on reducing the number of banks required during execution of a given application. Reducing memory space requirements of an application can bring three potential benefits. First, if we are to design a customized memory system for a given embedded application, reducing its memory requirements can cut the overall cost. Second, if we are to execute our application in a multi-programmed environment, the saved memory space can be used by other applications, thereby increasing the degree of multiprogramming. Third, it is also possible to reduce the energy consumption in a banked memory system by reducing the amount of memory space occupied by application data and placing the unused banks into low-power operating modes. This paper proposes a novel memory saving strategy for array-dominated embedded applications. The idea is to exploit the value locality in array data (e.g., those from the multi-media domain) by storing arrays in a compressed form to save memory space. Based on the compressed forms of the input arrays, our compiler-based approach automatically determines the compressed forms of the intermediate and output arrays and also automatically restructures the application code so that we can also reduce execution time (by exploiting value locality). Our experimental results show that this scheme is very effective in practice and reduces the memory space requirements of the applications tested by 19% on average. The experimental results also show that the proposed approach reduces the execution cycles of the original codes by 14% on average [C1031]

"Graph-Based Procedural Abstraction"

Procedural abstraction (PA) extracts duplicate code segments into a newly created method and hence reduces code size. For embedded micro computers the amount of memory is still limited so code reduction is an important issue. This paper presents a novel approach to PA, that is especially targeted towards embedded systems. Earlier approaches of PA are blind with respect to code reordering, i.e., two code segments with the same semantic effect but with different instruction orders were not detected as candidates for PA. Instead of instruction sequences, in our approach the data flow graphs of basic blocks are considered. Compared to known PA techniques more than twice the number of instructions can be saved on a set of binaries, by detecting frequently appearing graph fragments with a graph mining tool based on the well known gSpan algorithm. The detection and extraction of graph fragments is not as straight forward as extracting sequential code fragments. NP-complete graph operations and special rules to decide which parts can be abstracted are needed. However, this effort pays off as smaller sizes significantly reduce costs on mass-produced embedded systems [C1032]

"Quantizer Effects on EBCOT Based Compression"

In order to make wavelet based image processing algorithms usable for portable multimedia devices different optimization strategies need to be taken into account. Besides optimizing the hardware structures for better performance, the overall processing load has to be minimized as proposed in this paper. Coarse quantizer steps sizes reduce the entropy and therefore we get shorter code words after the entropy coder. We propose a reduction of the data accuracy in the quantizer, saving up to 28% processing power. Image quality and compression ratio are not compromised. [C1033]

"Power Reduction in VLIW Processor with Compiler Driven Bypass Network"

With the increase in issue width, bypass control of a processor become more complex. Also, in a processor, operands are read both from register file as well as from bypass. For a multi-port register file, read/write energy is much more than that of single port register file. Both redundant register read/write and bypass control area can be reduced with compiler hints for register bypass. In this work we suggest an innovative way to represent compiler bypass hints that serve both these motivations. Further, bypass hints are used in effective design of multi-stage bypass network. Experiments on media-bench benchmarks show that by using our approach: (i) register file energy savings can be as much as 60%; (ii) and synthesis of VLIW core saves 2-4% of the core area [C1034]

"Energy-Aware Tag Anti-Collision Protocols for RFID Systems"

Energy consumption of mobile readers is becoming an important issue as applications of RFID systems pervade different aspects of our lives. Surprisingly, however, these systems are not energy-aware with the focus till date being on reducing the time to read all tags by the reader. The problem of tag arbitration in RFID systems is considered with the aim of trading off time for energy savings at the reader. The approach of using multiple time slots per node of a binary search tree is explored through three anti-collision protocols that aim to reduce the number of colliding responses from tags. This results in fewer reader queries and tag responses and, hence, energy savings at both the reader and tags (if they are active tags). An analytical framework is developed to predict the performance of our protocols, with the numerical evaluation of this framework validated through simulation. It is shown that all three protocols provide significant energy savings when compared to the existing query tree protocol while sharing the deterministic and memoryless properties of the latter [C1035]

"Interframe Bus Encoding Technique for Low Power Video Compression"

This paper proposes a data encoder to reduce switched capacitance on system bus. The method focuses on transferring raw video data (pixels) between off-chip memory and on-chip memory which is common in video compression applications. This method is based on entropy coding to minimize bus transition. The existing technique exploits the correlation between neighbouring pixels. In our technique, pixel correlation between two consecutive frames was exploited. The method shows 54% transition saving when combined with the existing technique which is equivalent to 38% power saving for 15pF off-chip bus capacitance. This method is suitable for applications where multiple frames are transferred from off-chip memories such as in MPEG-4 AVC/H.264 encoder [C1036]

"Customization of Register File Banking Architecture for Low Power"

Register file banking is an effective alternative to monolithic register files in embedded processor based systems. In this work, we propose techniques for performing application specific customization of register file banking structure. First, we propose two techniques based on: (i) profiling; and (ii) static application analysis to arrive at a customized energy-efficient bank configuration for a given application on a dual bank register file. We also propose a technique to extend the exploration to a multi-bank register file architecture and an associated register allocation algorithm for further power reduction. This reduces register file power consumption by allocating variables in frequently accessed basic blocks to separate appropriately sized register file bank of active registers. Experimental results indicate that our customized dual bank configuration inferred by both techniques gives energy savings of 40% over a monolithic register file, and the multi-bank register file customization gives a further 15-20% energy savings [C1037]

"A Phase-Based Self-Tuning Algorithm for Reconfigurable Cache"

The performance of a given cache architecture is largely determined by the behavior of the application using the cache. Reconfigurable cache is an effective low-power technique. Using the technique, microprocessor's cache can be configured dynamically to adapt itself to the requirement of running program, and minimize the energy consumption and performance loss. We introduce a phase-based self-tuning algorithm (PBSTA), which can automatically, transparently, and dynamically manage the reconfigurable cache on a per-phase basis. In contrast with previous works, the algorithm seeks not only to lower the cache's energy consumption effectively, but also reduce the performance loss due to unnecessary reconfigurations. By simulating numerous MiBench benchmarks, the results show that the PBSTA, when applied to reconfigurable cache, saves on average 40% of total memory access energy compared with a conventional cache and the associated performance loss is close to 1.8%. [C1038]

"Compression for Low Power Consumption in Battery-powered Handsets"

Only summary form given.Java has been introduced to the mobile/wireless handsets and Java enabled handsets are now prevalent in the market, showing their successful launch. A variety of attractive services have been developed and promise a lot of fun to our daily lives, which are however targeted to the high end products that are very expensive. We focus on economic types with similar performance to the high end products. Memory compression is a key technique to achieve the goal and is integrated into a Java runtime environment. We save memory with runtime compression and reduce power by a memory bank partitioning technique (powering off unused memory banks). In memory compression algorithms and the Java runtime environment are studied. The Wilson and Kaplan (WK) algorithm is discussed as in-memory compression and introduced to the Java heap as an alternative of the garbage collection (gc). Experiments show around 10% of speedup and up to 45% of memory saving in the application core part (20.0 % of memory overhead for a user interface). The Java system using the memory compression outperforms its base configuration and will give further chance to reduce memory demand in combination with the garbage collection designed for the Java compressed heap. Experiments show

that the in-heap memory compression technique can save more than 50 % (up to 60 %) of the heap demand and that half of the memory banks for the Java heap may never be turned on. 50 % of the power consumption (memory leakage current) can be saved. The hardware compressor and decompressor are currently ten thousand times faster than the software counterparts. The time overhead could be negligible by introducing the hardware compressor and decompressor. Hardware/software codesign is an additional key to achieve our goal. The contribution of the runtime memory and heap compression is threefold: small memory demand, lower power consumption, and negligible time overhead in battery-powered handsets. Future work i--ncludes several issues unsolved in the Java memory compression: studies of integration of CLDC Hot Spot implementation and extension of the Java virtual machine to the traditional virtual machine. [C1039]

"Power Delivery Aware Floorplanning for Voltage Island Designs"

Voltage island has become a very effective design style for power saving by assigning different supply voltages to different modules. However, the new design style also brings forward new challenges, especially to the designer of P/G networks. In this paper, we study the power delivery problem in voltage island designs, and propose to consider voltage drop during the floorplanning process to reduce design iterations. We have implemented a floorplanner supporting voltage islands with special considerations on power delivery integrity. Our analysis shows that it is unnecessary to consider the pitch of the P/G network in the floorplan stage. Using this strategy to guide our new floorplaner, we can get more robust low power design under almost the same run time. Experimental results have demonstrated the effectiveness of our approach [C1040]

"Energy efficiency of different data transmission methods in IEEE 802.15.4: study and improvement"

IEEE 802.15.4 is a new standard intended to serve a set of simple but important applications with very low power consumption and relaxed data rate requirements. Among these applications are residential networks, medical sensor networks, and industrial monitoring networks. In this paper, we propose new mechanisms to reduce the energy consumption of IEEE 802.15.4 devices further. Analysis results show that our schemes can improve energy efficiency of the devices, and save up to 47% energy in tracking beacons. Thus it can extend the lifetime of the entire personal area network [C1041]

"Bandwidth-efficient Display Controller for Low Power Devices in Presence of Occlusion"

Traditional image composition for output display involves accessing discrete overlay images and blending them together as per the requirement of the application. Increased display sizes and number of overlays increases the memory bandwidth. For low power SOCs with integrated display controllers display traffic has an adverse effect on the application's performance and power consumption. Based on the overlay positions and blending method used for output image composition only one overlay may occlude another fully or partially. Hardware display accelerators can take advantage of such occlusion to reduce memory bandwidth without compromising image quality. This paper presents strategies for such reduction for some of the popular blending algorithms. A bandwidth efficiency metric n is defined and is evaluated for each of the presented schemes. Savings in memory bandwidth leads to higher performance of applications and also reduced power at the memory interface and hence increasing battery lifetime. [C1042]

"Shortcut Tree Routing in ZigBee Networks"

ZigBee is the emerging industrial standard for ad hoc networks based on IEEE 802.15.4. Due to characteristics such as low data rate, low price, and low power consumption, ZigBee is expected to be used in wireless sensor networks for remote monitoring, home control, and industrial automation. Since one of the most important goals is to reduce the installation and running cost, ZigBee stack is embedded in small and cheap micro-controller units. Since tree routing does not require any routing tables to send the packet to the destination, it can be used in ZigBee end devices that have limited resources. However, tree routing has the problem that the packets follow the tree topology to the destination even if the destination is located nearby. We propose the shortcut tree routing protocol to reduce the routing cost of ZigBee tree routing by using the neighbor table that is originally defined in the ZigBee standard. While following the ZigBee tree routing algorithm, we suggest forwarding the packet to the neighbor node if it can reduce the routing cost to the destination. Simulation results show that the shortcut tree routing algorithm saves more than 30 percent of the hop count compared with ZigBee tree routing. [C1043]

"An Energy-Efficient Approach to Scheduling in Wireless Sensor Networks"

It is very important to reduce the energy consumption in wireless sensor networks, where the nodes operate on batteries. With consideration of both the transmission energy and the circuit energy consumption, we study the

problem of energy efficiency in time-division-multiple-access (TDMA) link scheduling, and derive the optimal scheduling protocol to minimize the energy utilization for wireless sensor network. In order to reduce the computational complexity, we develop a suboptimal fractional-inverse-log scheduling (FILS) protocol for real implementation, which is shown to reduce a significant amount of energy consumption compared to previously designed protocols. Finally, we also developed the simplified distributed fractional-inverse-log scheduling to remove the communication overhead in centralized scheduling protocols, and simulation results show that it is very efficient in energy saving especially for a large-scale wireless sensor network [C1044]

"Energy-Efficient Cache Replacement Policies for Cooperative Caching in Mobile Ad Hoc Network"

Data caching on mobile clients is widely seen as an effective solution to improve system performance. In particular, cooperative caching, based on the idea of sharing and coordination of cache data among multiple users, can be particularly effective for information access in mobile ad hoc networks where mobile clients moving frequently and network topology changing dynamically. Most existing cache strategies perform replacement independently, and they seldom consider coordinated replacement and energy saving issues in the context of a mobile ad hoc network. This paper analysed the impact of energy on designing a cache replacement policy and formulate the energy-efficient coordinated cache replacement problem (ECORP) as a 0-1 knapsack problem. A heuristic algorithm called ECORP-greedy and an optimal solution called ECORP-OPT are presented to solve the problem. Simulations show that the proposed policies can significantly reduce energy consumption and access latency when compared to other replacement policies. [C1045]

"SmartBone: An Energy-Efficient Smart Backbone Construction in Wireless Sensor Networks"

Wireless sensor network is a rapidly growing discipline with new technologies emerging, and new applications under development. The nodes in a wireless network generally communicate with each other along the same wireless channel. Unfortunately, sharing among wireless channels decreases network performance due to radio interference, and also raises energy consumption due to packet retransmission when interference occurs. Many topology control algorithms have been proposed to solve these problems. One widely used strategy is the backbone method. Backbone algorithms aim to reduce the backbone size. However, poor performance may be explored if only few backbone nodes are selected. Therefore, several heuristic algorithms such as SBC have been proposed. However, these algorithms cannot efficiently eliminate redundant nodes, and dramatically decrease performance, especially in relatively sparse networks. This study proposes a novel heuristic-based backbone algorithm called SmartBone to choose proper backbone nodes from a network. SmartBone includes two major mechanisms. Flow-bottleneck preprocessing is adopted to find critical nodes, which act as backbone nodes to improve connectivity. Dynamic density cutback is adopted to reduce the number of redundant nodes depending on local area node density of network. SmartBone simultaneously considers the balance of network performance and energy savings. Significantly, the proposed algorithm has a 50% smaller backbone size than SBC, and improves the energy saving ratio from 25% using SBC to 40% using SmartBone. Moreover, SmartBone improves the packet delivery ratio from 40% to 90% when the density of sensor networks becomes relatively sparser. [C1046]

"Effective Power Control for Multimedia Streaming with QoS Constraints in Heterogeneous Networks"

Power consumption is a critical issue in multimedia streaming over a heterogeneous network, where wired and wireless links are interoperated together. To effectively reduce power consumption in this type of networks, we propose an effective power control method that can determine the optimal transmit powers for multimedia traffic with QoS constraints. Optimal transmit power of a network node can be characterized by a cost function, which jointly takes into account the transmit power and link quality under an end-to-end frame-error constraint. Two proposed methods, namely, route-based power management and link-associated power management, are developed to solve the power cost problem. Experiments are conducted through simulation in a heterogeneous network. The results demonstrate the relative superiority and effectiveness of the link-associated approach in power saving. [C1047]

"A Cross-Layer Data Gathering Scheme for Heterogeneous Sensor Networks Based on Polling and Load-balancing"

In this paper, a contention-free polling protocol and a load-balancing algorithm, for two-layered heterogeneous sensor networks were proposed, based on the energy consumption features of the physical layer, MAC layer and network layer. By introducing some powerful nodes, sensors can be organized into clusters. Each powerful node works as a local data sink and gathers data from sensors in the cluster. The power consumption model of IEEE 802.15.4-based transceivers was first analyzed. Based on physical layer features of such low-power, low-rate

transceivers, a contention-free polling protocol for inner-cluster data gathering was designed, so that packet collision can be avoided. By deactivating the transceivers of sensors which do not need to transmit or receive packets, energy consumption on idle listening can be saved. A load-balancing algorithm at network layer was also proposed to maximize the network lifetime by taking into consideration of power consumption features at the physical and MAC layers. Simulation results show that the proposed scheme can achieve more than one order of magnitude improvement compared to the FLOW-CSMA combination and reduce the duration of sensor duty cycle by at least 50% under various offered traffic loads. [C1048]

"Low Power UWB Transceiver Design Using Dynamic Voltage Scaling"

Low power consumption is a critical issue in many UWB systems. This paper investigates the application of dynamic voltage scaling (DVS) and other low power design techniques to a multiband-OFDM UWB transceiver baseband circuit design in order to reduce average power consumption of the chip. The results show significant power savings over the conventional approach. [C1049]

"Distributed Coordination of Sensors for End-to-End Reliable Event and Query Delivery"

This paper presents a new transport solution for WSNs addressing bidirectional end-to-end event and query reliability. The authors aim to reduce the reliable transport overhead while guaranteeing the reliability to deliver all events and queries in WSN applications. The proposed lightweight solution can achieve desired event reliability in conjunction with query reliability by operating with the least possible number of messages, and using a small subset of coordinators which are responsible of loss detection and recovery. Coordinators are selected using a distributed, low-cost algorithm with adaptive path discovery and maintenance features to utilize the cost of retransmissions and energy consumption. Simulation results show that, using such a coordination of sensors, significant savings on communication costs for event and query reliability are attainable while minimizing packet loss, energy consumption, and end-to-end delay. [C1050]

"Reducing Power Consumption in Network Discovery with Motion Detection in Heterogeneous Wireless Networks"

Seamless handoff is critical to providing high-quality services for mobile users. Before handoff, a mobile terminal (MT) must be aware of the impending handoff and determine what other wireless networks are available in time. In the network discovery stage, an MT must activate its interfaces for base station search, association, AAA (authentication, authorization, accounting), address acquisition, and so on. Therefore, if insufficient time is available for the MT to perform these procedures, then the connection will be disrupted. However, frequent interface activation can cause considerable battery drain. This paper presents a network discovery algorithm with motion detection, NDMD, to solve these problems. NDMD can simply use the received signal strength (RSS) to predict a user's motion without the assistance of a positioning system. Based on the predicted moving behavior, an MT can perform network discovery in time to reduce handoff dropping rate and prevent unnecessary activation of its interfaces to save the battery power. Simulation results show that NDMD can effectively detect user behavior, reduce power consumption in network discovery, and improve handoff quality. [C1051]

"Object-Oriented Reconfiguration"

As embedded systems are getting more complex, they are also presenting more stringent constraints like performance, power consumption, memory footprint and so on. At the same time, because of market pressures, their development time must be constantly reduced. The employment of object orientation would solve the design cycle problem. However, OO languages like Java or C+ + are not targeted to any of the embedded systems constraints stated before. Based on all these facts, this work focuses on providing the high OO abstraction, while maintaining embedded systems perspective. The methodology consists in the execution of selected objects in a reconfigurable hardware, which solves the overhead problems. This way, with efficient execution of certain intensively used objects in the reconfigurable array, we show performance improvements of up to 47% and savings of 37% in energy consumption, still taking advantage of the well known benefits of an object-oriented language. For our experiments we used a native Java processor, together with a complete MP3 player, representing a complex embedded system benchmark. [C1052]

"High Efficiency IPM Motor Drives for Hybrid Electric Vehicles"

In the 21stcentury, global warming has become an important issue. Carbon dioxide (CO_2) gas emissions should be reduced to preserve the correct air quality as per Kyoto protocol, implemented on February 16, 2005 by most of the countries. Modern human beings, who enjoy the fruits of electric energy technologies for climate controlled home and work place environments via air conditioners/heat pumps, and mass transportation using cars as necessities, cannot put up with the inconveniences of the past. In order to maintain and develop this energy

consuming technologies, availability of sustainable energy sources and their effective uses through efficiency improvements are of paramount importance. Power electronics and electric motor drives are the enabling technologies crucial for industrial competitiveness in the world market place. One of the most valuable achievements in power electronics is to introduce degree of freedom to variable frequency from the fixed value of the generated electrical power supplies. Over 60% of the generated energy is consumed by electric motors. Variable speed drive, which regulates the speed of the motor by controlling the frequency through smart uses of power electronics and control systems, can significantly reduce the energy consumption. Thus improvements in efficiency of the drive systems are the most effective measures to reduce primary energy consumption; and thereby reduce CO2gas emissions, which cause global warming. The objective of this paper is to provide a short introduction to the recent emergence of high efficiency and high performance interior permanent magnet (IPM) synchronous motors. Highlights of IPM motors include wide spread application in Japanese made hybrid electric vehicles to save precious electric energy, reduce gas emission and deter climate change. [C1053]

"Numerical Optimization of Speed Profiles of Inverter Trains Considering DC Feeding Circuit"

An algorithm optimizing total energy consumption of multiple inverter train operation considering DC feeding circuit is investigated in this paper. The proposed mathematical formulation can deal with several characteristics of trains, especially the effect of regenerative braking system. The developed optimization algorithm based on the gradient method is applicable to solve the formulated problems. The algorithm is ready to apply practical large-scale problems. The formulation and algorithm enables us to discuss energy-saving operation quantitatively. Several numerical analyses are demonstrated to verify the reliability and validity of the proposed method and clarify the energy-saving operation for two trains. The results shows that train speed profiles and control inputs strongly depend on the phase of departure times. The proposed algorithm can reduce energy consumption by 4.2~17.9% from that based on the conventional operation rule. These results indicates that the numerical analyses are significant to realize energy-saving operation. [C1054]

"An Implementation of Page Allocation Shaping for Energy Efficiency"

Main memory in many tera-scale systems requires tens of kilowatts of power. The resulting energy consumption increases system cost and the heat produced reduces reliability. Emergent memory technologies will provide systems the ability to dynamically turn-on (online) and turn-off (offline) memory devices at runtime. This technology, coupled with slack in memory demand, offers the potential for significant energy savings in clusters of servers. However, to realize these energy savings, OS-level memory allocation and management techniques must be modified to minimize the number of active memory devices while satisfying application demands. We propose several page shaping techniques and structural enhancements to proactively and reactively direct allocations to a minimal number of devices. To evaluate these techniques on real systems, we implemented these shaping techniques in the Linux kernel. Experiments using our OS extensions coupled with a simple history-based heuristic (to track demand and control state transitions) yield up to 60% energy savings with less than 1% performance loss for various benchmarks including lmbench and SPEC. [C1055]

"Power-Aware Speedup"

Power-aware processors operate in various power modes to reduce energy consumption with a corresponding decrease in peak processor throughput. Recent work has shown power-aware clusters can conserve significant energy (>30%) with minimal performance loss (<1%) running parallel scientific workloads. Nonetheless, such savings are typically achieved using a priori knowledge of application performance. Accurate prediction of parallel power consumption and performance is an open problem. However, such techniques would improve our understanding of power-aware cluster tradeoffs and enable identification of system configurations optimized for performance and power ("sweet spots"). Speedup models are powerful analytical tools for evaluating and predicting the performance of parallel applications. Unfortunately, existing speedup models do not quantify parallel overhead for simplicity. Consequently, these models are incapable of accurately accounting for performance and power. We propose power-aware speedup to model and predict the scaled execution time of power-aware clusters. The new model accounts for parallel overhead and predicts (within 7%) the power-aware performance and energy-delay products for various system configurations (i.e. processor counts and frequencies) on NAS parallel benchmark codes. [C1056]

"A Near-optimal Solution for the Heterogeneous Multi-processor Single-level Voltage Setup Problem"

A heterogeneous multi-processor (HeMP) system consists of several heterogeneous processors, each of which is specially designed to deliver the best energy-saving performance for a particular category of applications. A low-power real-time scheduling algorithm is required to schedule tasks on such a system to minimize its energy

consumption and complete all tasks by their deadline. The problem of determining the optimal speed for each processor to minimize the total energy consumption is called the voltage setup problem. This paper provides a near-optimal solution for the HeMP single-level voltage setup problem. To our best knowledge, we are the first work that addresses this problem. Initially, each task is assigned to a processor in a local-optimal manner. We next propose a couple of solutions to reduce energy by migrating tasks between processors. Finally, we determine each processor's speed by its final workload and the deadline. We conducted a series of simulations to evaluate our algorithms. The results show that the local-optimal partition leads to a considerably better energy-saving schedule than a commonly-used homogeneous multi-processor scheduling algorithm. Furthermore, at all measurable configurations, our energy consumption is at most 3% more than the optimal value obtained by an exhaustive iteration of all possible task-to-processor assignments. In summary, our work is shown to provide a near-optimal solution at its polynomial-time complexity. [C1057]

"Determining the Minimum Energy Consumption using Dynamic Voltage and Frequency Scaling"

While improving raw performance is of primary interest to most users of high-performance computers, energy consumption also is a critical concern. Some microprocessors allow voltage and frequency scaling, which enables a system to reduce CPU power and performance when the CPU is not on the critical path. When properly directed, such dynamic voltage and frequency scaling can produce significant energy savings with little performance penalty. Various DVFS scaling algorithms have been proposed. However, the benefit is application-dependent. We cannot see if they achieve the energy consumption as minimum as possible. So, it is important to establish the baseline of the DVFS scheduling for any application. This paper determines minimum energy consumption in voltage and frequency scaling systems for a given time delay. We assume we have a set of fixed points where scaling can occur. A brute-force solution is intractable even for a moderately sized set (although all programs presented in this paper can be solved with the brute-force). Our algorithm efficiently chooses the exact optimal schedule satisfying the given time constraint by estimation. Besides, our time and energy estimations from the optimal schedule have reasonable accuracy with 1.48% of differences at maximum. [C1058]

"Microarchitecture Floorplanning for Sub-threshold Leakage Reduction"

Lateral heat conduction between modules affects the temperature profile of a floorplan, affecting the leakage power of individual blocks which increasingly is becoming a larger fraction of the overall power consumption with scaling of fabrication technologies. By modeling temperature dependent leakage power within a micro architecture-aware floorplanning process, we propose a method that reduces sub-threshold leakage power. To that end, two leakage models are used: a transient formulation independent of any leakage power model and a simpler formulation derived from an empirical leakage power model, both showing good fidelity to detailed transient simulations. Our algorithm can reduce subthreshold leakage by up to 15% with a minor degradation in performance, compared to a floorplanning process that does not model leakage. We also show the importance of modeling whitespace during floorplanning and its impact on leakage savings [C1059]

"A Stopping Criterion for Low-Density Parity-Check Codes"

Low-density parity-check (LDPC) codes have an inherent stopping criterion, parity-check constraints (equations). By testing the parity-check constraints, an LDPC decoder can detect successful decoding and stop their decoding, which is, however, not possible with turbo codes. In this paper, we propose a stopping criterion to predict decoding failure of LDPC codes, instead of detecting successful decoding. If the decoder predicts the decoding failure in advance, the receiver can more rapidly response to the transmitter and request for additional parity bits with an automatic repeat request (ARQ) protocol, which reduces overall system latency. The receiver can also save power consumption by avoiding unnecessary decoder iterations. The proposed stopping criterion makes use of the variations of the number of satisfied parity-check constraints in the belief-propagation (BP) decoding which is always tested in the conventional BP decoding to detect successful decoding. Thus, the proposed stopping criterion does not require any additional complexity. The counting of satisfied parity-check constraints shows behaviors of the BP decoding, which comes, otherwise, from the observations of changes of log-likelihood ratio (LLR) values in multi-bit resolution with additional complexity. [C1060]

"Integrated Data Reorganization and Disk Mapping for Reducing Disk Energy Consumption"

Increasing power consumption of high-performance systems leads to reliability, survivability, and cooling related problems. Motivated by this observation, several recent efforts focused on reducing disk power consumption through hardware, OS and compiler based techniques. This paper presents a novel approach to reducing disk power consumption of large-scale, array-intensive scientific applications. It proposes and evaluates a compiler-based approach that employs two complementary techniques: data reorganization and disk mapping. The first of

these, data reorganization, determines a suitable layout for data in the array space, whereas the second technique, disk mapping, decides the corresponding layout in the disk space. The goal of data reorganization and disk mapping is to ensure that data (from the different disk-resident arrays) that are accessed within the same loop iteration are colocated in the same set of disks. In this way, we can increase disk inter-access times (idle periods of disks) and this in turn allows better exploitation of the underlying hardware mechanisms used for reducing power. Our experiments with eight disk I/O-intensive scientific applications indicate that the proposed approach brings significant reductions in energy consumption, whether the underlying disk system uses spin-down disks or speed-reduced disks, two previously- proposed hardware-based disk power reduction schemes. The results also show that both the components of our scheme (data reorganization and disk mapping) are very important since applying any of these components alone does not generate large savings for most of our applica tions. [C1061]

"Peripheral-Conscious Scheduling on Energy Minimization for Weakly Hard Real-time Systems"

In this paper, we present a dynamic scheduling algorithm to minimize the energy consumption by both the DVS processor and peripheral devices in a weakly hard real-time system. In our approach, we first use a new static approach to partition real-time jobs into mandatory and optional part to meet the weakly hard real-time constraints. We then adopt an on-line approach that can effectively exploit the run-time variations and reduce the preemption impacts to leverage the energy saving performance. Extensive simulation studies demonstrate that our approach can effectively reduce the system-wide energy consumption while guaranteeing the weakly hard constraints [C1062]

"Design and Analysis of Low Power Dynamic Bus Based on RLC simulation"

In this paper, we propose a low power dynamic bus encoding scheme which simultaneously reduces the capacitive and inductive effects by the measurement of real RLC model. It should be noted that our method does not need a sufficient knowledge of the patterns on the bus. Our experimental results show that the proposed approach can save power consumption of the bus up to 12% compared to the nonencoded case. We also propose an area-aware scheme to optimize our circuits in terms of power consumption and area. The scheme can reduce the circuit area up to 29% while keeping almost the same power reduction [C1063]

"DRAM-Level Prefetching for Fully-Buffered DIMM: Design, Performance and Power Saving"

We have studied DRAM-level prefetching for the fully buffered DIMM (FB-DIMM) designed for multi-core processors. FB-DIMM has a unique two-level interconnect structure, with FB-DIMM channels at the first-level connecting the memory controller and advanced memory buffers (AMBs); and DDR2 buses at the second-level connecting the AMBs with DRAM chips. We propose an AMB prefetching method that prefetches memory blocks from DRAM chips to AMBs. It utilizes the redundant bandwidth between the DRAM chips and AMBs but does not consume the crucial channel bandwidth. The proposed method fetches K memory blocks of L2 cache block sizes around the demanded block, where K is a small value ranging from two to eight. The method may also reduce the DRAM power consumption by merging some DRAM precharges and activations. Our cycle-accurate simulation shows that the average performance improvement is 16% for single-core and multi-core workloads constructed from memory-intensive SPEC2000 programs with software cache prefetching enabled; and no workload has negative speedup. We have found that the performance gain comes from the reduction of idle memory latency and the improvement of channel bandwidth utilization. We have also found that there is only a small overlap between the performance gains from the AMB prefetching and the software cache prefetching. The average of estimated power saving is 15% [C1064]

"A robust edge encoding technique for energy-efficient multi-cycle interconnect"

In this paper, we propose a new edge encoding technique to reduce the energy consumption in multi-cycle interconnects. Both average and worst-case energy are reduced by desynchronizing the edges of rising and falling transitions. In a 1.2V 65nm CMOS technology, the approach achieves up to 31% energy reduction with no latency overhead over optimally designed conventional busses due to coupling capacitance reductions. The technique further reduces energy consumption by 38% with iso-throughput at the expense of one-cycle latency. Energy savings are shown to be more robust to process variations than previous techniques. [C1065]

"Scoping the potential of monitoring and control technologies to reduce energy use in homes"

This scoping study takes a broad look at how Information Technology-enabled monitoring and control systems in residences could play a role in mitigating energy use. Managing the residential sector is an important priority for addressing energy use, as use in homes represents 21% of US total energy demand, up 16% from 1994. Much energy is apparently wasted in delivering energy services not actually used by residents. These include

heating/cooling of unoccupied houses and rooms, overheating or overcooling to make up for temperature variations, leakage current due to appliances in standby or off mode, and purchase of needlessly energy intensive models of appliances. The results of our initial rough estimate is that around 40% residential energy use is used to deliver these types of "unused" energy services. IT-enabled monitoring and control technologies have played an important role in eliminating similar kinds of waste in other sectors, so it is natural to think that these systems could have an important role in the home as well. The technology level of energy control in homes is at least 20 years old, with simple programmable thermostats still in only about a quarter of US homes. Networked thermostats, power meters and switches, and zone heating are technologies that can provide information on energy use and allow energy use to be controlled for distribution only when needed. We estimate that monitoring and control systems could save from 3-26% of residential energy use. The lower end corresponds to use of a programmable thermostat and the upper to an integrated system including monitoring and control of appliances, plus zone heating/cooling. We propose that these results provide renewed motivation to investigate the promotion of smart home energy technologies. [C1066]

"PEAN: A Probabilistic Energy Aware Neighbor Monitoring Protocol for Mobile Ad Hoc Networks"

This paper presents a novel application of the wake-up based power management protocol. MAC layer power management protocols have been studied for years. The power management mechanism which exploits the IEEE 802.11 power saving mode to save energy by turning on/off the network interface card is called the wake-up based power management. The previous proposals for the wake-up based power management focus on the network operations and neighbor discovery. In this paper, we apply the wake-up based power management to neighbor monitoring in securing mobile ad hoc networks (MANETs). We propose a probabilistic wake-up based power management protocol for neighbor monitoring which aims to reduce energy consumption while preserving the effectiveness of misbehaving node detection. We show by analysis and simulation the relation between the wake-up probability and the misbehavior detection rate. [C1067]

"Multi-Agent System for Directed Diffusion in Wireless Sensor Networks"

This paper presents an agent based system to increase the life time of node in Wireless Sensor Networks. In environment where node density is massive, placement is heterogeneous and lot of sensory traffic with redundancy is produced; individual nodes waste limited wireless bandwidth and consume lot of energy. This minimizes their life time on the network. Directed diffusion paradigm for distributed sensing of the environment has stated to deal with the phenomenon. Directed diffusion approach is data centric in that all communication is for named data. All the nodes in the directed diffusion are application aware and achieve energy saving by choosing good paths and processing data in-network. We unmitigated our efforts to augment the node life time in sensor network by introducing mobile agents. Mobile agents can be used to greatly reduce the communication cost, especially over low bandwidth links, by moving the processing function to the data rather than bringing the data to a central processor (sink). Toward this end, we propose an agent based directed diffusion approach. [C1068]

"A Coverage and Connectivity Method to Cluster Topology in Wireless Sensor Networks"

That is always an important topic to extend the whole lifetime in wireless network environment. How to make use of the consumption of the limited energy in the sensor nodes? How many sensor nodes can establish an optimum cluster? This paper proposes an optimum nodes number on clustering-based routing protocol called CCC (coverage and connectivity method to cluster topology), which utilizes a node of its' optimum coverage and connectivity to transmit to another node and calculate the quantity of the nodes of an optimum cluster. In this article, the CCC, which is distributed the energy dissipation of sensor nodes and average energy savings. The performance of CCC is then compared to clustering-based schemes such as low-energy adaptive clustering hierarchy (LEACH). Simulation results show that CCC improves network lifetime and reduces whole average of energy consumption. [C1069]

"MCTA: Target Tracking Algorithm Based on Minimal Contour in Wireless Sensor Networks"

This paper proposes a minimal contour tracking algorithm (MCTA) that reduces energy consumption for tracking mobile targets in wireless sensor networks in terms of sensing and communication energy consumption. MCTA conserves energy by letting only a minimum number of sensor nodes participate in communication and perform sensing for target tracking. MCTA uses the minimal tracking area based on the vehicular kinematics. The modeling of target's kinematics allows for pruning out part of the tracking area that cannot be mechanically visited by the mobile target within scheduled time. So, MCTA sends the tracking area information to only the sensor nodes within minimal tracking area and wakes them up. Compared to the legacy scheme which uses circle-based tracking area, our proposed scheme uses less number of sensors for tracking in both

communication and sensing without target missing. Through simulation, we show that MCTA outperforms the circle-based scheme with about 60% energy saving under certain ideal situations. [C1070]

"Optimal Channel Changing Delay for Mobile TV Over DVB-H"

This paper provides an analysis on the optimal channel changing delay in DVB-H (Digital Video Broadcasting for Handhelds) channels for Mobile Television. DVB-H uses a time-sliced transmission scheme to reduce the power consumption used for radio reception in DVB-H receivers. Channel changing delay, i.e. changing from one audio-visual service to another, is increased due to the time slicing scheme in DVB-H. One of the significant factors in channel changing delay is the Decoder Refresh Delay. The Decoder Refresh Delay is the time from the start of video decoding to the start of correct output from decoder. This delay is minimized when a time-slice starts with a random access point picture such as an instantaneous decoding refresh (IDR) picture in H.264/AVC standard. In DVB-H, encapsulation into time-slices is performed independently from content encoding. At the time of encoding, the exact time-slice boundaries are typically unknown, and therefore it is impossible to align the location of IDR pictures to time-slice boundaries. The average decoder refresh delay can decrease by frequent IDR pictures in the bit stream. However, using very frequent IDR pictures drops the compression efficiency and the quality of compressed video dramatically. Another factor in channel changing delay is the delay required to compensate the variation in bit rate. In video streaming over DVB-H the improved quality and compression efficiency obtained by using variable bit rate should be exploited. Higher quality and compression performance can be provided by higher delay. Moreover, when changing channels, a delay is required until the start of the desired time-slice and a further delay is incurred to complete the reception of the entire time-slice. These delays depend on the time-slicing parameters that define the power saving percentage obtained as the result of the time-slice scheme. The lower the receiver power consumption, the higher delay is required. Therefore, there is a strong multil- ateral relationship between the quality of compressed video, the channel changing delay and the power consumption in the receiver. Simulations were conducted and based on the simulation results an optimal operating area is proposed. [C1071]

"An Optimal Algorithm for Low Power Multiplierless FIR Filter Design using Chebychev Criterion"

In this paper, we propose a novel finite impulse response (FIR) filter design methodology that reduces the number of operations with a motivation to reduce power consumption and enhance performance. The novelty of our approach lies in the generation of filter coefficients such that they conform to a given low-power architecture, while meeting the given filter specifications. The proposed algorithm is formulated as a mixed integer linear programming problem that minimizes Chebychev error and synthesizes coefficients which consist of pre-specified alphabets. The new modified coefficients can be used for low-power VLSI implementation of vector scaling operations such as FIR filtering using computation sharing multiplier (CSHM). Simulations in 0.25 mum technology show that CSHM FIR filter architecture can result in 55% power and 34% speed improvement compared to carry save multiplier (CSAM) based filters [C1072]

"The Selective Preference of Energy Saving and Consumption Reducing Project for Enterprise Based on Factor Analysis and Fuzzy Comprehensive Evaluation"

Generally, diversification of enterprises' production flow effects the selective preference of energy saving and consumption reducing project. This paper disintegrates enterprises' production flow, applies the factor analysis and fuzzy comprehensive evaluation to implement the selective preference of energy saving and consumption reducing project. A power plant case is presented at the end of the paper to illustrate the proposed model. [C1073]

"Novel critical-path based low-energy scheduling algorithms for heterogeneous multiprocessor real-time embedded systems"

In this paper, we propose novel low-energy static and dynamic scheduling algorithms with low computational complexities, for heterogeneous multiprocessor real-time embedded systems. We consider task graphs with deadlines and precedence relationships to satisfy. We propose a novel scheme, referred to as "critical-path information track-and update", based on critical-path analysis to distribute the slack-time over tasks such that energy consumption is minimized, while guaranteeing the precedence and timing constraints. Our dynamic scheduling algorithm applies the static scheduling algorithm during runtime based on the updated average-case execution demands of tasks. Our simulation results show that the proposed static scheduling algorithm consumes only 2% of the computational time with no degradation in energy savings, whereas the dynamic scheduling algorithm delivers up to 25% more energy savings while reducing the computational time overhead by more than 90%, when compared with heterogeneous multiprocessor scheduling algorithms. [C1074]

"A Voronoi dEtection Range Adjustment (VERA) approach for energy saving of wireless sensor networks"

Since the batteries in a wireless sensor networks cannot be replaced, efficient power management becomes an important research issue. If we can largely reduce the overlaps among detection ranges and decrease the amount of duplicate data then we can save energy more efficiently. Meguerdichian et al. exploit the coverage problems in wireless ad-hoc sensor networks in terms of Voronoi diagram and Delaunay triangulation. In this paper, we propose a Voronoi detection range adjustment (VERA) method that utilizes distributed Voronoi diagram to delimit the area of responsibility for each sensor. We then use genetic algorithm to optimize the most suitable detection range for each sensor. Simulations show that VERA outperforms maximum detection range, K-covered, and greedy methods in terms of reducing the overlaps among detection ranges, minimizing energy consumption, and prolonging the lifetime of the whole network. [C1075]

"Practical and accurate pulse-loss-prediction method and its application to switching power supply"

Following the decrease of power supply voltage for integrated circuits, the increase of power consumption of information technology systems as well as environmental issues, there is a need to reduce the energy consumption of the systems and the loss of power supply circuits, therefore an accurate and practical loss prediction method is required. This paper describes a new loss prediction method for switching power supply circuits, suited for quick evaluation and comparison of components with accuracy needed for power supply circuit design. A set of Pulse-Loss-Prediction equations was derived in explicit form of elementary functions, from resistive-loss frequency response model and square pulse current model, using Fourier transform and numerical calculation. When the resistance's frequency response of a component is known, its loss can be calculated rapidly and easily against pulse currents of arbitrary period and rise-fall time, in a switching power supply, before actually building one. Transformers' and MOS FETs' resistances are measured, their frequency dependencies are shown, their Pulse-Losses are calculated with the developed method and compared. This method was applied to actual development of a low voltage, high power DC-DC converter for a supercomputer. Component selection, optimization was carried out using this method, and an efficiency of 82% at 1.4 V, 200 A output, 280 V input, was realized. This new power supply gave significant power consumption reduction of the system from conventional model, contributing to initial and running cost reduction, energy saving and environmental conservation and sustainability. [C1076]

"Design and implementation of scalable low power radix-4 Montgomery modular multiplier"

This paper presents an efficient Montgomery modular multiplier for the modular exponentiation operation, which is fundamental to numerous public-key cryptosystems. Four aspects are considered: performance, power, reliability, and scalability. To increase performance, the architecture is based on the carry-save adder (CSA). To lower power consumption, we devised several effective techniques for reducing the spurious transitions and the expected switching activity (ESA) of high fan-out signals. To achieve scalability, we implement a 2-fold nested loop for the whole data processing flow. Lastly, to make sure that the arithmetic operation runs correctly without inducing data overflow error, we find out the optimum numbers of bits for all vectors appearing in the operation through a mathematical analysis. In the evaluation of hardware implemented using Xilinx "ISE WebPACK" tool for xc3s1600e-5fg484 (Spartan 3E) FPGA, the radix 4 design introduced in this paper has a significant gain in reducing the total computation time and power consumption over other compared designs. [C1077]

"A Low Power CMOS VCO for IEEE 802.11a Applications"

A low power consumption CMOS complementary cross-coupled LC-tank voltage-controlled oscillator (VCO) is presented. The low power consumption VCO has been implemented with tsmc 0.18 mum 1P6M CMOS technology. A pseudo-resistance transistor is utilized to reduce the DC bias current under a fixed supply voltage. The circuit consumes 2.58 mA from a 1.6 V power supply which saves up to 27% power compared with the conventional one. Furthermore, the proposed circuit which has oscillated frequency from 5.14 GHz to 6.25 GHz obtains 19.5% of tuning range. The phase noise achieves -116 dBc/Hz at 1 MHz offset frequency. The designed VCO can cover the frequency range of both 5.15 GHz-5.35 GHz and 5.725 GHz-5.825 GHz which is suitable for IEEE 802.11a receiver. [C1078]

"Experimental investigation of the energy consumption for wireless sensor network with centralized data collection scheme"

Energy consumption minimization onWSN (wireless sensors network) is an open challenge. WSN is typically composed by an elevated number of battery powered devices that cooperate to forward data to a rendezvous point. In order to maximize network lifetime many protocols implement sleeps policy and try to reduce devices

idle times. Unfortunately a trade off between energy requirements and data delivery delays exist and have to be carefully considered during communication protocol developments. In fact when the attention is moved to network implementation aspects, hardware's details became extremely important. The exact knowledge of device energy requirements during normal protocol operations is essential in order to optimize the energy saving strategies. With this conviction in mind, this work characterize through a campaign of measures the energy requirements of a sensor network based on EyesIFXv2.0 sensor nodes. In order to obtain a generalizable result, we have focused our attention on a simple centralized scheme and we have investigated traffic influences on the devices mean energy consumptions. Two important aspects of WSN has considered: Firstly we focused our attention on delay introduced by collision avoidance mechanism on data collections into a geographic area. Secondly we moved our interest on devices power consumption requirements under different network traffic conditions. [C1079]

"Estimate on CO2 emissions reduction effects achieved by the adoption of a water spray humidification system to clean rooms"

We proposed water spray humidification in an indoor system for clean rooms used for the production of semiconductors and FPDs, and calculated the energy-saving effect and CO2emission reduction effect of this system. As a result of estimate on annual energy consumption by air conditioning at model semiconductor factory, this system can be reduced heating load of 76% and CO2emission of 0.23 ton-CO2/Year per volume of outside air of 1 m3/min. [C1080]

""New Energy" for telecommunications power systems"

The considerable problems deriving from the growth of energetic consumptions and from the relevant environmental "emergency" due to the emissions of greenhouse gases, push people to And out new solutions and new technologies for the production of primary energy lit for fulfilling the pressing and growing energetic demands. This is also true in the telecommunication applications, which has seen, in the last years, a remarkable increase in the number of installations present on the whole national territory-sometimes located in hardly reachable areas-and the relevant growth of energetic consumptions. The aim of this work is to optimize energetic consumptions for a radio-telecommunication apparatus, through the combination of different interventions, even more advantageous and efficient from the economical and environmental point of view. The work will explore the possibility of interventions which would use both the renewable energetic sources (e.g.: photovoltaic cells) and strategies in energetic saving and interventions for reducing emissions. This study will evaluate, from a technical and economical point of view, the feasibility of some solutions, by: Energetic auditing for a radio-telecommunication station in different functionality contexts (urban and rural areas, different periods in the year, different running charges, etc.); Verification-even through specific field measurements -of environmental emissions deriving from radio- telecommunications systems; Analyses in the interventions of efficiency and energetic saving (optimization of air conditioning consumptions, efficiency in the temperature control system, etc.); Evaluation and development of interventions and technical solutions based on the production of a part of the power energy used by radio-telecommunication apparatus, through the use of photovoltaic cells on the same infrastructures; Analyses of possible uses of further renewable sources (e.g. wind micro turbines or new alternative power based-on fuel cells) generating energy usable from telecommunications power systems located in some parts of the territory not reached by the electricity net; Analyses of the social and environmental advantages in the introduction of technologies based on renewable sources for covering a part of the energetic radio-telecommunication installations' requirements. Environmental monitoring of the sites where prototypal solutions will be installed for comparing the conditions before and after the intervention. The proposing party of the project is the Department of Environmental Sciences of the Second University of Naples (DSA-SUN) in collaboration with the National Agency for the Environment Protection (APAT) and it foresees the participation of providers of mobile communications and technological partners, which, thanks to their experience in the mobile phone communications, are able to test the prototypical solutions deriving from the results of the studies carried out by the laboratories and structures of the DSA-SUN and APAT, and can also make some urban and rural sites available for testing the several proposed solutions. [C1081]

"Tag compression for low power in instruction caches"

As power consumption of the cache memory in modern processor designs tends to dominate, measures must be taken to keep it under control. This paper introduces an approach for reducing instruction cache power based on the operation of the Tag Compression Registers added in the cache system. The power savings show that, when the size of the Tag Compression Registers is properly fixed, the average saving on the power consumption of the instruction cache could be up to 64% compared with the traditional instruction cache structure. [C1082]

"Bandwidth- efficient voice activity detector"

The audio signal is processed in two frequency bands, to detect active and inactive frames present in the audio signal. The voice activity classification of the audio signal is performed depending on the evaluated plurality of parameters and pre-defined validation conditions. The plurality of parameters includes low band energy, high band energy, variance, variance factor, etc. Accurate classification of proposed VAD is evaluated by comparing the bandwidth saving from standard ITU-T G.729B VAD without degrading the voice quality. This bandwidth saving reduces power consumption of a transmitting device, which increases usage time of the battery of the transmitting device. [C1083]

"Energy-efficient Tracking of Mobile Objects with Early Distance-based Reporting"

Many location-based systems rely on fine-grained tracking of mobile objects that determine their own locations with sensing devices like GPS receivers. For these objects, energy is a very valuable and limited resource. A distance-based reporting protocol can be employed to reduce the energy they consume by sending position updates. However, the energy required for position sensing has not been considered in the past. In this paper, we study how the resulting energy consumption from both sensing and update operations can be reduced for distance-based reporting. We show that significant savings are achieved by sending position updates earlier than actually required. For uniform movement, we derive the minimal power consumption analytically. Subsequently, two novel online heuristics are proposed that control the sending of position updates at runtime. Their effectiveness is validated by extensive simulations. [C1084]

"Low-Power Area-Efficient Decimation Filters in Sigma-Delta ADCs"

The performances of different structures for Sine filters were analyzed and compared in this paper. To reduce their power consumption and chip area, a new optimum method was proposed. And it was implemented in poly-phase structure and direct-realization structure respectively for verification. In addition, the low-power area-efficient optimization scheme for decimation filters in Sigma-Delta ADCs was also discussed. All simulation results were obtained under supply voltage of 1.62 V using TSMC 0.18 mum CMOS technology. The results showed that, compared to CIC, 36% area and 50% power were saved for poly-phase structure and 64% power consumption was reduced for direct-realization structure. [C1085]

"Towards an energy efficient branch prediction scheme using profiling, adaptive bias measurement and delay region scheduling"

Dynamic branch predictors account for between 10% and 40% of a processor's dynamic power consumption. This power cost is proportional to the number of accesses made to that dynamic predictor during a program's execution. In this paper we propose the combined use of local delay region scheduling and profiling with an original adaptive branch bias measurement. The adaptive branch bias measurement takes note of the dynamic predictor's accuracy for a given branch and decides whether or not to assign a static prediction for that branch. The static prediction and local delay region scheduling information is represented as two hint bits in branch instructions. We show that, with the combined use of these two methods, the number of dynamic branch predictor accesses/updates can be reduced by up to 62%. The associated average power saving is very encouraging; for the example high-performance embedded architecture n average global processor power saving of 6.22% is achieved. [C1086]

"Leakage current control of nano-scale full adder cells using input vectors"

As CMOS technology scaling continues into the nanoscale domain, static or leakage power consumption becomes a vital design parameter. This paper proposes methods for reducing leakage currents by controlling the input vector in nano-scale full adder cells operating in either active mode or standby mode. With proper input vector control, it is possible to obtain over 40% leakage power savings for most of the full adder circuits presented. [C1087]

"Polyphase Implementation of Non-recursive Comb Decimators for Sigma-Delta A/D Converters"

In a sigma-delta analog to digital (A/D) converter, the most computationally intensive block is the decimation filter and its hardware implementation may require millions of transistors. Since these converters are now targeted for a portable application, a hardware efficient design is an implicit requirement. In this effect, this paper presents a computationally efficient polyphase implementation of non-recursive cascaded integrator comb (CIC) decimators for sigma-delta converters (SDCs). The SDCs are operating at high oversampling frequencies and hence require large sampling rate conversions. The filtering and rate reduction are performed in several stages to reduce hardware complexity and power dissipation. The CIC filters are widely adopted as the first stage of

decimation due to its multiplier free structure. In this research, the performance of polyphase structure is compared with the CICs using recursive and non-recursive algorithms in terms of power, speed and area. This polyphase implementation offers high speed operation and low power consumption. The polyphase implementation of 4thorder CIC filter with a decimation factor of '64' and input word length of '4-bits' offers about 70% and 37% of power saving compared to the corresponding recursive and non-recursive implementations respectively. The same polyphase CIC filter can operate about 7 times faster than the recursive and about 3.7 times faster than the non-recursive CIC filters. [C1088]

"Energy Saving Policy for CMP System Based on M/M/c Queue with Synchronous Vacations"

Dynamic power management (DPM) and dynamic voltage scaling (DVS) have been used as effective strategies to reduce the power consumption of portable systems. Most of existing optimal algorithm based on DPM and DVS need information of task set such as release time, execution time and deadline in advance. We present a real-time two-stage policy for multiprocessor systems to reduce the energy consumption. We propose a model of M/M/c queue with synchronous vacations to control the states of processors at system level. Besides, we use the frequency controller to modulate the operating frequency of processors based on the prospective workload. The simulating experiment results demonstrate that our algorithm increase energy efficiency with little system performance degradation. [C1089]

"A Decentralized Hole-Shape Regulation Technique for Enhancing Patrol and Deployment Tasks in Mobile WSNs"

In wireless sensor networks (WSNs), a hole is formed due to the non-uniform deployment, nodes failure, and some natural phenomena such as animals' residence or fierce wind making sensor nodes broken. The existence of a hole reduces both the accuracy of data collection and the efficiency of communications. Recently, many studies proposed mechanisms to detach a robot that loads with static sensors to heal the hole and maintain the spatial full coverage. Some other studies utilized mobile sensors to patrol the hole, maintaining the temporal full coverage. However, an irregular hole results in the redeployment and patrolling tasks inefficiency. This protocol proposes a novel mechanism, called HONOR, to normalize an irregular hole in a mobile WSN. Mobile sensors that detect the hole cooperate with each other to regularize the irregular hole in a distributed manner. As a result, the efficiency of robot's redeployment and the mobile sensors' patrol are significantly improved. Simulation results reveal that HONOR efficiently regularizes the hole shape and therefore saves energy consumption and delay time required for the robot's redeployment and the mobile sensors' patrol. [C1090]

"A Study on Data Aggregation and Reliability in Managing Wireless Sensor Networks"

Using data aggregation to reduce power consumption is a well studied area. In this paper we show a new result: data aggregation can also be used to increase reliability. In scenarios where status is being collected from every node (e.g. network management), one measure of reliability is the completeness (nodes included). Using some of the power savings from aggregation to increase the retransmission limit for aggregated data gives significant improvements in completeness. The contribution of this paper is in providing a detailed comparison of the completeness and energy efficiency for aggregated and non-aggregated data. Results, derived by numerical analysis and simulation, show that with data aggregation and increased retransmission limits, reliability can be substantially improved, while still saving power. These results are applicable to designing network management protocols for Wireless Sensor Networks, as well as for other scenarios where high completeness is required for network-wide data collection. [C1091]

"Is Your Low Power Design Switched On?"

Power is the key driver in most electronic systems design. Managing system power to increase battery life and reduce electricity consumption and heat generation are key considerations in developing many types of systems from mobile handsets, portable navigation systems and compute servers. New design techniques including clock gating, power gating, multi-voltage and dynamic voltage and frequency scaling have been employed to reduce both dynamic and static energy consumption. The design of low power electronic systems creates new design and verification challenges. Today's systems-on-chip are composed of large IP blocks approaching and exceeding 1 million gates. How can the system low power design intent be applied without requiring modification to and time consuming re-verification of the IP's golden RTL code? How can the functional impacts of power gating, retention and isolation be verified early in the design process when it is cheaper and easier to fix problems? Can implementation-dependent low power design functionality such as accurate retention save and restore protocols be verified prior to synthesis? In this presentation, we will discuss Accellcra's Unified Power Format standard for low power design intent and using UPF for verification. [C1092]

"Tree-Clustered Data Gathering Protocol (TCDGP) for Wireless Sensor Networks"

Wireless Sensor Networks (WSNs) consists of plenty nodes which are low cost, low power consuming, small volume and short-transmitting. As sensor nodes are deployed in sensing field, they can help people to monitor and aggregate data. Researchers also try to find more efficient ways of utilizing limited energy of sensor node in order to give longer life time of WSNs. Therefore, how to reduce node's energy that is consumed in transmitting data has became a very important issue. From many kinds of paper, multi-hop routing protocol is well known for power saving in data gathering. Recently researches uses such types of the cluster-based (e.g., LEACH), the chain-based (e.g., PEGASIS) and the tree-based (e.g., TREEPSI) to establish their energy-efficient routing protocol. In this paper, we propose tree-clustered data gathering protocol (also called TCDGP) to improve the LEACH and TREEPSI. The novel proposed protocol can preserve both advantages and improve the power consumption further. Finally, simulation results show that our proposal has better performance than before. [C1093]

"Adaptive Application-specific Cooperative Relay for Wireless Video Sensor Networks"

In this paper, we propose an adaptive application-specific cooperative relaying mechanism for delivering layered coded multimedia data over wireless sensor networks. The proposed approach is to optimally map source data layers of different perceptual importance to relay nodes, so that the most important data layer can be transmitted in high quality. Each relay node only needs to detect and forward the assigned sub-streams (layers) of multimedia data. The distinctive benefit of this approach is to minimize the video distortion induced by buffer overflow and delay violation, while reducing transmission processing requirements on each relay node and providing significant savings in transmit and receive energy. Experimental results show that, compared with other cooperative methods, the proposed algorithm achieves significant performance improvement. [C1094]

"Performance Analysis of DVS Algorithms for Reducing Processor Energy Consumption"

Dynamic voltage scaling (DVS) is an energy saving technique, which is achieved by reducing energy dissipation of the core by lowering the supply voltage and operating frequency. DVS technology lies at the heart of advanced digital products ranging from laptops, personal digital assistants, mobile phones and even game consoles. DVS has been widely acknowledged as a powerful technique for trading off for power consumption and delay for processors. In this paper a new DVS algorithm is presented, which achieves better energy savings with deadline guarantees by splitting task between discrete frequency levels and task deferring technique. The proposed DVS algorithm is compared with existing basic RT-DVS algorithms for real-time periodic task sets, analyzing their energy efficiency, and discussing the performance differences quantitatively. The simulation results show that the proposed algorithm closely approaches the theoretical lower bond on energy consumption and reduces the energy consumption by 10-15% over the existing DVS algorithm. [C1095]

"Exploiting Spatial Correlation in a three dimensional Wireless Sensor Network"

Physical attributes such as temperature exhibit gradual change in value with space. Observations from the sensor nodes are thus highly correlated. In this paper, we propose a scheme to exploit the spatial correlation of data in a three dimensional wireless sensor network (WSN), in a way so as to reduce the number of transmissions in the network, thereby saving energy. The presented work is an extension of the earlier proposed TREG scheme which is only applicable to two dimensional WSN. Our scheme involves formation of binary tree and transmission of data along the tree nodes. Simulation has been carried out for different tree heights. Simulation results show that a tree height of four provides results with optimal values. [C1096]

"Cluster Organization based Design of Hybrid MAC Protocol in Wireless Sensor Networks"

Wireless sensor networks have the limitations of energy. An efficient MAC protocol has to be applied to serve the purpose of energy saving and also aiming to make it cost efficient. This paper presents a novel hybrid MAC protocol that uses the information of clusters from routing layer to divide the MAC layer functionality into two types, namely, TDMA based intra-cluster communication and CSMA based inter-cluster communication. A distinctive feature of this approach is its robustness to synchronization errors and the associated power consumptions and delay performances are also computed resulting due to optimized performance of the hybrid mode for cluster organization. Simulation results show that this hybrid MAC layer thus considerably reduces the energy consumption in network nodes thereby increasing the total network lifetime. [C1097]

"Leakage Current Reduction in Data Caches on Embedded Systems"

Nowadays, embedded systems can be found in a wide range of pervasive devices (e.g., smart phones, PDAs, or video/digital cameras). These devices contain large cache memories, whose power consumption can reach about

50% of the total spent energy, from which leakage energy is the predominant fraction in current technologies. This paper proposes a technique to reduce leakage energy consumption in data caches on embedded systems, which is based on the fact that most stored bits take a logical value of zero. The proposed technique has been evaluated on a model of a contemporary high-end embedded microprocessor, namely the ARM Cortex A8 processor, executing a set of standard embedded benchmarks. Experimental results show that leakage energy savings reach about 40% with no IPC loss. [C1098]

"Cost-Efficient Partially-Parallel Irregular LDPC Decoder with Message Passing Schedule"

This paper proposes an improved message passing schedule for irregular LDPC decoder. Redundant memory accesses and column operations are removed by utilizing the characteristics of partial-parallel irregular LDPC decoding algorithm. As a result, the memory access frequency and hardware cost are efficiently reduced. According to the experimental results and comparison with existing work, proposed decoder provides a 30% hardware area reduction and a 36% power consumption saving with the same error correcting performance. [C1099]

"CT image reconstruction using hexagonal grids"

In the transversal plane CT exhibits a nearly rotational symmetric point spread function. Pixel sampling is typically done on Cartesian grids which are not ideal from a signal processing point of view. It is advantageous to use a hexagonal grid which can capture the same signal components with 13% fewer sampling points. In 3D one can even save 29%. We developed an efficient scheme to allow for arbitrarily shaped field of views and a hierarchical memory layout. The latter divides the images into small hexagonal subimages, similar to honeycombs, whose size is small enough to avoid cache misses on CPU-based algorithms or to be used on dedicated signal processing hardware such as GPUs (graphics processing units) or CBEs (cell broadband engines) that may be memory limited. As the final step a resampling algorithm converts from the hex domain to the Cartesian domain before storing images. We implemented a hyperfast CBE-based Feldkamp algorithm for the hexagonal lattice and compared its performance and its image quality to reconstructions using the standard Feldkamp algorithm. Both algorithms were run on the Dual Cell Based System (DCBS, Mercury Computer Systems, Berlin, Germany) on two CBEs with 3.2 GHz each. A 5123volume was reconstructed from 720 projections of 5122detector pixels. Image quality of the hexagonal approach was identical to the direct approach using the Cartesian lattice: the maximum relative difference between the MTFs was 1% and image noise differed by not more than 3%. The improvement in reconstruction speed was approximately 12% for the hexagonal grid which is slightly lower than the expectation. The complete reconstruction finished in about 10 s. With identical image quality reconstruction on the hexagonal grid is a simple and effective approach to significantly reduce memory consumption and reconstruction time. Existing reconstruction algorithms can be easily modified to operate in the hexagonal domain. [C1100]

"Half VDD Clock-Swing Flip-Flop with Reduced Contention for up to 60% Power Saving in Clock Distribution"

A new low clock swing flip-flop (F/F) is proposed. The existing low clock-swing F/F's consume high power, introduce speed penalty due to contention currents or require large silicon area due to separate well for substrate biasing. By reducing contention currents, our proposal efficiently mitigates those issues. Measurements and simulations are carried out based on a 90 nm CMOS process, demonstrating reductions of active power by 71%, area by 36% and delay by 35% compared to previous proposals. It is shown that the combination of a low- clock swing distribution tree with the new F/F can save up to 60% of the total clock system power. [C1101]

"Dual-Threshold Voltage Technique for Asynchronous Pre-Charge Full Buffer Linear-Pipelines"

Scaling the technology and reducing the feature size in integrated circuits have caused leakage power consumption to become one of the main challenges to the digital design. Dual-threshold CMOS circuit, which has both high and low threshold transistors in a single chip, can be used to deal with the leakage problem in high performance applications. This paper presents dual-threshold voltage technique for reducing leakage power dissipation of Pre-Charge Full Buffer asynchronous linear-pipelines while still maintaining high performance. We employed Folded Dependency Graph to produce a formal performance analysis. In order to reduce leakage power an algorithm for assigning a high threshold voltage is proposed. Results obtained indicate that our proposed technique can achieve on average 30% savings for leakage power, while there is no performance penalty. [C1102]

"SKIROC: A front-end chip to read out the imaging silicon-tungsten calorimeter for ILC"

That paper describes the new front-end ASIC "SKIROC" designed to read-out the technologic prototype of Si-W

calorimeter for ILC (International Linear Collider). The very high granularity of that new calorimeter designed for particle flow physics involves an unprecedented level of integration. Achieving the read-out of the 82 millions channel of the future calorimeter will be possible by using full integrated system on chip (SoC), as close as possible from the silicon detector. The SoC shall feature self trigger capability to ensure a early zero suppress and therefore avoid a huge data flow to the data acquisition. SKIROC also features a power pulsing supply to fit the beam structure of ILC and save power to improve compactness on the calorimeter by avoiding active cooling. A gain of two orders of magnitude is saved on the power consumption by using idle mode on the front-end electronics. The analogue data are converted into digital inside the ASIC and are stored in an internal RAM. The ASIC can be read out by token ring to reduce the number of lines in the detector. More than 1.3 million ASIC will be necessary to read out the whole calorimeter. [C1103]

"Logic design techniques for 65 to 45nm and below for reducing total energy and solving technology variations problems"

In sub-100nm technologies, leakage related problems are based on the standby current's exponential dependency on both, parameter scaling and parameter variation. Countermeasures, reducing the standby current and its spread can be classified into 3 categories: First, improved devices can reduce leakage sources by orders of magnitude, requiring completely new process steps. Next, performance and leakage can be traded off for conventional technologies. Low leakage devices control standby currents but their performance loss will reduce applicability. Finally, power management implements and controls circuits, where leakage and performance can be tuned at run-time, saving power on idle. This part of the special session will focus on design of new devices, reducing the negative dependence on channel length, oxide thickness, and body potential and improving the switching behavior. Afterwards, device and circuit level techniques tackling drawbacks of popular power management techniques are presented. For power gating, this means a reduction of the recovery current, a circuit style having a predictable timing and low area overhead, and a design stabilizing the interface towards ungated parts. For body biasing, body currents dominating reverse bias and even influencing forward bias have to be regarded and controlled. The gain of state assignment techniques, which are easy to use with conventional EDA tools, needs to be boosted to justify their application. [C1104]

"Reducing the Power Consumption in Networks-on-Chip through Data Coding Schemes"

This work investigates the reduction of power consumption in Networks-on-Chip (NoCs) through the reduction of transition activity using data coding schemes developed for bus-based systems and proposes a new coding scheme suitable for NoC-based systems. The estimation of the NoC power consumption was performed with basis on macromodels which reproduce the power consumption on each internal NoC module according to the transition activity on its input ports. Such macromodels were embedded in a system model and a series of simulations were performed, aiming to analyze the trade-off between the power savings due to coding techniques versus the power consumption overhead due to the encoding and decoding modules. The proposed coding scheme presented the best results for all of the simulated traffic patterns, when compared to other coding schemes found in the literature. [C1105]

"Power-Efficient and Low Latency Implementation of Programmable FIR filters Using Carry-Save Arithmetic"

This paper presents a new Programmable Finite-Impulse Resonse (FIR) digital filter scheme based on a low latency, power efficient architecture with reduced hardware complexity. In the proposed scheme, the input data is kept in bit-parallel form, while the coefficients enter the circuit in digit-serial form. The coefficient digits are encoded using the Modified Booth algorithm to reduce the partial products required for each multiplication. The structure of the filter is based on the technique of merging adjacent multiply-add units. The computation of the intermediate results is implemented using the carry-save arithmetic. Also, the coefficient digits of adjacent multiply-add units enter the filter in digit-skew form, while the input data sample remains stable until the relative output sample is produced. Thus, the proposed architecture results in a circuit with reduced hardware cost and lower power consumption, compared to other schemes presented in the bibliography. [C1106]

"Buffer Insertion and Sizing in Clock Distribution Networks with Gradual Transition Time Relaxation for Reduced Power Consumption"

Clock distribution network consumes a significant portion of the total chip power since the clock signal has the highest activity factor and drives the largest capacitive load in a synchronous integrated circuit. A new algorithm is proposed in this paper for buffer insertion and sizing in an H-tree clock distribution network. The objective of the algorithm is to minimize the total power consumption while satisfying the maximum acceptable clock transition time constraints at the leaves of the clock distribution network for maintaining high-performance. The

algorithm employs non-uniform buffer insertion and progressive relaxation of the transition time requirements from the leaves to the root of the clock distribution network. The proposed algorithm provides up to 30% savings in the total power consumption as compared to a standard algorithm with uniform buffer insertion aimed at maintaining uniform transition time constraints at all the nodes of a clock tree. [C1107]

"An Energy-Efficient Hybrid Data Collection Scheme in Wireless Sensor Networks"

We propose an energy-efficient hybrid data collection architecture based on controllably mobile infrastructure for a class of applications in which sensor networks provide both low-priority and high-priority data. High-priority data require a data delivery scheme with low latency and high fidelity. Meanwhile low-priority data may tolerate high-latency data delivery. Our approach exploits the design of a network that supports a hybrid data delivery scheme to enhance the network performance and reduces total network energy usage. In our system design two delivery schemes are deployed for purposes of comparison. The first is the traditional ad hoc approach to deliver high-priority data with high fidelity and low latency. The second presents a controllable infrastructure in the sensor field, which acts as low-priority data collection agent. Through simulations, we show that our proposed approach can provide substantial energy saving in this class of sensor application compared to the traditional multihop approach used alone. [C1108]

"Exergy Analysis for Performance Optimization of a Steam Turbine Cycle"

Exergy analysis of a 500 MWe steam turbine cycle is performed to identify the components that offer significant work potential saving opportunity. Criteria of performance relevant to the individual components are formulated. Exergy flows, exergy consumption due to irreversibilities and rational performance parameters for the turbine cycle and its components are computed by using plant operation data under different conditions. Energy efficiency of the turbine cycle is low due to large energy rejection, but the derived exergy efficiency of the turbine cycle is high due to low exergy rejection from the cycle. Part load operation exhibits lower energy efficiency due to higher energy rejection relative to net output. On the contrary, exergy rejection from the cycle relative to net output does not increase during low load operation. Results show that poor part load exergy efficiency is due to higher exergy destruction relative to net output. Higher pressure feed heaters deal with larger exergy and therefore, need more attention to improve cycle efficiency. Operation and maintenance decisions based on exergy analysis have proved to be more effective in reducing inefficiencies in operating power plant. Exergy-based approach of performance analysis will help practicing power engineers manage energy resources and environment better. [C1109]

"IPM motor drives for hybrid electric vehicles"

In the 21stcentury, global warming has become an important issue. Carbon dioxide (Co2) gas emissions should be reduced to preserve the correct air quality as per Kyoto protocol, implemented on February 16, 2005 by most of the countries. Modern human beings, who enjoy the fruits of electric energy technologies for climate controlled home and work place environments via air conditioners/heat pumps, and mass transportation using cars as necessities, cannot put up with the inconveniences of the past. In order to maintain and develop this energy consuming technologies, availability of sustainable energy sources and their effective uses through efficiency improvements are of paramount importance. Power electronics and electric motor drives are the enabling technologies crucial for industrial competitiveness in the world market place. One of the most valuable achievements in power electronics is to introduce degree of freedom to variable frequency from the fixed value of the generated electrical power supplies. Over 60 % of the generated energy is consumed by electric motors. Variable speed drive, which regulates the speed of the motor by controlling the frequency through smart uses of power electronics and control systems, can significantly reduce the energy consumption, particularly in heavy-duty cycle fan, pump, car and compressor systems. Thus improvements in efficiency of the drive systems are the most effective measures to reduce primary energy consumption; and thereby reduce Co2gas emissions, which cause global warming. The objective of this paper is to provide a short introduction to the recent emergence of high efficiency and high performance interior permanent magnet (IPM) synchronous motors. Highlights of IPM motors include wide spread application in Japanese made hybrid electric vehicles (HEV) sector to save precious electric energy, reduce gas emission and deter climate change. [C1110]

"Low Power Implementation of Decimation Filters in Multistandard Radio Receiver Using Optimized Multiplication-Accumulation Unit"

In this work, the implementation of decimation filters for multistandard wireless transceivers was optimized to reduce its power consumption. The power reduction is achieved through the usage of a MAC unit inside the filters that reduce the total activity and therefore the dynamic power. The multiplication function of the MAC unit is based on the Radix-4 modified-Booth algorithm for the generation of the partial products. For the partial

products summation, carry save addition was used. A Pipeline stage is then introduced to allow the accumulation of the result of the partial product summation step and the previous multiplications results. The power consumption of the different filters in the multistandard radio receiver was already optimized using the clock-gating technique at the circuit level. Experimental results show a power reduction of 9,48% when using the optimized MAC unit in comparison to the same architecture of the filters where only clock-gating technique is used and a total reduction of 61,98% compared to the implementation without any optimization. [C1111]

"High Efficient Intelligent Motor Control for a Hybrid Shunting Locomotive"

So many shunting locomotives are used all around the world. In order to save fuel and reduce pollution, they can be converted to Hybrid Electric Locomotives (HELs). In this paper, the selection and use of the induction electric machines for energy conversion in a plug in Hybrid Electric Locomotive is introduced. An old G12 locomotive is renovated and converted to a hybrid electric locomotive. To drive the locomotive, two induction motors are placed in two of the four axles of the locomotive. Due to the funding limits of the project, a prototype with two small motors was built. The G12 locomotive has four axles. Therefore, if the locomotive is mass produced, up to four motors with higher power ratings may be used that will give up to five times more torque and power. Instead of a 750 kVA diesel generator, a 80 kW diesel engine and a 50 kVA generator is used. Two 1200 volt, 300 ampere inverters with IGBT modules are used to drive each motor of the locomotive. The inverters are supplied by 480 volt, traction lead acid batteries. There are three ECUs for the motor and locomotive control. One is a master controller and to drive the LCD panels and the two others are for the inverter controllers. During the day, a shunting locomotive has around 60% idle time. In this condition, the locomotive consumes fuel and as its engine works at no load, the efficiency is zero and pollution is very high. A diesel engine in a hybrid technology either will be off or run at its rated torque and power. Therefore, its efficiency is high and at the same time the pollution and the fuel consumption are reduced a lot. The engine will be off unless the battery state of charge (SOC) reduced to a certain level. Moreover, instead of a 750 kVA diesel engine a 50 kVA diesel generator is used. [C1112]

"Optimal Power Train Design of a Hybrid Refuse Collector Vehicle"

Due to the stop-and-go drive cycle of refuse collector vehicles, hybrid power trains allow significant fuel saving. These power trains are very complex systems because of additional components like an electrical machine, an energy storage, etc. In order to exploit full potential of such systems optimal sizing of the components is essential. The sizing of the components can be seen as an optimization problem with the objectives "minimize fuel consumption" and "minimize vehicle weight". For the optimization scalable component models are required, which are presented here. The results of the optimization show that additional fuel saving combined with reduced weight is possible with optimally sized components compared to a heuristically designed vehicle. [C1113]

"Design of ultra low power CML MUXs and latches with forward body bias"

In this paper, a novel Forward Body Biasing (FBB) circuit is proposed for ultra low power Current Mode Logic (CML) MUXs and Latches. Through the proposed clocked-power FBB circuit, the supply voltage VDDand the dc-level of the differential inputs can be reduced significantly, while maintaining the original swing of differential outputs. Our architecture can reach power saving up to 60%, and 50% in average with slight penalty of area and frequency. The design methodology and performance analysis for FBB CML MUXs and Latches are presented. The same design concept can also be extended to logic circuits composed of differential input pairs. [C1114]

"A feasibility analysis of power-awareness and energy minimization in modern interconnects for high-performance computing"

High-performance computing (HPC) systems consume a significant amount of power, resulting in high operational costs, reduced reliability, and wasting of natural resources. Therefore, power consumption has become an increasingly important design constraint in high-performance clusters. In this regard, research on power-aware HPC has emerged. While most research has focused at understanding and utilizing applicationspsila behavior to scale down the CPU for energy savings, this paper demonstrates the positive impact of modern interconnects in delivering energy-efficiency in high-performance clusters. In this work, we first present the power-performance profiles of the Myrinet-2000 and Quadrics QsNetIIat the user-level and MPI-level in comparison to a traditional, non-offloaded Gigabit Ethernet. Such information enables us to devise a power-aware MPI runtime library that automatically and transparently performs message segmentation and re-assembly in order to increase energy savings. Secondly, by designing and evaluating a number of all-gather collectives, we argue that it is possible to increase the energy-efficiency of a cluster by optimizing its messaging layers. [C1115]

"Future mobile device interconnections"

The developed concept of ultra low power multi gigabit serial interface for mobile devices removes limits from mechanical design and device architectures. Power consumption of differential line drivers were reduced to 0.8 mW by lowering common-mode voltage of signals to 200 mV and using voltage source type drivers with 50-ohm output impedance to generate +-200 mV high-speed differential signal to receiver inputs. Lowering supply voltage to 200 mV and removing the parallel termination from receiver input are possible with voltage-source type driver when output impedance is matched to line impedance, providing additional 75% power saving without any change in receiver differential input signal. Zero idle power consumption of CMOS inverters makes them ideal single-ended drivers and receivers for short control messages using the same wires as high-speed drivers when no high-speed differential signaling is required. [C1116]

"Research on energy saving of Pharos Remote Monitoring and Control System based on wireless sensor network"

This paper studies energy saving of PRMCS (pharos remote monitoring and control system) based on WSN (wireless sensor networks). RTU (remote terminal unit), sensor networks of PRMCS, are installed in outdoor fieldwork, and limited in power, PRMCS saving energy become a key problem. We develop a low power consumption method for PRMCS in which LEACH route algorithm and Sleep-Waken model dispatch are designed to reduce power consumption. Test results indicate that for RTU and sensor networks, our solution method can save over 170% energy compared with traditional method. [C1117]

"Runtime system support for software-guided disk power management"

Disk subsystem is known to be a major contributor to the overall power budget of large-scale parallel systems. Most scientific applications today rely heavily on disk I/O for out-of-core computations, checkpointing, and visualization of data. To reduce excess energy consumption on disk system, prior studies proposed several hardware or OS-based disk power management schemes. While such schemes have been known to be effective in certain cases, they might miss opportunities for better energy savings due to their reactive nature. While compiler based schemes can make more accurate decisions on a given application by extracting disk access patterns statically, the lack of runtime information on the status of shared disks may lead to wrong decisions when multiple applications exercise the same set of disks concurrently. In this paper, we propose a runtime system based approach that provides more effective disk power management. In our scheme, the compiler provides crucial information on the future disk access patterns and preferred disk speeds from the perspective of individual applications, and a runtime system uses this information along with current state of the shared disks to make decisions that are agreeable to all applications. We implemented our runtime system support within PVFS2, a parallel file system. Our experimental results with four I/O-intensive scientific applications indicate large energy savings: 19.4% and 39.9% over the previously-proposed pure software and pure hardware based schemes, respectively. We further show in this paper that our scheme can achieve consistent energy savings with a varying number and mix of applications and different disk layouts of data. [C1118]

"FKEE Approaches in Solving Energy Wasting Occurrences in UMP's Lecture Halls"

It is important to note that air-conditioning and mechanical ventilating system (ACMV) and lighting system consume the most electrical energy in a building in Malaysia. In University Malaysia Pahang (UMP), due to the nature of the buildings, split units air-conditioning systems are used in the faculty office blocks and the lecture halls. It is found that a major portion of the energy consumed came from the lecture hall buildings. The appliances are running on a fixed setting throughout the day, and are sometimes turned on when they should be off. This contributes to energy wastage. The energy wasted can be reduced by controlling the appliances and system using a control system while maintaining a comfortable and safe environment in the building. This paper presents a preliminary study on energy wastage in a UMP lecture hall. In this case study, a data logger is installed to collect data for further analysis on energy consumption in the hall. Also reported in this paper is the preliminary design of a energy saving control system for air-conditioning and lighting system that can be used in lecture halls. [C1119]

"Adaptive Spatial Resolution Control Scheme for Mobile Video Applications"

Video streams can be compressed to fit the available network by controlling three factors; temporal resolution, spatial resolution and picture quality. Controlling picture quality by modifying the quantization parameter (QP) is most widely used. But we demonstrate that reducing the spatial resolution is more effective in a low bit-rate environment, and we show how to find the optimal spatial resolution for the available bandwidth. Varying the spatial resolution is especially effective 1) when the bandwidth between the video encoder and the displaying

device varies considerably with time, which is the case in wireless networks, and 2) when the display device is sensitive to energy saving. Both of these considerations are met by a portable media player which is displaying streaming video content transmitted by a remote video server through a wireless network. If the bit-rate is low, our technique can improve the picture quality by more than 1 db compared to adjustment of QP, accompanied by a halving of energy consumption. [C1120]

"Energy Saving Based on CPU Voltage Scaling and Hardware Software Partitioning"

We examine the possible energy savings by mapping critical software functions from a microprocessor to configurable logics. A system-on-a-chip containing configurable logic is now commercially available. The configurable logic is typically intended to implement peripherals and co-processors without increasing chip count. We show that reduced software energy is an extra significant benefit, making such chips even more useful. We identify critical software functions of an application and implement them in the configurable logic such that the application can complete sooner, allowing us to put the system in a low-power state for longer periods, thus reducing energy. We use estimation-based approach for a hypothetical device having a 32-bit MIPS-extension processor plus on-chip configurable logic, yielding energy savings of 40%, increasing to 54% assuming voltage scaling. [C1121]

"Time Division Flooding Synchronization Protocol for Sensor Networks"

Clock synchronization is an essential service for various applications in wireless sensor networks (WSNs). Most of available synchronization protocols are based on CSMA MAC scheme. They are energy inefficient in dense sensor networks. Despite many power-saving TDMA MAC protocols have been proposed, few of them are qualified to flood synchronization messages. The novel one here adopts a carefully designed time division flooding scheme, which divides time into slots and assigns each node a unique one for transmitting synchronization packets. In this way, the active duration of each node can be dramatically reduced. The new slot allocation policy guarantees active periods of nodes along the forwarding paths be scheduled successively, so synchronization packets can be spread out in a short time. Besides, a special clock frequency skew compensation technique is employed to prolong the re-synchronization interval. Simulation shows that our protocol achieves high energy efficiency and fast convergence speed. [C1122]

"Cooperative Dynamic Voltage Scaling using Selective Slack Distribution in Distributed Real-Time Systems"

This work is based on the observation that existing energy management techniques for mobile devices, such as dynamic voltage scaling (DVS), are non-cooperative in the sense that they reduce the energy consumption of a single device, disregarding potential consequences for other constraints (e.g., end-to- end deadlines) and/or other devices (e.g., energy consumption on neighboring devices). This paper argues that energy management in distributed real-time systems has to be end-to-end in nature, requiring a coordinated approach among communicating devices. A cooperative distributed energy management technique (Co-DVS) is proposed that: i) adapts and maintains end-to-end latencies within specified timeliness requirements (deadlines); and ii) enhances energy savings at the nodes with the highest pay-off factors that represent the relative benefits or significance of conserving energy at a node. The proposed technique employs a feedback-based approach to dynamically distribute end-to-end slack among the devices based on their pay-off factors. [C1123]

"Power Consumption Evaluation of Sleep Mode in the IEEE 802.16e MAC with Multi Service Connections"

In the sleep mode, a mobile subscribe station (MSS) sleeps for a sleep interval and wakes up at the end of this interval in order to check buffered packet(s) at base station (BS) destined to it. If there is no packet, the MSS increases the sleep window up to the maximum value or keeps it unchanged and sleeps again. In this paper, we study the effect of presence of multi service connections with different power saving classes (PSCs) on power consumption for IEEE 802.16e nodes while operating in the sleep mode. Using multi service connections may result in overlapping of availability and unavailability intervals and reducing the effectiveness of power saving mode of the subscriber. [C1124]

"A Distributed Topology Control Algorithm in the Presence of Multipath Propagation"

Each node in a wireless multihop network can adjust the power at which it makes its transmissions and thus change the topology of the network by choosing the neighbors with which it directly communicates. Many previous algorithms for distributed topology control have assumed an ability at each node to deduce some spatial information such as the direction and the distance of its neighbor nodes with respect to itself. However, such a

deduction of spatial information cannot be relied upon in a multipath environment where different paths of a signal may have different loss characteristics and none of the paths may be line-of-sight. In this paper, we present Step Topology Control (STC), a simple distributed topology control algorithm which reduces power consumption while preserving the connectivity of a heterogeneous sensor network in a multipath environment. The STC algorithm avoids the use of GPS devices and also makes no assumptions about the distance and direction between neighboring nodes. We provide analytical proofs of the relationship between the STC algorithm and a cone-based topology control algorithm. We present a detailed simulation- based comparative analysis of the energy savings achieved by the STC algorithm and previously known algorithms that also seek to reduce power consumption while preserving connectivity. The results show that the STC algorithm performs significantly better than other algorithms, especially in the presence of radio irregularities and multipath propagation. In addition, the STC algorithm scales better than other algorithms in performance and in fact, is more effective with increasing numbers of nodes. [C1125]

"Nonlinear Control of VAVAC System via Feedback Linearization"

This paper presents the design of a nonlinear controller for variable air volume air conditioning (VAVAC) by feedback linearization approach. VAVACs are aimed at reducing building energy consumption while maintaining the primary role of air conditioning. The temperature of the space is maintained at a constant level by establishing a balance between the cooling load generated in the space and the supply air delivered to meet the load. The dynamic model of VAVAC is formulated as a MIMO bilinear system. Feedback linearization method is applied for decoupling and linearization of the non linear model. Simulation results are presented to demonstrate the potential of keeping comfort and save energy by this methodology. The results obtained with the conventional controller and feedback linearizing controller are compared, and superiority of the proposed approach is established. [C1126]

"Power-efficient FSM mapping in FPGAs through SEMB dormancy control"

Controllers implemented as finite-state machines (FSMs) occupy a major portion of FPGA designs. These FSMs can be implemented on synchronous embedded memory blocks (SEMBs) in current FPGAs. This approach, in addition to reducing considerable amount of power, also has several implementation benefits. In this research, we propose to further minimize the power consumed by the FSMs that are mapped to the SEMBs. We present an algorithm that maps the FSM outputs across the SEMBs based on its transition probabilities and thereby maximizes the dormancy of the SEMBs. For a given FSM as a state transition table, the algorithm determines for each transition in the table, the combination of inputs, outputs and state bits which contribute to the dormant transitions of the SEMB. Further, we develop a flow to determine the net power saved by this approach by computing the power consumed in the enable control logic and report the power savings for a variety of microprocessor models and MCNC benchmark circuits. Experimental results show a reduction of 8% to 21% in power compared to the SEMB based FSM technique and that it consumes 30% to 74% less dynamic power compared to the traditional LUT/FF implementation. [C1127]

"A low-power adiabatic content-addressable memory"

This paper presents a novel CAM (content- addressable memory) using CPAL (complementary pass- transistor adiabatic logic) circuits. All circuits except for CAM cells are realized using CPAL circuits. The match-lines are driven using bootstrapped NMOS switches. The charge of large node capacitance on match-lines, bit-lines, word-lines, and address-lines is well recovered in fully adiabatic manner. The power consumption of the proposed CAM is greatly reduced. Simulations show that the proposed CAM attains energy saving of 84% to 92% for search operation compared to the conventional CMOS implementation from 10 MHz to 100 MHz. [C1128]

"Dual diode-Vth reduced power gating structure for better leakage reduction"

Leakage has become one of the most dominant factors of power management and signal integrity of nanometer scale integrated circuits. Recently, power gating structures has proven to be effective in controlling leakage. In this paper an alternative dual diode-Vth reduced power gating structure is proposed for better reduction of leakage currents, especially for low-power, high-performance portable devices. The proposed technique maintains an intermediate power saving state as well as the conventional power cut-off state. Experimental results have demonstrated that the proposed technique can significantly reduce leakage current and associated power consumptions during the HOLD and CUT-OFF power saving modes. It has also been demonstrated that the proposed technique significantly reduces ground bounce due to power mode transition. [C1129]

"High performance CMOS symmetric low swing to high swing converter for on-chip interconnects"

This paper reports a symmetric high performance, low to full swing level converter (sib-driver) for recovering signal levels at the receiver end of the global interconnects with large capacitive loads. The proposed sib-driver provides a matching receiver for the up-down low swing voltage driver (UDLD) signaling style for driving the global interconnect lines. When implemented on 0.13 mum CMOS 1.2 V technology, the sib-driver performs 23% faster, and reduces the power delay product and energy delay product by 25.5%, (having similar active area, of 19.6 mum2), when compared with a counterpart up low swing voltage driver (ULD) level converter (lc-driver). This paper also proposes several other level converter receivers, each with different performance energy saving trade off. The paper also provides comparative performance evaluation of the various proposed level converters and lc-driver. [C1130]

"Heuristic-Path and Observer based Low-Energy Scheduling Algorithms for Body Area Network Systems"

In this paper, we propose novel low-energy static and dynamic scheduling algorithms for the heterogeneous Body Area Network (BAN) systems, where task graphs have deadlines (timing constraints) and precedence relationships to satisfy. Our proposed algorithms, with low computational complexities, use the novel "path information track-and-update" scheme to distribute slack over tasks such that the overall energy consumption is minimized, and an observer mechanism to guarantee the application constraints. Our dynamic scheduling algorithm utilizes the results from the static scheduling algorithm and attempts to aggressively reduce the energy consumption. Simulations for the task graph for a typical BAN application show that our scheduling algorithms achieve better energy savings with less than 5% of the computational time, compared with the recent heterogenous multiprocessor scheduling algorithms. [C1131]

"Iterative Radix-8 Multiplier Structure Based on a Novel Real-time CSD Recoding"

Real-time implementation of many digital signal processing (DSP) algorithms and multimedia applications is performance limited by the available speed, energy efficiency, and area requirement of multiplication. This is exacerbated in handheld multimedia devices due to the small size and limited battery lifetimes. In our previous work, we introduce a novel canonical signed digit (CSD) iterative multiplier structure in which the conversion from 2's complement to CSD representation is implicitly implemented in real-time. In this work, we further improve the iterative multiplier performance by introducing explicit radix-8 hardware support in which the multiplier is shifted by one octal digit in each iteration as opposed to only one or two bits. Thus, this new structure further reduces the power consumption while simultaneously increasing the computational bandwidth significantly with only a small sacrifice in area consumption. This new design also uses a bypass technique to further reduce the need for devices such as carry save adder (CSA) arrays and adder trees for partial product reduction operations. Therefore, the new structure introduced here greatly improves the multiplier throughput and energy efficiency. Moreover, the number of iterations required to complete a fixed length multiply is data dependent as a result of a novel variable shifting technique; hence there is no energy and time overhead expended for unnecessary iterations as observed in multipliers where the number of iterations is fixed. Our results show that this new iterative structure delivers significant performance improvements with respect to speed, area, and power consumption relative to previous iterative multiplier designs. [C1132]

"Variation-Aware Low-Power Buffer Design"

Process variation (PV) is a consequence of manufacturing imperfections, which may lead to degraded performance or higher leakage power. In this paper, we focus on the design of an intelligent buffer that logically reorders the entries in FIFO buffer to minimize overall leakage power consumption. The buffer architecture, called IntelliBuffer, has been designed and evaluated in 90 nm and 32 nm CMOS technology. Our synthesized results show that our proposed design is as fast as a conventional buffer structure, while providing the ability to reduce power consumption significantly. When our buffer was used in a network-on-chip (NoC) implementation, we obtained 24% leakage savings at 90 nm, and savings of 28% at 32 nm. To further validate the efficacy of our proposed design, we incorporated IntelliBuffer into ViChaR, a recently introduced dynamic buffer management system for NoC routers. Experimental results indicate a marked reduction in ViChaR's leakage power consumption (21% at 90 nm) when IntelliBuffer is employed. [C1133]

"Voltage island-driven floorplanning"

Energy efficiency has become one of the most important issues to be addressed in today's system-on-a-chip (SoC) designs. One way to lower the power consumption is to reduce the supply voltage. Multi-supply voltage (MSV) is thus introduced to provide higher flexibility in controlling the power and performance trade-off. In region-based MSV, circuits are partitioned into "voltage islands" where each island occupies a contiguous physical space and operates at one supply voltage. These tasks of island partitioning and voltage level

assignments should be done simultaneously in the floorplanning process in order to take those important physical information into consideration. In this paper, we consider this core-based voltage island driven floorplanning problem including islands with power down mode, and propose a method to solve it. Given a candidate floorplan solution represented by a normalized Polish expression, we are able to obtain optimal voltage assignment and island partitioning (including islands with power down mode) simultaneously to minimize the total power consumption. Simulated annealing is used as the basic searching engine. By using this approach, we can achieve significant power savings (up to 50%) for all data sets, without any significant increase in area and wire length. Our floorplanner can also be extended to minimize the number of level shifters between different voltage islands and to simplify the power routing step by placing the islands in proximity to the corresponding power pins. [C1134]

"Sizing and placement of charge recycling transistors in MTCMOS circuits"

A downside of using Multi-Threshold CMOS (MTCMOS) technique for leakage reduction is the energy consumption during transitions between sleep and active modes. Previously, a charge recycling (CR) MTCMOS architecture was proposed to reduce the large amount of energy consumption that occurs during the mode transitions in power-gated circuits. Considering the RC parasitics of the virtual ground and VDD lines, proper sizing and placement of charge-recycling transistors is key to achieving the maximum power saving. In this paper, we show that the sizing and placement problems of charge-recycling transistors in CR-MTCMOS can be formulated as a linear programming problem, and hence, can be efficiently solved using standard mathematical programming packages. The proposed sizing and placement techniques allow us to employ the CR-MTCMOS solution in large row-based standard cell layouts while achieving nearly the full potential of this power-gating architecture, i.e., we achieve 44% saving in switching energy due to the mode transition in CR-MTCMOS compared to standard MTCMOS. [C1135]

"A Flexible Design Flow for a Low Power RFID Tag"

This paper describes the implementation of a passive RFID tag targeting low power implementation, which works on 915 MHz UHF frequency. The proposed architecture allows customizing the command sets implemented inside its digital block, according to the target application needs, saving area and reducing power consumption. A flexible design flow is proposed for the customization, verification and synthesis of the digital block, targeting low power requirements. [C1136]

"Co-Ordinated Adaptive Power (CAP) Managemet for Wireless Sensor Networks"

In order to have energy optimized sensor nodes a low power hardware design is the basic requirement, on that low power device applying sleep scheduling algorithms further energy savings can be achieved. CAP i.e.co-ordinated adaptive power management is a technique which is applied during active periods of the sensor nodes so that energy consumption is further reduced and lifetime can be increased. CAP management is used to save energy consumption of processing unit and communication unit of a sensor node in a co-ordinated manner. Both of these units are dynamically adapted to a particular operating mode that depends on the workload of the node. Co-ordinating computational and communication unit together gives better power optimization by removing the need for multiple hardware interfaces and by having a centralized power management unit. This kind of coordination also reduces the possibility of packet loss due to limited buffer sizes. [C1137]

"Lightweight Signal Processing in Sensor Node for Real-time Traffic Monitoring"

Wireless sensor network may be used for real-time traffic monitoring. In this paper, we describe the design and implementation of a practical wireless traffic information collection node (TICoN). We propose a specific lightweight adaptive signal processing algorithm based on matched filter, namely AEMFA, for traffic monitoring. We provide solutions to embed this signal processing algorithm in resource-limited sensor node, to reduce power consumption. We also propose a traffic volume detection algorithm, namely TVDA, based on AEMFA. Experimental results show that AEMFA algorithm performs well in sensor node. The algorithm is efficient both in traffic volume detection with an accuracy of 90%, and in energy saving up to 80%. [C1138]

"Analysis and Study of the Relationship of Energy Consumption and CPU buffer of a wireless sensor node"

In order to maximize the lifetime of a sensor node, circuits, architecture, algorithms and protocols must be energy efficient. There are many methods to reduce the energy of a node, among them dynamic power manage (DPM) and dynamic voltage supply (DVS) are two effective mechanisms to achieve energy saving. This paper presents the impacts of buffer length and buffer overflow probability on CPU energy. Additional energy savings can be attained by increasing the buffer length without sacrificing performance and reducing an order of

magnitude of buffer overflow probability. [C1139]

"An Exponential Energy Saving Strategy to Wireless Sensor Network"

Energy saving strategies for wireless sensor networks, that change the sleeping time of sensor nodes as function of activity level of the sensing field, in order to improve the trade-off between the average network energy consumption and the average data delivery delay is presented in this paper. The exponential increase or decrease of sleeping time considers the event detection frequency in the sensing field as well as the level of activity of sensor forwarding sensing data of the others sensor nodes. These strategies have been simulated and the average data delivery delay was compared with the one produced by another strategy recently reported. The simulation results show that the proposed strategy reduces the energy consumption of the sensor nodes with small degradation of the data delivery delay. [C1140]

"Efficient Energy Saving in Wireless Sensor Networks Through Hierarchical-based Clustering"

Prolonged network lifetime, scalability, and load balancing are important requirements for many wireless sensor network applications. Clustering sensor nodes is an effective approach for achieving these goals. In this paper, we propose a Distributed Energy-efficient Clustering-based Hierarchy Protocol (DECHP), which distributes the energy dissipation evenly among all sensor nodes to improve network lifetime and average energy savings. The performance of DECHP is then compared to different clustering-based schemes. Simulation results show that DECHP reduces overall energy consumption and improves network lifetime over its comparatives. [C1141]

"Evaluating voltage islands in CMPs under process variations"

Parameter variations are a major factor causing power-performance asymmetry in chip multiprocessors. In this paper, we analyze the effects of with-in-die (WID) process variations on chip multicore processors and then apply a variable voltage island scheme to minimize power dissipation. Our idea is based on the observation that due to process variations, the critical paths in each core are likely to have a different latencies resulting in core-to-core (C2C) variations. As a result, each core can operate correctly under different supply voltage levels, achieving an optimal power consumption level. Particularly, we analyze voltage islands at different granularities ranging from a single core to a group of cores. We show that the dynamic power consumption can be reduced by up to 36.2% when each core can set its individual supply voltage level. In addition, for most manufacturing technologies, significant power savings can be achieved with only a few voltage islands on the whole chip: a single customized voltage setting can reduce the power consumption by up to 31.5%. Since the nominal operating frequency remains unchanged after the modifications, our scheme incurs no performance overhead. [C1142]

"Dynamically compressible context architecture for low power coarse-grained reconfigurable array"

Most of the coarse-grained reconfigurable array architectures (CGRAs) are composed of reconfigurable ALU arrays and configuration cache (or context memory) to achieve high performance and flexibility. Specially, configuration cache is the main component in CGRA that provides distinct feature for dynamic reconfiguration in every cycle. However, frequent memory-read operations for dynamic reconfiguration cause much power consumption. Thus, reducing power in configuration cache has become critical for CGRA to be more competitive and reliable for its use in embedded systems. In this paper, we propose dynamically compressible context architecture for power saving in configuration cache. This power-efficient design of context architecture works without degrading the performance and flexibility of CGRA. Experimental results show that the proposed approach saves up to 39.72% power in configuration cache with negligible area overhead. [C1143]

"Cluster restructuring scheme for wireless sensor networks"

Limited by application and node structure, wireless sensor networks (WSNs) call for energy effective algorithms. Therefore, a cluster restructuring scheme (CRS) applicable to most cluster based hierarchical network architectures is presented. Using this scheme, no position information of any sensor node is needed. According to the received signal intensity, each cluster member selects a data relay node within the cluster to set up an energy-saving data relay link. Depending on the delay constraints, each cluster member forwards data either to the cluster head or to the data relay node automatically. Forwarding data through the data relay links not only decreases the transmission energy, but reduces link interferences and energy consumption for data receiving of some neighbor nodes. Simulation results show that, in a round of data transmission, the CRS reduces the average energy consumption of the cluster heads by up to 90% and of the cluster members by up to 97% in a cluster of 30 nodes. [C1144]

"Performance Analysis of Energy Saving Scheme with Extra Active Period for LAN Switches"

A huge number of LAN switches are currently in use worldwide, so ways in which they can save energy are of great practical interest. A simple way to save power is to switch the interface to sleep mode when no packets are buffered, and to keep it in active mode while there are packets to be transmitted. This would appear to be the most effective energy saving scheme. However, mode switching gives rise to an in-rush current, which causes electrical damage to devices. This problem arises from over-frequent mode switching, which should be avoided. Thus, the main objective is to develop a way to reduce the number of mode switchings that result in quite short duration sleep modes, as these do not contribute so much to energy saving but lead to damage to the device. To this end, a method is adopted which keeps the interface in active mode for an extra period after all packets are flushed out from the buffer; this is the "extra active period". This scheme protects the device at the expense of energy saving efficiency. In this paper, the scheme is evaluated analytically in terms of its power reduction ratio and the frequency of mode changes, by modifying the M/M/1 and IPP/M/1 queuing models. The numerical results show how the duration of the extra active period degrades the energy saving performance while successfully reducing the number of mode changes. These results will enable LAN switches to be designed with energy saving in mind yet within the constraints of device characteristics. [C1145]

"Thermal Effects with Leakage Power Considered in 2D/3D Floorplanning"

Leakage power is becoming a key design challenge in current and future CMOS designs. Due to technology scaling, the leakage power is rising so quickly that it largely elevates the die temperature. In this paper, we deeply investigate the impact of leakage power on thermal profile in 2D and 3D floorplanning. Our results show that chip temperature can increase by about 11 V in 2D design and 68 V for 3D case with leakage power considered. Then we propose a thermal-driven floorplanning flow integrated with an iterative leakage-aware thermal analysis process to optimize chip temperature and save leakage power consumption. Experimental results show that for 2D design, the max chip temperature can be reduced by about 8 "C and the proportion of leakage power to total power can be reduced from 19.17% to 11.12%. The corresponding results for 3D are 60 degC temperature reduction and 16.3% less leakage power proportion. [C1146]

"Energy-Aware Scheduling of Real-Time Tasks in Wireless Networked Embedded Systems"

Recent technological advances have opened up several distributed real-time applications involving battery-driven embedded devices with local processing and wireless communication capabilities. Energy management is the key issue in the design and operation of such systems. In this paper, we consider a single-hop networked real-time embedded system where each node supports both dynamic voltage scaling (DVS) and dynamic modulation scaling (DMS) power management techniques to tradeoff time for energy savings. In this model, we address the problem of scheduling periodic complex tasks where each task consists of several precedence constrained message passing sub-tasks. Our contributions towards this problem are twofold. First, we analyze the system level energy-time tradeoffs considering both the computation and communication workloads by defining a novel energy gain metric. We then present static (centralized) and dynamic (distributed) energy gain based slack allocation algorithms which reduce the total energy consumption, while guaranteeing the ready time, deadline and precedence constraints. We compare the performance of the proposed algorithms with several baseline algorithms through simulation studies. Our results show that the proposed algorithms perform significantly better than the baseline algorithms for the simulated conditions. Finally, we identify several interesting energy-aware research problems in the area of networked real-time embedded systems. [C1147]

"Energy-Aware Scheduling for Streaming Applications on Chip Multiprocessors"

Streaming applications have become increasingly important and widespread, and they will be running on soon-to-be-prevalent chip multiprocessors (CMPs). We address the problem of energy-aware scheduling of streaming applications, which are represented by task graphs, on a CMP using on/off and dynamic voltage scaling (DVS) on a per-processor basis. The goal is to minimize the energy consumption of streaming applications while satisfying two typical quality-of-service (QoS) requirements, namely, throughput and response time. To the best of our knowledge, this paper is the first work to tackle this problem. We make a key observation: the trade-off between static power and dynamic power should play a critical role in both parallel processing and pipelining that are used to reduce energy consumption in the scheduling process. Based on this observation, we propose two scheduling algorithms, Scheduling 1D and Scheduling 2D, for linear and general task graphs, respectively. The proposed algorithms exploit the difference between the two QoS requirements and perform processor allocation, task mapping and task speed scheduling simultaneously. Experimental results show that the proposed algorithms can achieve significant energy savings (e.g., 24% on average for 70 nm technology) over the baseline that only considers the response time requirement. [C1148]

"On the Data Dissemination in WSNs"

Data dissemination has been put forward as an important mechanism for WSN. The dissemination schemes allow sink nodes to diffuse information in the network. It is known as an energy-consuming phase. In this paper, we propose to resolve this problem in two steps: firstly using a localized self-organization scheme which generates a non-directed backbone; secondly, sink node sends a request through this backbone to create a directed dissemination structure in the network. Our scheme effectively reduces the data traffic during the dissemination phase and saves energy when compared to other schemes. It is also extended to run properly in multiple sinks and mobile sink scenarios. The results also put forward the benefits of using a self-organization scheme for data dissemination. [C1149]

"Power Reduction Technique for Successive-Approximation Analog-to-Digital Converters"

This paper addresses the problem of reducing power consumption in successive approximation ADC architecture as a building block of power-aware electronic devices. Two binary search control algorithms, intended to decrease the total ADC's consumed energy during the conversion cycle are proposed in this paper. Both algorithms take advantage of sensor input signal properties and dynamically reduce the number of conversion steps in order to save energy. Metrics for evaluating energy efficiency of the conversion process, called energy reduction factor, Feris involved. Simulation results show that energy saving per conversion cycle of up to 25 % can be obtained. [C1150]

"Power Scheduling for Wireless Sensor and Actuator Networks"

We previously presented a model for some wireless sensor and actuator network (WSAN) applications based on the vector space tools of frame theory. In this WSAN model there is a weight associated to each sensor-actuator link denoting the importance of that communication link to the actuation fidelity. These weights were shown to be useful in pruning away communication links to reduce the number of active channels. Inspired by recent work in power scheduling for decentralized estimation, we investigate the optimal allocation of system resources for achieving a desired actuation fidelity. In this scheme, each sensor acquires a noisy observation and sends a message to a subset of actuators using an MQAM transmission strategy. The message sent on each sensor-actuator communication link is quantized with a variable number of bits, with the number of bits optimized to minimize the total network power consumption subject to a constraint on the actuation distortion. We show analytically and verify through simulation that performing this optimal power scheduling can yield significant power savings over communication strategies that use a fixed number of bits on each communication link. [C1151]

"Power Reduction in Network Equipment Through Adaptive Partial Reconfiguration"

We introduce a new approach to reducing FPGA power consumption. By exploiting the time varying nature of a systems environment, we are able to extract power consumption savings. We do this by closely tracking environmental changes and adapting the implementation accordingly using partial reconfiguration. We chose network infrastructure equipment to provide the context for the work since it is a significant consumer of FPGAs and is deployed in diverse environments. The network industry is also very interested in reducing FPGA power consumption as part of a major system wide effort, since it faces regulatory pressure, environmental concerns and rising electricity bills. We present a new experimental framework for measuring the power consumption of FPGA cores. The framework is used in an illustrative case study of how the approach works with a Viterbi decoder. The experiments give encouraging results and show that significant savings in power consumption can be obtained. [C1152]

"Scheduled PSM for Minimizing Energy in Wireless LANs"

Power conservation is a general concern for mobile computing and communication. In this paper, we investigate the performance of the current 802.11 power saving mechanism (unscheduled PSM) and demonstrate that background network traffic can have a significant impact on the power consumption of mobile stations. To improve power efficiency, a scheduled PSM protocol based on time slicing is proposed in this paper. The protocol adopts the mechanism of time division, schedules the access point to deliver pending data at designated time slices, and adaptively adjusts the power state of the mobile stations. The proposed scheme is near theoretical optimal for power saving in the sense that it greatly reduces the effect of background traffic, minimizes the station idle time, and maximizes its energy utilization. Comprehensive analysis and simulations are conducted to evaluate the new protocol. Our results show that it provides significant energy saving over the unscheduled PSM, particularly in circumstances where multiple traffic streams coexist in a network. Moreover, it achieves the saving at the cost of only a slight degradation of the one-way delay performance. [C1153]

"Better leakage reduction by exploiting the built-in MOSFET-Vth characteristics"

Leakage has become one of the most dominant factors of power management and signal integrity of nanometer scale integrated circuits. Recently, power gating structures has proven to be effective in controlling leakage. In this paper an alternative dual-Vth reduced power gating structure is proposed for better reduction of leakage currents, especially for low-power, high-performance portable devices. The proposed technique maintains an intermediate power saving state as well as the conventional power cut-off state. Experimental results have demonstrated that the proposed technique can significantly reduce leakage current and associated power consumptions during the hold and cut-off power saving modes. It has also been demonstrated that the proposed technique significantly reduces ground bounce due to power mode transition. [C1154]

"A Delay Constraint Energy Saving algorithm in IEEE 802.16e wireless man"

Saving energy is an important issue in IEEE 802.16e Broadband Wireless Access (BWA) networks. Sleep-mode operation in the IEEE 802.16e effectively saves energy consumption in order to extend life time of a Mobile Subscribe Station (MSS). However, frame response delay is another important performance metric. The constraint is that the sleep- mode operation can reduce consumed energy, but it must guarantee reasonable frame response delay. In this paper, we evaluate in details the effects of maximum sleep interval on energy consumption and on frame response delay of MSS in the sleep-mode operation. Furthermore, we propose a Delay Constraint Energy Saving (DCES) algorithm to quickly determine maximum sleep interval which minimizes energy consumption with frame response delay constraint. The validation of DCES algorithm suggests that the algorithm can provide a potential guidance to energy saving. [C1155]

"PSM-throttling: Minimizing Energy Consumption for Bulk Data Communications in WLANs"

While the 802.11 power saving mode (PSM) and its enhancements can reduce power consumption by putting the wireless network interface (WNI) into sleep as much as possible, they either require additional infrastructure support, or may degrade the transmission throughput and cause additional transmission delay. These schemes are not suitable for long and bulk data transmissions with strict QoS requirements on wireless devices. With increasingly abundant bandwidth available on the Internet, we have observed that TCP congestion control is often not a constraint of bulk data transmissions as bandwidth throttling is widely used in practice. In this paper, instead of further manipulating the trade-off between the power saving and the incurred delay, we effectively explore the power saving potential by considering the bandwidth throttling on streaming/downloading servers. We propose an application-independent protocol, called PSM-throttling. With a quick detection on the TCP flow throughput, a client can identify bandwidth throttling connections with a low cost Since the throttling enables us to reshape the TCP traffic into periodic bursts with the same average throughput as the server transmission rate, the client can accurately predict the arriving time of packets and turn on/off the WNI accordingly. PSM-throttling can minimize power consumption on TCP-based bulk traffic by effectively utilizing available Internet bandwidth without degrading the application's performance perceived by the user. Furthermore, PSM-throttling is client-centric, and does not need any additional infrastructure support. Our lab-environment and Internet-based evaluation results show that PSM-throttling can effectively improve energy savings (by up to 75%) and/or the QoS for a broad types of TCP-based applications, including streaming, pseudo streaming, and large file downloading, over existing PSM-like methods. [C1156]

"A Reconfigurable CAM Architecture for Network Search Engines"

A novel reconfigurable content addressable memory, called RCAM, is proposed that supports on-the-fly reconfiguration between CAM and TCAM. The area overhead of the proposed RCAM cell is only 5.6% when compared to conventional TCAM. This overhead is compensated by area saving due to removal of the priority encoder. Other features of our architecture include reconfigurability, and better overall performance and power. To achieve these we incorporated two novel techniques: (i) a hybrid CAM/TCAM architecture that allows user to pre-define CAM/TCAM cell behavior in each bit or word position and ultimately curtail the overall power consumptions of memory unit: and (ii) a wired-AND technique by which we can completely eliminate the sorting requirement and thus significantly reduce the update time. A 4 Kb RCAM architecture was implemented using 0.18 mum CMOS technology. The simulations indicate a search time of 6.15 ns, i.e. capability of handling about five OC-192 at wire speed. [C1157]

"Early-Pruning K-Best Sphere Decoder for MIMO Systems"

The sphere decoding algorithm has been used for maximum likelihood detection in MIMO systems, and the K-Best sphere decoding algorithm is proposed for MIMO detections for its fixed complexity and throughput. However, to achieve near-ML performance, the K needs to be sufficiently large, which leads to large

computational complexity and power consumption in hardware implementation. In this paper, we have developed some efficient early-pruning schemes, which can eliminate the survival candidates that are unlikely to become ML solution at early stages. Therefore, the computational complexity and the power consumption can be significantly saved. The simulation results show that for the 4ΓŕB—4 64QAM MIMO system, totally 55% computational complexity (or power consumption) can be reduced by applying our proposed schemes. [C1158]

"Low Power Multipliers Using Enhenced Row Bypassing Schemes"

In this paper, we proposed two novel low power multipliers based on enhanced row bypassing schemes. The essence of the power saving idea is eliminating unnecessary computation via signal bypassing. In an array multiplier, futile computations occur on those columns or rows of adder corresponding to zero bits in the input operands. Previous designs resort to input gating and output multiplexing to accomplish signal bypassing. The proposed designs, however, successfully resolve the adverse DC power consumption problem due to voltage loss in gated signals and implement the multiplexing mechanism cleverly via clock CMOS (C2MOS) circuitry. Two versions of the design are proposed with one emphasizing on maximizing power saving and the other focusing on reduced circuit complexity. The circuit overheads of both designs are confined to 23.4% and 12.8%, respectively. The proposed designs also achieve better and consistent power saving than previous work under a wide range of Vddand the power saving can be as high as 17%. [C1159]

"Energy-Optimized Fuzzy Control of Induction Motors Based on Nonintrusive Efficiency Estimation"

Electricity is the main type of energy consumed by industry. Awareness of opportunities for reducing electrical consumption has brought an emphasis on electrical energy saving for research such as in power electronics. This paper proposes an energy optimized control using fuzzy logic for induction motors based on noninstrusive efficiency estimation. The presented control is viewed as a direct energy saving technique since it takes into account both the input and output powers of the induction motor, through feedback of the efficiency estimate. [C1160]

"An Aggregation Tree Constructing Algorithm Based on Energy Consumption Assessment"

This paper first gives an analysis of data aggregation and data compression based on the energy consumption of sensor nodes, after which an approach is proposed to construct an aggregation tree in the case of non-perfect aggregation since GIT considers only the case of perfect aggregation and it does not work well if the aggregation is non-perfect. An assessment scheme that can get the information of hops from the aggregation point to the sink and the hops from the aggregation point to the source node is used to construct such an aggregation tree. Moreover, the energy consumption of the aggregation is also considered. This scheme can be used when perfect aggregation cannot be performed. In this paper, an approach to reduce the cost of reinforcement is also proposed, in which the reinforcement work is done by the source nodes themselves, not by the sink node. Simulation result shows that this approach can save more energy than GIT when the aggregation ratio is small. This result also provides a theoretical limit of aggregation to tell when GIT will lose its superiority and thus gives us a direction to choose among the aggregation algorithms. Another result shows that the further the sources are away from the sink, the less reinforcement messages are needed. [C1161]

"Improving Scalability and Complexity of Dynamic Scheduler through Wakeup-based Scheduling"

This paper presents a new scheduling technique to improve the speed, power, and scalability of a dynamic scheduler. In a high-performance superscalar processor, the instruction scheduler comes with poor scalability and high complexity due to the inefficient and costly instruction wakeup operation. From simulation-based analyses, we find that 98% of the wakeup activities are useless in the conventional wakeup logic. These useless activities consume a lot of power and slowdown the scheduling speed. To address this problem, the proposed technique schedules the instructions into the segmented issue window based on their wakeup addresses. During the wakeup process, the wakeup operation is only performed in the segment selected by the wakeup address of the result tag. The other segments are excluded from the wakeup operation to reduce the useless wakeup activities. The experimental results show that the proposed technique saves 50-61% of the power consumption, reduces 42-76% in the wakeup latency compared to the conventional design. [C1162]

"Using Serial Resistors to Reduce the Power Consumption of Resistive Touch Panels"

In this paper we analyze the characteristics of the resistive touch panel to find a simple way to reduce power consumption. A touch panel's current consumption is less than 1 muA while waiting, with the different of kinds of touch panels there is a 50 mA to 100 mA difference in the current consumption while operating. This difference has a great effect on the operation time of consumer electronic products. In this paper we propose a method according to Ohm's law of adding in serial resistors to reduce current consumption. As the serial resistors

inserted are higher, the current consumption becomes lower, and the analog sensed voltage becomes lower, too. However, a small sensed voltage may produce the wrong output signal based on the resolution of the A/D conversion, and then the touch panel may show an unstable phenomenon. Through experiments we have found which values for the serial resistor both save power consumption and still maintain the similar operation sensitivity of the resistive touch panel. [C1163]

"An Asymmetric Quorum-based Power Saving Protocol for Clustered Ad Hoc Networks"

Clustering in Mobile Ad Hoc Networks (MANETs) has shown to be a promising technique to ensure the scalability and efficiency of various communication protocols. Since stations in MANETs are usually equipped with batteries as the power source, it is critical to ensure the energy efficiency of clustering schemes. The Quorum-based Power Saving (QPS) protocols render extensive energy conservation as compared with IEEE 802.11 Power Saving (PS) mode and are widely studied over the past years. However, most existing QPS protocols adopt a symmetric design where stations in the network are guaranteed to discover each other. Observing that in clustered environments there is no need to insist in all-pair neighbor discovery, we propose an Asymmetric Cyclic Quorum (ACQ) system. The ACQ system guarantees the neighbor discovery between each member node and the clusterhead in a cluster, and between clusterheads in the network. A construction scheme is presented in this work, which assembles the ACQ system in O(1) time. We show that by taxing slightly more energy consumption on the clusterhead, the average energy consumption of stations in a cluster can reduce substantially than can be achieved by traditional QPS protocols. Simulation results show that the ACQ system outperforms the previous studies up to 52% in energy efficiency, while introducing no extra worst-case latency. [C1164]

"Potentials for reducing the power requirement of magnetic suspension systems by implementing a linear quadratic gaussian controller"

Magnetic bearings provide an energy-saving and resource-sparing possibility for supporting rotors running at high speed. This paper studies the potential of reducing the energy demand of magnetic levitation systems. Practical investigations show that this is obtainable by combining an optimal state estimator with an optimal state space controller. This configuration is known as Linear Quadratic Gaussian (LQG) regulator. In a sequential way, all the steps required for implementing this control strategy are depicted, starting with describing and modelling of the system which is a fully magnetically levitated blower in this case. Subsequently, the realization of the system state estimator is delineated. Both hints for carrying out the discretization of the continuous time model and a simple approach for choosing the variance matrices of the estimator are given. Special attention is paid to the design of the state feedback controller. The influence of the weighting matrix elements on the controller performance is investigated as well as an integrative extension of the regulator which ensures good reference response behaviour. Finally, measurements concerning the energy consumption of the levitation system are presented. The results show that both in static and dynamic case the implementation of the LQG regulator yields reduced control energy effort, compared to a system controlled by a conventional PID controller. It is noteworthy that, simultaneously to the enhancement of energy efficiency, implementing the LQG controller improves the dynamic properties of the levitation system, e.g. transient time and overshoot. [C1165]

"A 8-bit 500-KS/s low power SAR ADC for bio-medical applications"

This paper presents a successive approximation register analog-to-digital converter (SAR ADC) design for bio-medical applications. An energy-saving switching sequence technique is proposed to achieve low power consumption. The average switching energy of the capacitor array can be reduced by 56% compared to a conventional switching method. The measured signal-to-noise-and-distortion ratios of the ADC is 46.92 dB at 500 KS/s sampling rate with an ultra-low power consumption of only 7.75-muW from a 1-V supply voltage. The ADC is fabricated in a 0.18-mum CMOS technology. [C1166]

"An Experimental Study of Passive UHF RFID System with Longer Communication Range"

Radio-frequency identification (RFID) systems are useful for reducing costs in supply chains. The communication range between the reader and the tag is one of the most important points in the application of RFID to supply chain management. We present results of experiments conducted on our passive RFID prototype system that we designed with the aim of increasing the communication range. It uses an intermittent transmission method to reduce the power consumption of the tag IC. Our results show that the power consumption was reduced to about three-quarters by using intermittent transmission with a duty ratio of 40%. Our experimental results indicate that optimization of the transmitting signal is effective for saving power consumption at tag IC and increasing the communication range. [C1167]

"Leakage power reduction through dual Vth assignment considering threshold voltage variation"

In today's sub-100nm CMOS technologies, leakage current has become an important part of the total power consumption, affecting both yields and lifetime of digital circuits. Dual Vth assignment, which is proven to be an effective method of reducing leakage power in the past, is also effective in today's technologies with certain modifications. In the paper, based on a statistical timing analysis (SSTA) framework we presented a dual Vthassignment method which can effectively reduce the leakage power even in the presence of large Vth variation. Besides, we use a statistical DAG pruning method which takes correlation between gates into account to speed up the dual Vthassignment algorithm. Experimental results show that statistical dual Vthassignment can reduce on average 40% more leakage current compared with conventional static method without affecting the performance constraints. Our DAG pruning method can reduce on average 30% gates in the circuit and save up to 50% of the total run time. [C1168]

"Register binding guided by the size of variables"

An important problem is how to carry out register binding such that any register has to be bound to a set of variables such that the difference between their sizes is as small as possible. For the case of hardware implementations, satisfying this latter constraint will allow to reduce the complexity of the clock generation tree, and saving area occupied by the registers which is very important for the case of system-on-chip and some embedded systems. When registers are already built, satisfying this latter constraint would allow reducing power consumption due to useless switching activities that will happen into any register that is bound to variables with different sizes. Assuming that the size in bits of any variable is known, we propose in this paper exact algorithms to optimally solve this problem for the case of acyclic graphs. An extended version of this problem is how to solve it while controlling the number of variables to be assigned to a same register. We also propose exact algorithms to optimally solve this latter version of the problem. Experimental results are provided. We also test the impact of the proposed approach in the case of a hardware implementation using the design analyzer tool from Synopsys Inc.. Obtained results have shown that both area and power consumption have been reduced. [C1169]

"Integrating Energy-saving Concept into General Product Design"

Currently, Energy and Environmental issues are worldwide concerns. Energy savings is also without doubt the most effective strategy for environmental protection. This paper introduces a new general product design method. Our research effort will be directed towards the following three primary objectives: (1) investigating all the aspects related to energy-saving issues throughout the entire product life cycle; (2) developing a mathematical model (called Energy Factor) to calculate the products' energy consumption throughout the entire life cycle; (3) establishing the theoretical frame of the new innovative product design method. In this innovative method, the energy-saving concept will be applied at the first step of product life cycle, i.e. product design. And we believe that it will bring the product design to a new stage, which can design the energy-saving products and manufacturing systems. In order to reduce the energy consumption throughout the entire product life cycle (from cradle to grave), this design method is based on axiomatic design theory, and integrates design unit and energy factor concepts. In this paper, the theory frame will be described in detail, and the new concept called energy factor will be introduced briefly. [C1170]

"Optimal Locations for Join Processing in Sensor Networks"

Battery lifetime tends to become the limiting factor for query processing in sensor networks; this calls for energy-saving implementations of query-algebra operators. As the join operator is important for data acquisition in sensor networks, e.g., to explore correlations in the data, recent research has brought up a number of in-network strategies for join processing. But it is still unclear in which cases such strategies can be applied. In some scenarios it might even be optimal to process a join query using a centralized implementation. This paper presents our work in progress on analyzing how join queries can be optimally handled in sensor networks. In particular, we provide theoretical bounds on the energy-savings that can be achieved by distinct in- network strategies as opposed to a simple centralized join. An important aspect is that devising an optimal join strategy requires knowledge, e.g. of the join selectivity. Gathering this knowledge reduces the potential energy savings. Our major contribution is to show in which cases different in-network approaches are theoretically applicable and when the superior strategy is to perform the join at the base station. This is a first step towards devising practical join strategies. [C1171]

"Performance and power evaluation of SH-X3 multicore system"

We have developed an embedded processor that supports asymmetric multiple processor (AQMP), symmetric

multiple processor (SMP), and an AMP/SMP hybrid system. It contains four SH-X3 cores used to support cache coherency from that obtained using an SH-X2 core. In this paper, we evaluate the following three techniques to improve the processing performance and reduce the power consumption in parallel processing in the processor. The first technique is snoop controller (SiNC) to improve cache coherency performance. The performance overhead by snoop is decreased up to 0.1% when SPLASH-2 is executed. The second technique is detection and resolution of synonym problems so that we may not use the page coloring for page table management. The processes handling time in Linux is reduced by 29.4% compared with the case solved the problem with software. The third technique is the individual core clock frequency and the light sleep mode which is used to maintain the cache coherency even when the cores are stopped, to reduce the power consumption. The energy is decreased by 5.2% and 4.5%, respectively. As a result, the SH-X3 core achieved a performance that has scalability proportional to 0.72-0.93 times the number of cores and a power saving of 4.5-44.0% without increasing the execution time. [C1172]

"Numerical analyses of minimum energy operation of multiple trains under DC power feeding circuit"

An algorithm optimizing total energy consumption of multiple inverter train operation considering DC feeding circuit is investigated in this paper. The proposed mathematical formulation can deal with several characteristics of trains, especially the effect of regenerative braking system. The developed optimization algorithm based on the gradient method is applicable to solve the formulated problems. The algorithm is ready to apply practical large-scale problems. The formulation and algorithm enables us to discuss energy-saving operation quantitatively. Several numerical analyses are demonstrated to verify the reliability and validity of the proposed method and clarify the energy-saving operation for two trains. The results shows that train speed profiles and control inputs strongly depend on the phase of departure times. The proposed algorithm can reduce energy consumption by 4.2~17.9% from that based on the conventional operation rule. These results indicates that the numerical analyses are significant to realize energy-saving operation. Furthermore, it is also demonstrated that the method can be applied to the optimal voltage control of a substation. [C1173]

"Utilization of the standard-voltage-range in low-voltage networks for the usage of Local-Energy-Controllers without affecting the power-quality"

Low-voltage-networks operate with a nominal voltage charged with a tolerance range. Consumer's installations (CI) are feeded with different supply-voltages which depend on the location of the CI within the LV-grid and the load flow. At the feeding point of the CI no additional regulating device is foreseen. Local-energy-controllers can decrease the supply-voltage and influence the energy consumption of the CI. This paper shows when LECs operate properly and which preconditions have to be fulfilled for the energy-saving. Different consumer categories and the calculation algorithm for the amount of the energy saving will be introduced. At the end the algorithm will be compared with results of real LEC-installations. The properly engineered operation of an LEC saves energy, energy costs and reduce CO2, without affecting the power-quality negatively. [C1174]

"Limits on voltage scaling for caches utilizing fault tolerant techniques"

This paper proposes a new low power cache architecture that utilizes fault tolerance to allow aggressively reduced voltage levels. The fault tolerant overhead circuits consume little energy, but enable the system to operate correctly and boost the system performance to close to defect free operation. Overall, power savings of over 40% are reported on standard benchmarks. [C1175]

"An Energy-Efficient TDMA MAC for Wireless Sensor Networks"

This paper proposes an energy-efficient and collision-free medium access control protocol TDMA-WSN for wireless sensor networks. The protocol is based on time division multiple access (TDMA) principle and reduces energy consumption by avoiding overhearing, collision and idle listening. Nodes in TDMA-WSN build schedules based on information about their neighborhood to determine when they can transmit to their neighbors and when they should listen to the channel or sleep. TDMA-WSN proposes a novel resolution with three-d-hop neighborhood information to avoid collision caused by the two-hop collision-free principle used in some protocols. TDMA-WSN can accelerate passing message by arranging schedule based on routing information from the upper-layer. The simulation results indicate that TDMA-WSN outperforms contention-based protocols (e.g., S-MAC) and scheduling-based protocols (e.g., NAMA) with significant energy savings. [C1176]

"Energy Efficient Multi-rate Based Time Slot Pre-schedule Scheme in WSNs for Ubiquitous Environment"

Nowadays, smart spaces occupy an essential part of ubiquitous computing environment. The spaces integrated with wireless sensors networks, actuators and context-aware services become part of our daily life. Smart spaces are equipped with a large number of wireless sensors that aim to collect large quantities of context information, during the process, there exists a large amount of collisions and energy consumption. Therefore, this paper provides a novel multi-rate based local framing pre-schedule scheme to further reduce collisions and improve energy efficiency in CSMA/TDMA hybrid MAC layer of wireless sensor network. This MAC combines CSMA and TDMA functionalities together while obviates their shortcomings. Having been assigned, slot 0 is preserved as the pre-schedule slot, to inform neighbor nodes the schedule of the senders. During the pre-schedule slot, each node knows exactly the schedule of other neighbor nodes. Multi-rate and power scaling are applied to achieve further energy saving by adpoting an acceptable rate rather than maximum rate. Data rate is dynamically adjusted according to the traffic load of sending nodes, in an energy efficient data rate, to save energy. Being compared with Z-MAC in terms of performances, local framing pre-schedule and multi-rate in this experiment achieved further energy efficiency. [C1177]

"Fractional Cooperation using Coded Demodulate-and-Forward"

Since the introduction of cooperative diversity, many different implementations have been proposed to increase the reliability and/or power efficiency of distributed networks via relaying. One simple and flexible scheme introduced is coded demodulate-and-forward, where the relay only demodulates, instead of decodes, the received data, to create and forward a new codeword to the destination. This reduces the complexity of hardware as well as the energy consumption by the relay. In this paper, we consider another flexible feature of the coded demodulate-and-forward scheme, where the relay uses only a fraction of its codeword to assist the source, and saves the rest of the codeword for transmitting its own information. Previous schemes have generally focused on all-or-nothing cooperation where a relay either contributes all its resources or none at all to the source. Depending on the channel conditions, improved diversity order of the source codeword can be achieved with some small loss in the relay's own transmission performance. Here we identify the necessary criterion for the source to achieve a diversity order of 2. [C1178]

"Energy-efficient cooperative routing protocol for wireless sensor networks"

User cooperation based on spacial diversity can significantly improve the energy-efficiency of system. In this paper, a novel cooperative routing protocol is proposed in wireless sensor networks. A minimum energy multi-nodes cooperative path is constructed by the cooperative transmission of neighboring nodes and comparison of total power consumption. The distributive routing scheme can be implemented by carrying information about power consumption of route and cooperative cluster in Routing Request packet. Simulation results show that the energy-saving performance can be greatly improved compared with traditional non-cooperative routing. Meanwhile, the difficulty of control and complexity of computation can be reduced by using the select strategy of cooperative nodes, trading off a little decline in energy-efficiency. [C1179]

"A low clock swing, power saving and generic technology based D flip-flop with single power supply"

A low power, low clock swing D flip-flop (DFF) based on C2MOS (Clocked CMOS) and sense amplifier (SA) is proposed in this paper. This DFF is extensively applicable as it utilizes generic CMOS technology and needs no additional power supply specially for the clock sub-circuit. Simulation result shows that the average leakage power and dynamic power of this DFF are reduced by 78.73% and 8.74% respectively, with the delay slightly smaller, with the clock swing as low as 658 mV (under 1.8 V supply). [C1180]

"Low-Power built-in logic block observer realization for BIST applications"

This paper presents a low-power built-in logic block observer (LP-BILBO) to realize the performance in minimum power consumption. The proposed LP-BILBO is based on a low-power test module (LPTM) design to divide the system clock into two independent clocks for reducing the switching activity in power savings. Simulation results show that the proposed LP-BILBO can effectively save its own power consumption up to 48% (on average) during the low-power operation modes. Also, the performance analysis in benchmark ISCAS'89 circuits indicates that on average 44% power reduction can be obtained when the proposed LP-BILBO is adopted in the testing scheme. [C1181]

"Improved digital calibration technology in a 12-b, 40-MS/s pipelined ADC"

In the design of 12-bits 40MSample/s pipelined ADC, the traditional close-loop high performance residue amplifier in first stage is replaced by an open-loop amplifier to reduce power dissipation and increase circuit speed. The errors brought by open-loop amplifier are evaluated and calibrated by an improved statistics-based

background calibration technology. A self-adaptive search algorithm and a magnitude incremental comparison algorithm are presented in statistics-based background calibration technology to improve residue difference estimator circuit and LUT (look up table) of binary monotonically function respectively. The improved calibration technology can reduce digital circuit power dissipation and size significantly. Simulation results show that power consumption of digital circuit is reduced by 93% and room of ROM is saved by 84%. The ADC is implemented in SMIC 0.18 CMOS process, consumes 210 mW, and has a layout size of 3.2*3.7 mm2. [C1182]

"Low-power implementations of DSP through operand isolation and clock gating"

The advent of implantable devices such as digital cochlea has made low power circuit design an increasingly important research area. In this paper, we utilize the operand isolation to save power dissipation in data-path by reducing unnecessary switching activity and clock gating to reduce redundant power dissipation in registers of our DSP which is used for implantable digital cochlea. Experimental result from running application program on our design shows 27.64% reduction in dynamic switching power with no increase in critical path delay and only 2.10% area overhead. [C1183]

"A Media Access Protocol for Proactive Information Discovery in Ubiquitous Networks"

This paper proposes a MAC protocol for information discovery in ubiquitous networks. The proposed protocol is based on proactive discovery in which wireless devices periodically send advertisement broadcasts. The objective of the protocol is to provide the specified discovery time of the single-hop neighbors in a mobile ad hoc network. Since collisions in wireless network degrade performance on the discovery time, a node selects an adequate broadcast rate considering the network topology. In this paper, we show that using information about the number of neighbors in combination with framed Aloha scheme can provide the specified discovery time. We also consider a simple basic power saving mechanism which allows significantly reduce the power consumption [C1184]

"An Evaluation Study of a Fair Energy-Efficient Technique for Mobile Ad Hoc Networks"

In this study, we present a performance evaluation of an energy conservation technique designed for mobile ad hoc networks. This technique was designed with energy fairness central to its operation. This algorithm is not a routing algorithm. It works with existing routing protocols to complement their functionality from an energy-efficiency perspective. We show that this technique scales well with increased network traffic and population. We also compare it to the on-demand power management algorithm, a technique specifically designed to reduce idle energy consumption. Our comparison shows that our technique performs better in terms of energy savings and fairness as well as network lifetime extension [C1185]

"PBRCE: Energy Efficient MAC Protocol for Wireless Ad Hoc Networks"

The currently most popular medium access control (MAC) protocol, namely IEEE 802.11 distributed coordination function (DCF), is not energy efficient. In this paper we present the principles of achieving energy-efficiency in MAC protocol design for WLANs. Along these principles, we propose a novel dual-channel MAC protocol, called power-control binary-countdown-carrier-sense/request-to-send (RTS)/clear-to-send (CTS)/ensure-to-send (ETS) (PBRCE). PBRCE aims not only at energy-efficiency, but also at higher network throughput. The enhanced network performance is achieved by easing the "exposed terminal" and "hidden terminal" problems. The energy efficiency is achieved by reducing the collision rate-thus saving energy through avoiding retransmission of the same packets-and by controlling the signal transmission power and going to sleep mode to avoid the unnecessary passive listening [C1186]

"Adapting Predictions and Workloads for Power Management"

Power conservation in systems is critical for mobile, sensor network, and other power-constrained environments. While disk spin-down policies can contribute greatly to reducing the power consumption of the storage subsystem, the reshaping of the access workload can actively increase such energy savings. Traditionally reshaping of the access workload is a result of caches passively modifying the workload with the aim of increasing hit ratios and reducing access latency. In contrast, we present the a shifting predictive policy that actively reshapes the workload with the primary goal of conserving disk energy consumption. By reshaping the disk workload to explicitly lengthen idle periods, the disk can remain spun-down longer, saving more energy. We show that our approach can save up to 75% of disk energy compared to the common fixed-timeout spin-down policies. Our shifting algorithm dynamically shifts to the most energy efficient cache prefetching policy based on the current workload. This best shifting prefetching policy is shown to use 15% to 35% less energy than traditional disk spin-down strategies and 5% to 10% less energy than the use of a fixed (non-shifting) prefetching policy. [C1187]

"Joint rate and power adaptation for wireless local area networks in Nakagami fading channels"

In this paper, we propose a fast channel-driven rate and power adaptation (CDRPA) algorithm for wireless local area networks (WLAN). The proposed algorithm jointly adjusts the rate and power for data frame transmission in a generalized Nakagami fading channel. Different from the previous works, the CDRPA algorithm bases on the channel quality observed from the previous ACK frames and makes the selection only from the limited combinations of rate and power, instead of exhausted searching. Thus, the CDRPA algorithm greatly reduces the complexity compared to the previous approaches. Furthermore, to meat the different performance requirements, we propose several alternatives based on the CDRPA algorithm. Prom the viewpoint of energy saving, the CDRPA algorithm determines the transmit power first to maximize energy efficiency; while achieving the maximum goodput performance, the CDRPA first selects the appropriate transmit rate to ensure the successful transmissions. The numerical results show that the CDRPA algorithm can approach to the optimum performance in terms of energy efficiency and goodput while keeping the low complexity [C1188]

"Quick data-retrieving for U-APSD in IEEE802.11e WLAN networks"

The IEEE 802.11e defines a MAC protocol, which provides EDCA (enhanced distributed channel access) and HCCA (HCF controlled channel access) to support differentiation service over WLAN (wireless LAN). In IEE E802.11e WLAN, real-time application such as VoIP (voice over IP) can have more chance to access the WM (wireless medium) than non real-time application. In addition to QoS support in WLAN, power consumption is a critical issue when WLAN is used in handheld devices. For power saving in the use of real-time applications like VoIP under EDCA, U-APSD (unscheduled automatic power save delivery) was proposed in Y. Chen et al. (2004). In fact, it can save power consumption and works well when it is used for bi-directional voice connections generated at constant bit rate. However, when it is used for real-time applications like ON-OFF traffic, buffering delay at AP (access point) increases. To reduce the buffering delay, this paper proposes two mechanisms. Simulation results show that they can alleviate buffering delay generated at AP [C1189]

"Low-power mechanism with power block management"

In this paper, a low power mechanism with power block management is proposed to reduce the power consumption in DSP chips. Because the digital signal processing (DSP) chips use many functional units in the data-path to achieve parallel processing, the unnecessary functional units are also executed simultaneously, and they dissipate the power. In the paper, we classify the types of instruction sets based on their data flow in the DSP to generate the control signals which active the necessary units in their data-path. The mechanism is called power block management (PBM). We employ particular guarded circuits in the different situations to avoid the actions of unnecessary functional units so as to reduce the power dissipation. The experimental results show that the power consumption can be saved about 14% at the cost of less than 2.7% area increment [C1190]

"A 10b 50MS/s pipelined ADC with opamp current reuse"

Power-saving techniques such as opamp current reuse and capacitive level shift reduce the power consumption of a 10b pipelined ADC to 220muW/MHz. A 50MS/S prototype in 0.18mum CMOS consumes 18mW (11mW for analog) at 1.8V and occupies 1.1times1.3mm2. The measured ENOB of the ADC is 9.2b (8.8b) for a 1MHz (20MHz) input [C1191]

"Optimized Data Fusion in Bandwidth and Energy Constrained Sensor Networks"

This paper considers the problem of decentralized data fusion (DDF) for large wireless sensor networks with stringent bandwidth requirements. To reduce the power and bandwidth costs of wireless transmissions, each sensor node is confined to quantize its sensing data and send 1-bit information only. Under this setting, we derive the maximum likelihood (ML) data fusion rule for decentralized parameter estimation, and analyze its Cramer-Rao lower bound (CRLB) of the fusion performance in the sense of mean square distortion. Depending on the underlying noise characteristics, our 1-bit DDF scheme can achieve estimation performance competitive to or even surprisingly better than that of centralized fusion over unquantized data. There is considerable saving in communication costs, which in turn reduces network energy consumption. Furthermore, we investigate network optimization, for which a worst-case robust design methodology is adopted to formulate a well-behaved min/max optimization problem. From the information processing viewpoint, the resulting optimized network offers robust fusion performance at minimal costs of communication resources [C1192]

"Localization of Diffusive Sources Using Distributed Sequential Bayesian Methods in Wireless Sensor Networks"

We develop an efficient distributed sequential Bayesian estimation method to localize a diffusive source in wireless sensor networks. Potential applications include security, environmental monitoring, pollution control, and explosives detection. We first derive the physical model of the substance dispersion by solving the diffusion equations under different environmental scenarios. We then integrate the derived dispersion models into the distributed processing technologies, and propose a distributed sequential Bayesian localization technique, in which the state belief is transmitted in the wireless sensor networks and updated using the measurements from the new sensor node. In order to decrease the required communication burden we propose two parameterizable belief approximations: a Gaussian approximation and a new linear combination of polynomial Gaussian approximation. We also apply the idea of information-driven sensor scheduling and select the next sensor node according to certain criterions to reduce the response time and save energy consumption of the sensor network [C1193]

"Autonomic Power and Performance Management for Computing Systems"

With the increased complexity of platforms, the growing demand of applications and data centers' servers sprawl, power consumption is reaching unsustainable limits. The need to improved power management is becoming essential for many reasons including reduced power consumption & cooling, improved density, reliability & compliance with environmental standards. This paper presents a theoretical framework and methodology for autonomic power and performance management in e-business data centers. We optimize for power and performance (performance/watt) at each level of the hierarchy while maintaining scalability. We adopt mathematically-rigorous optimization approach minimizing power while meeting performance constraints. Our experimental results show around 72% savings in power as compared to static power management techniques and 69.8% additional savings with both global and local optimizations. [C1194]

"Energy Reduction by Workload Adaptation in a Multi-Process Environment"

Reducing energy consumption is an important issue in modern computers. Dynamic power management (DPM) has been extensively studied in recent years. One approach for DPM is to adjust workloads, such as clustering or eliminating requests, as a way to trade-off energy consumption and quality of services. Previous studies focus on single processes. However, when multiple concurrently running processes are considered, workload adjustment must be determined based on the interleaving of the processes' requests. When multiple processes share the same hardware component, adjusting one process may not save energy. This paper presents an approach to assign energy responsibility to individual processes based on how they affect power management. The assignment is used to estimate potential energy reduction by adjusting the processes. We use the estimation to guide runtime adaptation of workload behavior. Experiments demonstrate that our approach can save more energy and improve energy efficiency [C1195]

"Buffer Space Optimisation with Communication Synthesis and Traffic Shaping for NoCs"

This paper addresses communication optimisation for applications implemented on networks-on-chip. The mapping of data packets to network links and the timing of the release of the packets are critical for avoiding destination contention. This reduces the demand for communication buffers with obvious advantages in chip area and energy savings. We propose a buffer need analysis approach and a strategy for communication synthesis and packet release timing with minimum communication buffer demand that guarantees worst-case response times [C1196]

"Energy-Efficient FPGA Interconnect Design"

Despite recent advances in FPGA devices and embedded cores, their deployment in commercial products remains rather limited due to practical constraints on, for example, cost, size, performance, and/or energy consumption. In this paper, we address the latter bottleneck and propose a novel FPGA interconnect architecture that reduces energy consumption without sacrificing performance and size. It is demonstrated that the delay of a full-swing, fully-buffered interconnect architecture can be matched by a low-swing solution that dissipates significantly less power and contains a mix of buffer and pass-gate switches. The actual energy savings depend on the specifics of the interconnect design and applications involved. For the considered fine-grain FPGA example, energy savings are observed to range from a factor 4.7 for low-load critical nets to a factor 2.8 for high-load critical nets. The results are obtained from circuit simulations in a 0.13mum CMOS technology for various benchmarks [C1197]

"Power efficient stochastic-wireless sensor networks"

Energy utilization is a challenging problem in wireless sensor networks due to the limited battery capacity in sensor nodes. This paper presents a fundamentally different design of an energy-efficient WSN, named

stochastic-WSN (S-WSN). Two main energy-saving techniques are proposed: (i) optimal traffic flow and (ii) efficient scheduling and routing protocol to implement the optimal traffic flow. By using the optimal traffic flow, each sensor can decide its own activity in the routing procedure, thus, S-WSN realizes near-zero network administrative overhead. The optimal traffic flow provides a constructive approach for defining a scheduling algorithm, which keeps only a small subset of nodes awake in the network to provide connectivity while placing the majority of nodes in sleep mode. It reduces power consumption as well as operation interference. The network lifetime obtained using S-WSN provides a significant improvement as compared to using the energy balanced data propagation (EBDP) approach [C1198]

"Dynamic Resource Aware Software Configuration for Pervasive Application"

Due to the increasing proliferation and serious resource constraints of mobile devices, using the rich-resource server can help the mobile client to perform some tasks for improving performance and saving resources is more and more needed in pervasive computing. Remote execution is a static software configuration approach that is unsuitable for constantly changing environments. In this paper, we present a dynamic software partitioning algorithm that can allocate optimally the appropriate components among the machines to minimize the specified resource consumptions. Since dynamic software partitioning often leads to components' migration, we consider component migration cost, plus computation cost and communication cost, to set up a generic math model of resource consumption. Based on the network flow theory, we reduce the optimal software partitioning problem to the min-cut problem of a cost graph. Our algorithm can be used to find an optimal software partition to conserve network bandwidth, decrease response time of services and save energy of mobile devices, respectively. The simulation results show the algorithm is very effective, and can save significantly more resource than the previous studies [C1199]

"Adaptive Distributed Compression Algorithm for Wireless Sensor Networks"

In this paper we proposed a novel adaptive distributed wavelet compression (ADWC) algorithm for reducing energy consumption in a wireless sensor network, where each of the sensors has limited power. This algorithm is characterized by a distributed lifting factorization, which matches well with the transmission strategy employed in wireless sensor networks. It also presents an adaptive algorithm to select the optimal wavelet compression parameters to minimize total energy dissipation. The simulation results showed that these approaches can achieve significant energy savings without sacrificing the quality of the data reconstruction [C1200]

"EDF Plans for Implementation of Consumer Portal Functions"

EDF has widely implemented demand response in France. Six million meters provide residential customers with the ability to subscribe to an off-peak hours tariff. For commercial and industrial customers, different tariffs exist to provide substantial economies when the customer is able to control consumption. Today, EDF is looking at providing more flexible services, adapted to the complexity of the deregulated market. A proposal of the European parliament to increase energy efficiency at the end-use side (achieve an additional 1 % of savings each year) could also open a huge potential market. EDF is conducting several R&D projects on residential and commercial metering. A major aspect of the work is the integration to the information systems of the company. EDF is evolving its meters towards open standardized interface to answer regulatory mandates as well as to enable competitive procurement and reduce life-cycle costs [C1201]

"An Energy-efficient Contention-based MAC Protocol for Wireless Ad Hoc Networks"

In this paper, an energy-efficient contention-based MAC protocol (ECM) for wireless ad hoc networks is proposed. The ECM is the combined protocol of the power management scheme and the collision avoidance scheme of the IEEE 802.11 DCF to reduce the energy consumption of a node. The proposed ECM enhances power saving effects of the legacy IEEE 802.11 DCF, provides longer network lifetime, and delivers more packets than the power management scheme of the legacy IEEE 802.11 DCF. These results are shown throughout the simulation [C1202]

"Power Saving with p-Persistent Sleep Decision for Ubiquitous Mobile Communications"

Battery power is an important and limited resource in ubiquitous mobile communications. Energy consumption can be reduced by turning off the radio during idle times. In most power saving schemes, a node decides whether to put its wireless interfaces in the sleep state or in an awake state, based only on the presence of packets destined for the node. However, by considering other factors related to the node status such as the remaining energy, the node can achieve more power savings for the given delay constraints. In this paper, we propose a p-persistent power saving scheme for mobile devices (nodes) in ubiquitous mobile communications systems. The proposed scheme first computes the sleep probability, considering the node status-related factors,

including the channel state between nodes, the number of packets queued, the constraint on packet delay, the intensity of load, and the remaining available battery energy. Then, using the probability, the proposed scheme decides the node state. By using simulation, we compare the proposed scheme with IEEE 802.11 power saving mode. The results show that the proposed scheme saves remarkably more energy for the given delay constraints [C1203]

"Low-power multiplier with static decision for input manipulation"

In this paper, a method to reduce the power consumption of low-power multipliers is proposed. A decision logic module decides about complementing the input before sending it to the multiplier core. The decision is based on minimizing the switching activity and hence the power consumption. The decision logic proposed in this work, unlike the conventional dynamic decision logic modules, uses a small look up table to make its decisions statically once for all the possible combinations on new input and old input. This feature has lead to the reduction of the power, delay, and complexity of the logic compared to its predecessors while the power saving is negligibly reduced [C1204]

"Generalized Indexing for Energy-Efficient Access to Partially Ordered Broadcast Data inWireless Networks"

Energy conservation and access efficiency are two fundamental though competing goals in broadcast wireless networks. To tackle the energy penalty from sequential searching, the interleaving of index with data items has been proposed. Although, quite important contributions exist on providing broadcast indexes, they have one or more of the following problems. Firstly, all of them assume total ordering among broadcast data, and none considers the more general case of partial ordering. Secondly, they are balanced structure, which does not fit the "linear (one-dimensional) structure" of the wireless medium, in which imbalanced structures may offer significant advantages. Thirdly, they do not take into account the skewness in the access pattern, which prohibits larger performance gains to be reaped. Finally, they require all index items to be of equal size, which may not always give the optimal performance. To cope with all these problems, we introduce a new imbalanced tree-structured index. The new index is shown to be a generalization of two previously proposed high-performance indexes, and it introduces for the first time the problem of indexing partially ordered broadcast data. We present an experimental analysis of the proposed method, contrasting it with competing techniques. The analysis exhibits the efficiency of the proposed index in reducing the energy consumption without noticeably worsening the access latency [C1205]

"A Floorplan-Aware Dynamic Inductive Noise Controller for Reliable Processor Design"

Power delivery is a growing reliability concern in microprocessors as the industry moves toward feature-rich, power-hungrier designs. To battle the ever-aggravating power consumption, modern microprocessor designers or researchers propose and apply aggressive power-saving techniques in the form of clock-gating and/or power-gating in order to operate the processor within a given power envelope. These techniques, however, often lead to high-frequency current variations, which can stress the power delivery system and jeopardize reliability due to inductive noise (L(di/dt)) in the power supply network. To counteract these issues, modern microprocessors are designed to operate under the worst-case current assumption by deploying adequate decoupling capacitance. With the trend of lower supply voltage and increased leakage power and current consumption, designing a processor for the worst case is becoming less appealing. In this paper, we propose a new dynamic inductive-noise controlling mechanism at the microarchitectural level that limit the on-die current demand within predefined bounds, regardless of the native power and current characteristics of running applications. By dynamically monitoring the access patterns of microarchitectural modules, our mechanism can effectively limit simultaneous switching activity of close-by modules, thereby leveling voltage ringing at local power-pins. Compared to prior art, our di/dt controller is the first that takes the processor's floorplan as well as its power-pin distribution into account to provide a finer-grained control with minimal performance degradation. Based on the evaluation results using 2D floorplans, we show that our techniques can significantly improve inductive noise induced by current demand variation and reduce the average current variability by up to 7 times with an average performance overhead of 4.0% [C1206]

"UWB Communications with Under-Sampled Receivers"

In this paper, we investigate a novel coding idea proposed previously to enable under-sampled receivers. An under-sampled receiver can sample the received baseband signals at only a fraction of the Nyquist rate and turns out to be an effective solution to the bottleneck of high-rate sampling and processing in ultra-wideband (UWB) communications. The spectrum aliasing problem can be solved by an analogy between an under-sampled system and a multiple-antenna one. However, underlying differences between the two systems exist

and motivate the study of the fundamental limits of a coded under-sampled system. The study is carried out by characterizing the optimal coding structures with and without channel state information at transmitter (CSIT). A practical selective coding structure is also developed to provide satisfactory performance with reduced CSIT requirement. Finally, simulations are conducted to verify the theoretical characterization. Our results indicate that an under-sampled UWB system can benefit from power-saving, cost reduction, and full multipath diversity at the expanse of little or confined performance degradation [C1207]

"Applying the zeros switch-off technique to reduce static energy in data caches"

Zeros switch-off is a leakage energy reduction technique applicable to cache memories. It works at the cache word level by removing the power supply of all or part of its most significant bytes when they store a zero, taking advantage of the high percentage of zero data bits in common programs. Experimental results, obtained by using the SPEC2000 benchmarks suite, show that the average leakage energy savings reach 60.3% with no IPC loss indeed. The proposed technique can be combined with other existing energy reduction techniques, reaching, on average, 67.3% savings with 0.5% IPC losses [C1208]

"Strategic Versus Collaborative Power Control in Relay Fading Channels"

Relaying is often advocated for improving system performance by enhancing spatial diversity in wireless networks. Relay nodes make contributions to improving the source-destination link quality by sacrificing their own energy. In this paper, we address the issue of energy tradeoff made by relay nodes between transmitting their own data and forwarding other nodes' information in fading channels. Assuming channel state information (CSI) on fading amplitudes is perfectly known to both transmitters and receivers, we propose two power control and relaying policies. One is based on a strategic motivation, where each node functions as a relay and minimizes its own energy expenditure while meeting the outage probability requirement of all nodes. The second approach is based on complete collaboration, where the total energy consumption across all nodes is minimized. Numerical results demonstrate a significant impact of CSI on energy saving in relaying as compared with the relaying scheme without power control. In most cases, collaborative relaying dominates over the non-cooperative strategic one in the sense that the former not only minimizes total energy but also reduces individual energy expenditure of all nodes. This implies once forwarding and relaying is adopted across various nodes, exchanging of CSI becomes crucial, and collaborative energy minimization rather than the non-cooperative strategic approach should be pursued [C1209]

"Dynamic Standby Prediction for Leakage Tolerant Microprocessor Functional Units"

Leakage power is projected to comprise approximately 50% of the processor's power for sub 65 nm technologies. Much of this power is consumed in the processor's functional units. Accordingly, leakage control techniques are employed to reduce leakage in these functional units. Many of these techniques are dynamic and are based on an input sleep signal to initiate a low leakage mode. However, since most of these leakage control techniques are based on circuit level schemes, such techniques inherently lack information about the operational profile of the functional units they manage. This limitation is usually handled statically by using a fixed length counter that generates the sleep signal when the functional unit is idle for a specified number of cycles. In this paper, the limitations of the static sleep signal generation approach are identified, and the use of a dynamic alternative that is capable of adopting the counter length to the running application is proposed. In order to assess the accuracy of the proposed dynamic sleep signal generator, the length of the sleep period following the sleep signal generation is used as a metric to identify the usefulness of utilizing the dynamic approach. Experimental results for the dynamic alternative shows up to 98% accuracy in predicting the length of the standby period compared to an average of 40-60% in the static case, which translates into increased leakage savings. This is achieved while consuming 360 muW of overhead power at 1 GHz [C1210]

"Comparison of Clustering Algorithms and Protocols for Wireless Sensor Networks"

One of the mechanisms used to enlarge the lifetime of wireless sensor networks (WSN) and to provide more efficient functioning procedures is clustering. By assuming roles within a cluster hierarchy, the nodes in a WSN can control the activities they performed and therefore, reduce their energy consumption. However, the election of when to act as a data provider (saving energy) and when to act as a gateway (cluster head) between the nodes and the base station is not a simple task. To make this decision it is necessary to take into account aspects like power level signal, transmission schedules and networking functioning (proactive or reactive). In this paper we study some basic concepts related to the clustering process in WSN and presenting a comparison survey between different clustering protocols [C1211]

"System-Wide Dynamic Power Management for Portable Multimedia Devices"

Energy reduction is critical to increase the mobility and battery life for today's pervasive portable computing systems. At the same time, energy reduction must be subject to the real-time constraints and quality of service (QoS) requirements for multimedia applications running on many of these systems. This paper presents a novel run-time scheduling approach to reduce the system-wide energy consumption for such systems. In this paper, the multimedia applications are modeled using a popular weakly hard realtime model, i.e., the (m,k)-model. Our experimental results show that, by judiciously scheduling the real-time tasks and shutting down the processor and/or peripheral devices, our approach can lead to significant energy savings while guaranteeing the (m,k) firm deadlines at the same time [C1212]

"Fair Scheduling for Hybrid Mesh Network Interconnecting Video Sensors"

In this paper, we consider deployment of a wireless mesh network (WMN) to interconnect a video sensor network (VSN) and improve its energy efficiency. We propose a scheduling method for mesh nodes that performs fair scheduling if there is sufficient link capacity, and perform traffic grooming followed by scheduling using a novel constraint relaxation method if link capacity is insufficient. The resulting improvement in energy efficiency of the VSN is evaluated. Results show remarkable savings in power consumption of sensor nodes when a VSN is interconnected with a WMN: energy consumption in the VSN is reduced by approximately 55-79% when the probability that a sensor node can forward traffic to a mesh node is 50% [C1213]

"Development of an Experimental Model of BACnet-based Lighting Control System"

Lighting control system provides various benefits in building management such as operational convenience, energy saving and peak demand control. BACnet(building automation and control networks) is an international standard communication protocol for building automation and control networks. In this study, we developed an experimental model of BACnet-based daylighting and fluorescent lighting dimming control system. The experimental model consists of lighting control system and a mockup of indoor fluorescent lighting facility, which are interconnected using BACnet protocol. Using the experimental model, we evaluated the performance of BACnet-based lighting control system. Results from the experimental model show that the energy consumption for lighting can be reduced up to 40%. [C1214]

"Self-controlled Exploitation of Energy Cost saving Potentials by Implementing Distributed Demand Side Management"

Facing the shortage of energy resources and rising energy costs, it is crucial to increase the efficiency of energy usage. Daily consumption peaks in electrical power grids result in the necessity to maintain overcapacities that are only temporarily used. Although already deregulated, today's power markets still lack incentive for large consumer groups to avoid peak consumption. This paper discusses a distributed and integrated load management infrastructure based on a self-controlled load shifting strategy which aims to reduce peak consumption. Essential for its effective and flexible operation is the proposed communication infrastructure, which will enable a flow of information in addition to the flow of energy in national and international power grids. This low-cost and maintenance-free infrastructure will carry real-time pricing information and allow load management appliances to communicate with each other. As a result, the consumer can take part in the energy business and profit from shifting part of the daily load to off-peak hours. [C1215]

"Dual-Processor Design of Energy Efficient Fault-Tolerant System"

A popular approach to guarantee fault tolerance in safety-critical applications is to run the application on two processors. A checkpoint is inserted at the completion of the primary copy. If there is no fault, the secondary processor terminates its execution. Otherwise, should the fault occur, the second processor continues and completes the application before its deadline. In this paper, we study the energy efficiency of such dual-processor system. Specifically, we first derive an optimal static voltage scaling policy for single periodic task. We then extend it to multiple periodic tasks based on worst case execution time (WCET) analysis. Finally, we discuss how to further reduce system's energy consumption at run time by taking advantage of the actual execution time which is less than the WCET. Simulation on real-life benchmark applications shows that our technique can save up to 80% energy while still providing fault tolerance [C1216]

"Energy-Awareness in Distributed Java-Based Software Systems"

Distributed Java-based software systems are increasingly deployed onto heterogeneous mobile platforms with limited battery resources. In this domain, it is a crucial issue to preserve the energy resource and prolong the system's lifetime. To address this problem, we first suggest a framework that allows the system engineer to estimate the energy consumption of a distributed Java-based software system both during system construction-time and during runtime. Based on our energy estimation framework, we then present two efficient approaches

for reducing the software system's energy consumption and consequently increasing the system's lifetime. Finally, we discuss our strategy for evaluating our estimation framework and energy saving approaches [C1217]

"Design of Radix-4 SRT Dividers in 65 Nanometer CMOS Technology"

As technology evolves, there is a never ending need to explore design tradeoffs and alternatives. In the CMOS technologies of the recent past where minimizing the die area was crucial, radix-4 minimally redundant SRT dividers were widely used because they only require simple multiples of divisor. Quotient conversion was typically done by on-the-fly conversion. In deep submicron CMOS technology these decisions need to be reconsidered. Now it is attractive to use maximum redundancy to simplify quotient selection. Replacing the on-the-fly conversion that operates on every cycle with an adder that operates only one cycle reduces the switching factor by the order of 29times for the conversion during a double precision division. This is significant because the on-the-fly conversion can consume 30% of the total energy of a divider. Furthermore, the quotient computation is sped up by the elimination of the big lookup table of minimally redundant SRT dividers. To illustrate this concept of trading extra hardware for improved power and speed and a simpler implementation, a radix-4 maximally redundant divider is designed and implemented in 65 nm CMOS technology using an ASIC flow and single, double and triple VTdevices. Clock and data gating and data recirculation techniques are used to save power. Finally, a method to evaluate design alternatives for energy efficiency is proposed that takes into account the active power consumption, the inactive power consumption and the duty cycle [C1218]

"A new high speed dynamic PLA"

This paper presents a new high speed dynamic programmable logic array (DPLA). The conventional level-restored mechanism is eliminated by using a straightforward CMOS inverter at the charge sharing node on the discharge path. This inverter acts as a voltage monitor and can reduce the voltage swing to 1/2 Vddat the product lines or output lines. Thus power saving as well as high speed operation can be achieved. In addition, the smallest size inverter can be easily integrated to the design automation of DPLA without augmenting the structure of PLA. Furthermore, this design simplifies the design effort of buffering NAND gates and almost removes the serious glitch problem. Experimental results show that our proposed DPLA can be operated at high speed (>1GHz) with very small power delay product (PDP) [C1219]

"A New Technique to Exploit Instruction-Level Parallelism for Reducing Microprocessor Power Consumption"

A large portion of the power consumed by a high-performance out-of order microprocessor is attributed to units within the instruction window pipeline stages, from dispatch to commit. Power consumed within the window, and by the overall processor, is reduced by dynamic size adjustment of those units based on program needs. In this article, we introduce a new metric for estimating the instruction level parallelism (ILP) for a group of instructions using a simple ratio of the longest data dependence path's length to the total number of instructions in the group, hence referred to as the longest dependence path ratio (LDPR). We couple this concept with a design where units in the instruction window are divided into segments that are dynamically disabled for power savings when they are unused. The maximum number of enabled segments that a program can utilize is limited based on the amount of ILP estimated using the LDPR. We also show how measuring the LDPR is implemented by a simple extension to the dependence-check-logic at dispatch stage. Results using the LDPR show that power is saved with a minimal impact on performance, by reducing the number of available segments, not only in low ILP periods, but also over those having very high ILP. Using the Wattch power models and the MinneSPEC benchmarks, the LDPR implementation achieves an average of 36.5% of window power savings and 11% overall processor power savings, and with an average performance loss of a very modest 1.9% [C1220]

"PEAN: A Public Key Authentication Scheme in Wireless Sensor and Actor Network"

The Public Key Cryptography (PKC) has been proved to be able to be applied in memory-constrained sensor nodes and have nice properties for secure Wireless Sensor and Actor Network (WSAN). In order to prevent the man-in-the-middle attack, the public keys of nodes in WSAN must be authenticated with each other before communication. In this paper, we propose the PEAN scheme for public key authentication based on the Merkle tree and the deployment location knowledge. By using the deployment knowledge and the unique properties of WSAN like the heterogeneity, PEAN scheme can reduce energy consumption and, trade off the communication overhead and memory usage of heterogeneous nodes in WSAN. By using the oneΓ,Bïway hash functions, PEAN scheme can reduce computation complexity, communication overhead, and therefore save energy consumption comparing with the RSA algorithm and the ECC algorithm. [C1221]

"A Partition-Based Voltage Scaling Algorithm Using Dual Supply Voltages for Low Power Designs"

We proposed an effective voltage scaling technique to assign the supply voltage to gates in the circuit of dual power supplies. The algorithm is composed of a greedy voltage assignment phase and an iterative voltage re-assignment refinement phase. It reduces the total power without performance degradation. We apply the algorithm to several test cases. It shows that on average the total power saved is 54.7%. Compared to the GECVS technique (Kulkami, 2004), our algorithm reduces the number of level converters by 23.2% and the power consumption by 5.5%. The experimental result also shows the distribution of slack in the original and the power optimized designs. It shows that majority slacks of the gates are reduced. The algorithm utilizes the slack of gates to scale down the supply voltage of the gates such that the power consumption is reduced [C1222]

"A Self-Tuning Algorithm for Managing Reconfigurable Cache"

Reconfigurable cache with a set of adjustable configurations can be configured dynamically to adapt itself to the change in program characteristics and has tremendous benefits for performance and energy. However, how to dynamically manage reconfigurable cache is still a cumbersome task left for designers. We introduce a self-tuning algorithm (ETCA), which can dynamically manage reconfigurable cache on a per-phase basis. In contrast with previous works, ETCA seeks not only to lower cache's energy consumption effectively, but also reduce the performance loss due to unnecessary reconfigurations. By simulating numerous MiBench benchmark, the results show that ETCA, when applied to reconfigurable cache, saves on average 38% of total memory access energy compared with a conventional cache and the associated performance loss is close to 1.8% [C1223]

"Bit-Per-Joule Performance of Power Saving Ad Hoc Networks under Mobile Backbone Coverage"

Energy efficient MAC protocols have been developed for wireless sensor and ad hoc networks so that inactive nodes can transition to sleep state to conserve energy. It has been recognized that forming and keeping a continuously awake Connected Dominating Set (CDS) serves to significantly reduce the route setup latency (since it minimizes the number of wakeup operations that are undertaken). Recently published studies show that, under certain traffic conditions, the CDS approach can lead to the reduction of the average level of energy consumption while ensuring a high network throughput level. Under the Mobile Backbone Network (MBN) architecture introduced by I. Rubin et al., a mobile backbone is dynamically constructed to provide a topological covering of the network. Nodes that join the mobile backbone are identified as Backbone Nodes (BNs). In this paper, we study a MBN Power Saving (MBN-PS) system. The dynamically elected BNs are kept active and are used to effectively manage the awake and sleep states of their client nodes. We study the throughput (per-watt) efficiency performance of the MBN-PS protocol by analytical calculations, as well as by extensive simulation evaluations. We analytically show that when the number of active network flows is above a minimal level, the underlying throughput efficiency attained by the MBN-PS scheme is better than that achieved by a corresponding network that does not form a backbone structure. [C1224]

"A Power-aware and Range-free Localization Algorithm for Sensor Networks"

Power efficiency and accuracy are among the primary design requirements of the localization algorithms in wireless sensor networks. However, to the knowledge of the authors, there has been neither previous detailed study on the energy consumption of localization algorithms, nor previous algorithm that considers the power consumption as the main metric. In this paper, we propose a power-aware and range-free localization algorithm, LR-DV-hop algorithm, which can effectively reduce the communication overhead and energy consumption. It is shown in the simulation results that, our algorithm can save up to 50% power consumption of the classical DV-hop algorithm while achieve better localization accuracy [C1225]

"Micro-Frame Preamble MAC for Multihop Wireless Sensor Networks"

MAC protocols based on preamble sampling techniques like WiseMAC and BMAC offer significant energy savings for multihop wireless sensor networks. Although preamble sampling based techniques efficiently reduce idle listening in low-rate data networks, they introduce extra overhead due to possible reception of some irrelevant frames. In this paper, we identify the problem of receiving irrelevant frames and propose to replace the continuous preamble by a series of small frames that we call micro-frames. The resulting Micro-Frame Preamble (MFP) scheme makes it possible for a node to switch its radio off to avoid receiving irrelevant frames and improve energy savings. In the paper, we evaluate the theoretical energy savings of MFP compared with traditional preamble sampling techniques. We also discuss some experiences with our implementation of MFP on the Freescale MC13192 SARD. [C1226]

"Simultaneously Improving Code Size, Performance, and Energy in Embedded Processors"

Code size and energy consumption are critical design concerns for embedded processors as they determine the cost of the overall system. Techniques such as reduced length instruction sets lead to significant code size

savings but also introduce performance and energy consumption impediments such as additional dynamic instructions or decompression latency. In this paper, we show that a block-aware instruction set (BLISS) which stores basic block descriptors in addition to and separately from the actual instructions in the program allows embedded processors to achieve significant improvements in all three metrics: reduced code size and improved performance and lower energy consumption [C1227]

"Dynamic Power Save Techniques for Next Generation WLAN Systems"

The next generation 802.11 systems (802.11n) are geared towards high performance. Higher performance usually means higher dynamic power consumption. In this paper we describe techniques to reduce the dynamic power consumption in WLAN systems to help increase the battery life in mobile systems. Techniques that can be employed at the baseband based on the protocol knowledge, based on the dataflow implementation and microarchitecture techniques are explored. Techniques for the analog/RF portion of the WLAN system are also explored [C1228]

"Retention-aware placement in DRAM (RAPID): software methods for quasi-non-volatile DRAM"

Measurements of an off-the-shelf DRAM chip confirm that different cells retain information for different amounts of time. This result extends to DRAM rows, or pages (retention time of a page is defined as the shortest retention time among its constituent cells). Currently, a single worst-case refresh period is selected based on the page with the shortest retention time. Even with refresh optimized for room temperature, the worst page limits the safe refresh period to no longer than 500 ms. Yet, 99% and 85% of pages have retention times above 3 seconds and 10 seconds, respectively. We propose retention-aware placement in DRAM (RAPID), novel software approaches that can exploit off-the-shelf DRAMs to reduce refresh power to vanishingly small levels approaching non-volatile memory. The key idea is to favor longer-retention pages over shorter-retention pages when allocating DRAM pages. This allows selecting a single refresh period that depends on the shortest-retention page among populated pages, instead of the shortest-retention page overall. We explore three versions of RAPID and observe refresh energy savings of 83%, 93%, and 95%, relative to the best temperature-compensated refresh. RAPID with off-the-shelf DRAM also approaches the energy levels of idealized techniques that require custom DRAM support. [C1229]

"Energy-Efficient Cache Coherence for Embedded Multi-Processor Systems through Application-Driven Snoop Filtering"

Maintaining local caches coherent in bus-based multiprocessor systems results in significantly elevated power consumption, as the bus snooping protocols require local cache lookups for each memory reference placed on the common bus. Such a conservative approach is warranted in general-purpose systems, where no prior knowledge regarding the communication structure between threads or processes is available. In such a general-purpose context the assumption is that each memory request is potentially a reference to a shared memory region, which may result in cache inconsistency, if no correcting activities are undertaken. The approach we propose exploits the fact that in embedded systems, important knowledge is available to the system designers regarding communication activities between tasks allocated to the different processor nodes. We demonstrate how the snoop-related cache probing activity can be drastically reduced by identifying in a deterministic way all the shared memory regions and the communication patterns between the processor nodes. Cache snoop activity is enabled only for the fraction of the bus transactions, which refer to locations belonging to known shared memory regions for each processor node; for the remaining larger part of memory references known to be of no relation to the given processor node, snoop probings in the local cache are completely disabled, thus saving a large amount of power. The experiments which we have performed on a number of important applications demonstrate the effectiveness of the proposed approach [C1230]

"Low-Power Issues for SoC"

Development of semiconductor technology has led to a concept of system-on-chip (SoC). Complexity of modern applications and deep-submicron technologies make low-power design attitude compulsory. The higher the level of abstraction of a design at which power optimizations are applied, the higher are potential savings. In this paper we present an overview of some of the design measures to reduce energy consumption of SoCs [C1231]

"Approximate Data Collection in Sensor Networks using Probabilistic Models"

Wireless sensor networks are proving to be useful in a variety of settings. A core challenge in these networks is to minimize energy consumption. Prior database research has proposed to achieve this by pushing data-reducing operators like aggregation and selection down into the network. This approach has proven unpopular with early

adopters of sensor network technology, who typically want to extract complete "dumps" of the sensor readings, i.e., to run "SELECT *" queries. Unfortunately, because these queries do no data reduction, they consume significant energy in current sensornet query processors. In this paper we attack the "SELECT " problem for sensor networks. We propose a robust approximate technique called Ken that uses replicated dynamic probabilistic models to minimize communication from sensor nodes to the network's PC base station. In addition to data collection, we show that Ken is well suited to anomaly- and event-detection applications. A key challenge in this work is to intelligently exploit spatial correlations across sensor nodes without imposing undue sensor-to-sensor communication burdens to maintain the models. Using traces from two real-world sensor network deployments, we demonstrate that relatively simple models can provide significant communication (and hence energy) savings without undue sacrifice in result quality or frequency. Choosing optimally among even our simple models is NPhard, but our experiments show that a greedy heuristic performs nearly as well as an exhaustive algorithm. [C1232]

"Faster In-Network Evaluation of Spatial Aggregationin Sensor Networks"

Spatial aggregation is an important class of queries for geoaware spatial sensor database applications. Given a set of spatial regions, it involves the aggregation of dynamic sensor readings over each of these regions simultaneously. Nested spatial aggregation involves one more level of aggregation, combining these aggregates into a single aggregate value. We show that spatial aggregate values can often be computed in-network, rather than waiting until the partial aggregate records reach the root as is now the case. This decreases the amount of communication involved in query evaluation, thereby reducing the network's power consumption. We describe an algorithm that allows us to determine when an aggregate record for any spatial region is ready to be evaluated in-network, based on decorating the routing tree with region leader lists. We also identify several important scenarios, such as nested spatial aggregation and filtering predicates, when the savings from our approach are expected to be particularly great. [C1233]

"Workload-Aware Dual-Speed Dynamic Voltage Scaling"

Dynamic voltage scaling (DVS) is a frequently used technique in mobile and embedded systems, aimed at reducing the energy consumption of mobile processors. In systems with a discrete number of frequency levels, existing dual-speed DVS approaches compute an optimal theoretical CPU speed and approximate it by choosing the two neighboring discrete speed levels. By comparing experimentally the energy savings attained with different frequency combinations on a mobile platform, this work shows that choosing the two neighboring frequency levels does not necessarily yield the highest energy savings. As a result of the above observation, this work introduces an online approach to dual-speed DVS that a) formulates a model for speed selection based on the workload characteristics of the current task set, b) computes a frequency pair that yields the best possible energy savings for a given taskset and workload [C1234]

"A noise-tolerant matchline scheme with XOR-based conditional keeper for energy-efficient TCAM"

A novel AND-type match-line scheme with XOR-based conditional keeper for ternary content-addressable memory (TCAM) are presented in this paper. The XOR-based conditional keeper is turned off at some critical moments to reduce the search time and power consumption. High fan-in AND-type match-line schemes are used to demonstrate the effectiveness of the XOR-based conditional keeper in the presence of noise sources. 37.8% search time reduction and 15.6% power saving are achieved by using the proposed TCAM architecture. Based on TSMC 0.13 mum CMOS technology at 1.2 V supply voltage, a 256 words times 128 bits ternary CAM is designed. The simulation results show that the search time of proposed TCAM architecture is 1.17 ns and energy metric of proposed TCAM architecture is 0.752 fJ/search [C1235]

"Low-power and low-latency cluster topology for local traffic NoCs"

In this paper, we introduce a topology for network on chips that is named cluster-mesh (CM) topology. This architecture reduces dynamic and static power consumption in NoCs and can reduce latency of communications in low traffic or local traffic applications. With cluster-mesh topology, area reduction in routers is about 44% and in links we can save more than 50% in area too. The dynamic power in this architecture is reduced more than 20%. The idea of clustering may be applied to some other topologies such as Torus and Octagon [C1236]

"Multi-Bank Main Memory Architecture with Dynamic Voltage Frequency Scaling for System Energy Optimization"

Several techniques were developed to reduce processor consumption which was the predominant source of dissipation. However with the technology evolution and the development of new applications that make heavy use of large memory data size, the energy savings obtained by these techniques become limited. In this article

we showed that dynamic voltage frequency scaling technique (DVFS) increases the main memory consumption. A multi-banked memory architecture, having the capability of setting banks in low power modes when they are not accessed, is adopted to reduce the memory consumption. An approach of tasks allocation and banks configuration reducing the memory energy is developed at system level for multi-task and real-time systems. Experimental results show that, when we combined DVFS technique with an efficient multi-bank architecture and tasks to banks allocation, a system energy saving that reaches 35% is obtained [C1237]

"Compiler-based adaptive fetch throttling for energy-efficiency"

Front-end instruction delivery accounts for a significant fraction of energy consumption in dynamically scheduled superscalar processors. Different front-end throttling techniques have been introduced to reduce the chip-wide energy consumption caused by redundant fetching. Hardware-based techniques, such as flow-based throttling, could reduce the energy consumption considerably, but with a high performance loss. On the other hand, compiler-based IPC-estimation-driven software fetch throttling (CFT) techniques result in relatively low performance degradation, which is desirable for high-performance processors. However, their energy savings are limited by the fact that they typically use a predefined fixed low IPC-threshold to control throttling. In this paper, we propose a compiler-based adaptive fetch throttling (CAFT) technique that allows changing the throttling threshold dynamically at runtime. Instead of using a fixed threshold, our technique uses the decode/issue difference (DID) to assist the fetch throttling decision based on the statically estimated IPC. Changing the threshold dynamically makes it possible to throttle at a higher estimated IPC, thus increasing the throttling opportunities and resulting in larger energy savings. We demonstrate that CAFT could increase the energy savings significantly compared to CFT, while preserving its benefit of low performance loss. Our simulation results show that the proposed technique doubles the energy-delay product (EDP) savings compared to the fixed threshold throttling and achieves a 6.1% average EDP saving. [C1238]

"A Power-Aware Technique for Functional Units in High-Performance Processors"

This paper presents a hardware technique to reduce the static and dynamic power consumption in functional units of a 64-bit superscalar processor. Our approach is based on substituting some of the 64-bit power-hungry adders by others with 32-bit lower power-consumption adders, and modifying the protocol in order to issue as much instructions as possible to those low power-consumption units incurring a negligible performance penalty. Our technique saves between 14.7% and a 50% of the power-consumption in the adders which is between 6.1% and a 20% of power-consumption in the execution units. This reduction is important because it can avoid the creation of a hot spot on the functional units [C1239]

"Reinforcement temporal difference learning scheme for dynamic energy management in embedded systems"

Dynamic power management is a technique to reduce power consumption of electronic systems by selectively shutting down idle components. In this paper a novel and non-trivial enhancement of conventional reinforcement learning is adopted to predict the optimal policy out of the existing DPM policies. Reinforcement learning is a computational approach to understanding and automating goal-directed learning and decision-making. The effectiveness of this approach is demonstrated by an event driven simulator which is designed using JAVA for power-manageable embedded devices. Results of the experiments conducted in this regard establish that the proposed DPM scheme enhances power savings considerably. [C1240]

"Modified Force-Directed Scheduling for Peak and Average Power Optimization using Multiple Supply-Voltages"

In this paper, we consider the problem of peak and average power optimization in high-level synthesis. We focus on the scheduling task under timing constraint using supply voltage scaling since it is considered as the most efficient technique for reducing power consumptions in CMOS circuits. We propose a two-phase heuristic for peak and average power minimization using multiple supply voltages scheduling technique. The first phase is the modified power-force-directed scheduling (MPFDS) heuristic based on the well-known force-directed scheduling technique. The second phase is a post-processing procedure (power-area-saving) that is a revisit of the output schedule from the first phase in order to exploit the available rooms to get more power and/or the operating resources minimization. Results show that our proposed heuristic is capable of achieving near-optimal results with polynomial complexity [C1241]

"Charge recycling in MTCMOS circuits: concept and analysis"

Designing an energy efficient power gating structure is an important and challenging task in multi-threshold

CMOS (MTCMOS) circuit design. In order to achieve a very low power design, the large amount of energy consumed during mode transition in MTCMOS circuits should be avoided. In this paper, we propose an appropriate charge recycling technique to reduce energy consumption during the mode transition of MTCMOS circuits. The proposed method can save up to 46% of the mode transition energy while, in most cases, maintaining, or even improving, the wake up time of the original circuit. It also reduces the peak negative voltage value and the settling time of the ground bounce [C1242]

"Adaptive online scheduling for asymmetric wireless sensor networks"

Increasing onboard processing capabilities of sensors enable self-organization in wireless sensor networks to dynamically adapt to ad-hoc topologies and to react to task or network changes. Such self-organization, however, comes at a cost of additional energy consumption of the sensor nodes with already limited power resources. Energy limitations of sensor nodes in unattended environments require a trade-off between power consumption and topology maintenance. In this paper we present our adaptive online scheduling (AOS) protocol that exploits application based data flow characteristics to reduce power consumption during self-organization. Data flow characteristics is used to govern route selection, and to formulate a collision-free transmission schedule that enables risk-free sleeping time. Our simulation results suggest that AOS's transmission schedule provides more than 50% energy savings in steady state in comparison to SMACS [C1243]

"Sleep Schedule for Fast and Efficient Control of Parameters in Wireless Sensor-Actor Networks"

Wireless sensor-actor networks can provide remote sensing and actuation services in a variety of applications. Depending on the application, the network should rapidly respond to critical variations in sensor input and take appropriate control action by the actor nodes without any delay. In order to prolong the lifetime of sensor networks, energy saving is done using sleep scheduling algorithms. Though the existing methods save energy, they lead to a large increase in end-to-end latency, which affects the efficiency of the sensor-actor network that requires fast control action. We propose a novel sleep schedule for the radio of the nodes for fast and efficient control of parameters (SEC) in sensor-actor networks with a semi-automated architecture that require minimum latency. During normal operation, the sensor nodes sense the parameters periodically using a static schedule. If the value of any parameter exceeds the set point the sink calculates the error signal and the sleep schedule is changed dynamically to activate the actor nodes in the area of interest. The corresponding sensor-actor nodes are made completely active till the error signal becomes zero, i.e. till the parameters are brought within the set point. The objectives of our protocol are to (1) minimize the latency in controlling the parameters by activating the actor nodes for the appropriate duration using the dynamic schedule (2) reduce the energy consumption by activating the neighboring sensor-actor nodes completely, only when parameters exceed the set point. Simulation results show that SEC protocol performs better than S-MAC by providing nearly 80% low latency with minimum energy consumption [C1244]

"Energy Saving Schedule for Target Tracking Sensor Networks to Maximize the Network Lifetime"

Target tracking sensor networks monitor and track the movement of a target object. Energy management in these sensor networks is crucial to prolong the network lifetime. We propose a new protocol EST (energy saving schedule for target tracking sensor networks) that provides a dynamic sleep schedule for the radios such that maximum energy is saved without affecting the sensors' activities. When there is no target, the communication modules of sensor nodes are put into sleep using a static schedule, except the border nodes. Interior nodes do not perform the sensing activity in the surveillance state. If a target arrives, the sleep schedule for the radios is changed dynamically in order to send the arrival message to neighboring sensors. By receiving the arrival message, the sleeping neighbor nodes start sensing. The objectives of our protocol are to (1) balance the lifetime of all the sensor nodes in the network to increase the network lifetime (2) reduce the energy consumption by activating the sensors only when the target arrives in that region. Simulation results show that EST provides a significant amount of energy savings and potentially increases the network lifetime by 25% more than S-MAC at low load [C1245]

"Data Aggregation in Distributed Sensor Networks: Towards An Adaptive Timing Control"

Data aggregation in wireless sensor networks (WSNs) has attracted wide attention since it could reduce the amount of wireless data communication and thus save power consumption, which is one of the top concerns in low-power WSN systems. Given a data aggregation tree (DAT) for data query purpose in a WSN, and the expected query accuracy, we show the feasibility to use a low-cost timing control scheme to adaptively adjust the waiting period in each DAT level so that the end-to-end query delay could be optimized, i.e. without unnecessary pause in an aggregation node. For such an adaptive timing control scheme, we propose to use a finite state machine (FSM)-based auto-feedback control algorithm to adjust the waiting period of each DAT node

to "timely" respond to the queries. Our sensor network simulation results and hardware experiments verify the validity of our proposed timing control scheme [C1246]

"Analysis of pulse signaling for low-power on-chip global bus design"

Pulse signaling is proposed for on-chip global bus design to reduce dynamic power consumption. To maximize power saving, shorter pulse width and longer propagation length are preferred. In this work, a complete set of analytical models are developed for pulse propagation along RLC lines. These models connect line geometries and electrical properties of an input pulse with several important design metrics, such as delay, pulse width, maximum propagation length, and power saving. Excellent model accuracy is achieved as compared to SPICE simulations. These models can be easily implemented into design tools to facilitate the optimization of pulse signaling on lossy on-chip global buses. Furthermore, pulse signaling can be integrated with a time-division scheme to further reduce power consumption. Using the newly developed models, it is demonstrated that more than 70% dynamic power can be saved in this scheme in on-chip bus design [C1247]

"Energy-Efficient Real-Time Heterogeneous Server Clusters"

With increasing costs of energy consumption and cooling, power management in server clusters has become an increasingly important design issue. Current clusters for real-time applications are designed to handle peak loads, where all servers are fully utilized. In practice, peak load conditions rarely happen and clusters are most of the time underutilized. This creates the opportunity for using slower frequencies, and thus smaller energy consumption, with little or no impact on the Quality of Service (QoS), for example, performance and timeliness. In this work we present a cluster-wide QoS-aware technique that dynamically reconfigures the cluster to reduce energy consumption during periods of reduced load. Moreover, we also investigate the effects of local QoS-aware power management using Dynamic Voltage Scaling (DVS). Since most real-world clusters consist of machines of different kind (in terms of both performance and energy consumption) we focus on heterogeneous clusters. For validation, we describe and evaluate an implementation of the proposed scheme using the Apache Webserver in a small realistic cluster. Our experimental results show that using our scheme it is possible to save up to 45% of the total energy consumed by the servers, maintaining average response times within the specified deadlines and number of dropped requests within the required amount. [C1248]

"Energy savings through embedded processing on disk system"

Many of today's data-intensive applications manipulate disk-resident data sets. As a result, their overall behavior is tightly coupled with their disk performance. Unfortunately, most of these applications quickly become disk bound since disk I/O times, the communication latencies, and energy consumption required to transfer disk data to the host machine can be very large. A promising solution to this problem is to embed computational power into the disk storage system. This paper concentrates on such a smart disk based architecture and proposes an automated approach that partitions a given application code between the host machine and the smart disk. The main goal is to perform data filterings, identified at compile time, on the smart disk, thereby reducing the energy spent in communicating disk data to the host unit for processing. To achieve this, the proposed approach uses integer linear programming to identify the code fragments that perform significant data filtering and assigns such fragments to the smart disk for execution. In addition to the communication energy benefits of the proposed approach, we show in this paper that this approach can also help us better exploit the low-power management capabilities provided by the system. Our experiments with four data-intensive applications indicate significant energy savings. [C1249]

"Power-aware scheduling and dynamic voltage setting for tasks running on a hard real-time system"

This paper addresses the problem of minimizing energy consumption of a computer system performing periodic hard real-time tasks with precedence constraints. In the proposed approach, dynamic power management and voltage scaling techniques are combined to reduce the energy consumption of the CPU and devices. The optimization problem is first formulated as an integer programming problem. Next, a three-phase solution framework, which integrates power management scheduling and task voltage assignment, is proposed. Experimental results show that the proposed approach outperforms existing methods by an average of 18% in terms of the system-wide energy savings. [C1250]

"Droop Compensation Technique with Simple Structure for OFDM mobile transmitter"

Generally the system clock is same to OFDM time sample rate at OFDM mobile systems to reduce the power consumption of handheld systems. For this reason, the droop phenomena that both edges of frequency channel band fall down is occurred by the sample-and-hold operation of digital to analog converters. In this paper, we

have proposed the compensation technique to predistort the OFDM subcarriers with the inverse sine before the inverse fast Fourier transformation operation. The proposed technique can be implemented with the one multiplier and look-up table to save inverse sine weighting values operating to the low frequency. We have presented the simulation results on the droop compensation with WiBro standard based on OFDMA in Korea and the measurement results on the droop compensated frequency response [C1251]

"Integrated link/CPU voltage scaling for reducing energy consumption of parallel sparse matrix applications"

Reducing power consumption is quickly becoming a first-class optimization metric for many high-performance parallel computing platforms. One of the techniques employed by many prior proposals along this direction is voltage scaling and past research used it on different components such as networks, CPUs, and memories. In contrast to most of the existent efforts on voltage scaling that target a single component (CPU, network or memory components), this paper proposes and experimentally evaluates a voltage/frequency scaling algorithm that considers CPU and communication links in a mesh network at the same time. More specifically, it scales voltages/frequencies of both CPUs in the network and the communication links among them in a coordinated fashion (instead of one after another) such that energy savings are maximized without impacting execution time. Our experiments with several tree-based sparse matrix computations reveal that the proposed integrated voltage scaling approach is very effective in practice and brings 13% and 17% energy savings over the pure CPU and pure communication link voltage scaling schemes, respectively. The results also show that our savings are consistent with the different network sizes and different sets of voltage/frequency levels [C1252]

"Power-performance efficiency of asymmetric multiprocessors for multi-threaded scientific applications"

Recently, under a fixed power budget, asymmetric multiprocessors (AMP) have been proposed to improve the performance of multi-threaded applications compared to symmetric multiprocessors. An AMP is a multiprocessor system in which its processors are not operating at the same frequency. Power consumption has become an important design constraint in servers and high-performance server clusters. This paper explores the power-performance efficiency of hyper-threaded (HT) AMP servers, and proposes a new scheduling algorithm that can be used to reduce the overall power consumption of a server while maintaining a high level of performance. Prototyping AMPs on a commercial 4-way SMP server, we show that on average 15.6% energy savings and 6.1% slowdown for the HT-disabled case, and 7.1% energy savings and 4.8% slowdown for the HT-enabled case can be achieved across NAS and SPEC OpenMP applications. [C1253]

"On the Use of Nodes with Controllable Mobility for Conserving Power in MANETs"

We explore the idea of using relay nodes with controllable mobility as intermediate hops for reducing the power consumption in a mobile ad hoc network (MANET). We formulate the relay positioning problem and propose four variations of a simple algorithm to compute the optimal position and the movement of the relay nodes. Results from a preliminary simulation study indicate that deployment of relay nodes does result in considerable power savings in MANETs. [C1254]

"A New 6-bit Flash A/D Converter using Novel Two-Step Structure"

In this study, we develop a new kind of 6-bit flash ADC with a new two-step structure to greatly reduce the chip size. The first coarse 4-bit uses an array of CMOS inverters rather than comparators for flash conversion. To detect various input signal levels, we adjust the ratio of channel length and width in the CMOS inverters to change the transition threshold. The result of coarse 4-bit is used to generate a reference level for fine 2-bit converting using full parallel structure. The advantages are that the ADC circuit can save reference resistors and reduce power dissipation. The new 6-bit ADC chip dissipates only 13mW using 0.35mum process when it works at 100MHz [C1255]

"A configuration memory hierarchy for fast reconfiguration with reduced energy consumption overhead"

Currently run-time reconfigurable hardware offers really attractive features for embedded systems, such as flexibility, reusability, high performance and, in some cases, low-power consumption. However, the reconfiguration process often introduces significant overheads in performance and energy consumption. In our previous work we have developed a reconfiguration manager that minimizes the execution time overhead. Nevertheless, since the energy overhead is equally important, in this paper we propose a configuration memory hierarchy that provides fast reconfiguration while achieving energy savings. To take advantages of this hierarchy

we have developed a configuration mapping algorithm and we have integrated it in our reconfiguration manager. In our experiments we have reduced the energy consumption 22.5% without introducing any performance degradation [C1256]

"Reconfiguration of embedded Java applications"

This work presents the development of a coarse grain reconfigurable unit to be coupled to a native Java microcontroller, which is designed for an optimized execution of the embedded application. Code fragments to be accelerated through this unit are identified by profiling the application. The unit is able to explore ILP in a simple way and allows for Java compatibility, while also reducing the number of executed instructions, thus improving the performance with simultaneous energy savings. In many cases, as demonstrated by experiments, it also allows for smaller power consumption. [C1257]

"Energy efficient MPSoC on-chip communication bus synthesis using voltage scaling technique"

This paper presents an energy efficient on-chip communication synthesis for shared bus based architecture. An assumption for the synthesis is that a system has already been partitioned and mapped onto the appropriate modules of a SoC so that size of data to be transferred at each time by an on-chip module is fixed. The problem of communication synthesis is modeled in NLP (nonlinear programming), which finds an energy efficient minimum number of bus(es) and an optimal size of bus width by simultaneously performing resource selection, scheduling, binding and voltage scaling of an on-chip bus. The supply voltage is scaled to reduce the total energy consumption of a bus by exploiting the slack of each on-chip module. The experimental results conducted on real-life examples, demonstrate the synthesis of an energy efficient communication bus with total energy saving up to 44.6% by scaling its supply voltage [C1258]

"Stream Processing in Networks of Smart Devices"

Increasing attention on data streams has led to research in developing systems for querying streaming data. Special challenges arise, when data are gathered using networked devices which have constrained resources. Examples for such systems are sensor networks where motes can use their processing capability to reduce communication and save energy. Yet, it is still an open research issue how stream queries can optimally be processed in such networks. In this paper we address the problem of mapping stream queries to heterogeneous device-networks. We present a metric for handling the trade-off between quality of service (QoS) and energy consumption. This includes a model which describes how query operators and their hosting devices affect energy consumption and QoS. Based on the model we have developed an algorithm that optimizes mappings and the mapped query plans for a given network. We also discuss results calculated by a prototype that uses our metric [C1259]

"Energy-optimal dynamic voltage scaling for sporadic tasks"

Reducing power consumption is a challenge to system designers. Dynamic power management (DPM) and dynamic voltage scaling (DVS) have emerged as efficient solutions to reduce the power consumption of embedded and portable systems. This paper proposes an online dynamic voltage scaling policy expressed as energy-optimal sporadic task scheduling (EOSTS) for sporadic tasks. EOSTS differs from other existing DVS policies in the fact that the former essentially consists of an energy-optimal model, based on strict theorems proving. Four theorems are proposed in this paper altogether, which is helpful to power management policy optimization research. Experimental results demonstrate that EOSTS policy is superior in power saving to general DPM policies [C1260]

"Improved technological solution for urban transportation system by tram"

The paper presents an improved technological solution for the electric drivings of trams KTD, whose aim is to reduce the energetic consumptions and the increase of exploring safeness and travelers comfort. The new solution uses choppers that substitute the accelerator used in the initial technical solution. The analysis of the experimental determinations made over a tram provided with the new equipment (tram no. 106) and respectively over a tram with the old equipment (tram no. 105) from RAT Craiova revealed that the energetic consumptions were reduced to 41.6%. The equipment reliability was also increased, simultaneously with savings in the exploiting costs. The new technological solution includes a monitoring and diagnosis system, that resulted into the diminishing of traffic-faults number, with beneficial effects over the urban traffic fluidity [C1261]

"Enterprise Strategies for Reducing the Life-Cycle Energy Use and Greenhouse Gas Emissions of Personal Computers"

This paper examines the effectiveness of several important enterprise strategies for reducing the life-cycle energy use and greenhouse gas (GHG) emissions of office computers. A modeling framework is presented, which quantifies the annual primary energy use and GHG emissions necessary to maintain and operate an enterprise personal computer (PC) stock. The case of a California-based enterprise with 5,000 desktop PCs is considered as a baseline scenario. The model is applied to estimate technically-achievable reductions in life-cycle energy use and GHG emissions associated with six common enterprise PC management strategies, as compared to the baseline scenario. The total technical potential for primary energy savings is estimated at roughly 60%; the total technical potential for GHG savings is estimated at roughly 35% [C1262]

"Use of a Computer-Based System to Measure and Manage Energy Consumption in the Home"

Energy use in homes represents 21% of US total energy demand in 2004. Managing this sector is an important priority for addressing global warming, conserving resources and improving energy security. Much energy is wasted in delivering energy services not actually used by residents. Two examples include heating/cooling and lighting of unoccupied houses and rooms, and overheating or overcooling to make up for temperature variations. IT-enabled monitoring and control technologies have played an important role in eliminating similar kinds of inefficiencies in other sectors, so it is natural to think that these systems could have an important role in the home as well. The technology level of energy control in most homes is at least 20 years old, with simple programmable thermostats still in only about a quarter of US homes. Networked thermostats, power meters and switches, and zone heating are technologies that can provide information on energy use and allow it to be controlled for distribution only when needed. In addition to direct energy savings, there is also a demand to reduce indirect needs for energy infrastructure through peak shifting, or redistributing of electricity demand more evenly throughout the day. In addition to surveying these energy management issues, this article also relates the experience of a pilot project setting up monitoring/control systems in three Sacramento homes. The design specifications of these systems combine capabilities for Web-based monitoring and control and peak shifting via pre-cooling, and load shedding. The pilot has shown that such a monitoring and control system satisfying the design parameters can be implemented via mainly off-the-shelf parts. Much work remains to be done however, to develop low-cost user friendly systems attractive to typical homeowners [C1263]

"A novel clustering algorithm for efficient energy saving in wireless sensor networks"

Energy efficiency operations are essential in extending wireless sensor networks lifetime. Among the energy-saving-based solutions, clustering sensor nodes is an interesting alternative that features a reduction in energy consumption through: (i) aggregating data; (ii) controlling transmission power levels (iii) balancing load; (iv) putting redundant sensor nodes to sleep. This paper introduces a novel clustering algorithm that uses a distributed approach to set up non-overlapping clusters, while performing cluster heads rotation as well as carrying out other energy intensive tasks. Besides the transmission power and the energy level of each node, the proposed clustering algorithm considers nodes number that a cluster head can handle aiming at ideally partitioning the network. In fact, the nodes number constituting the cluster is confined around a pre-defined threshold, facilitating thus the optimal operation of the medium access control (MAC) protocol. Further, intending to reduce the computation and the communications cost as well as the messages exchanged, the proposed algorithm invokes the cluster formation only at the system activation, and delays as long as possible the cluster head turn over [C1264]

"Distributed cross-layer scheduling for in-network sensor query processing"

In-network sensor query processing is a cross-layer design paradigm in which networked sensor nodes process data acquisitional queries in collaboration with one another. As power efficiency is still one of the most severe constraints in this paradigm, we propose a distributed, cross-layer scheduling scheme for it. In this scheme, each node employs its MAC, routing, and query layers to negotiate with its parent its timing for transmission and constructs a schedule for its query processing. It then follows the schedule to compute, communicate, and sleep in each query processing cycle. This scheduling reduces wasted listening and receiving as well as the switching between active and sleeping modes. Consequently, it results in 50-60% of power saving on real sensor nodes in our experiments. Additionally, it outperforms two existing scheduling schemes both on schedule construction efficiency and on schedule quality [C1265]

"A low power multimedia system based on the microscopic dynamic voltage scaling (DVS)"

This paper presents a DVS based multimedia system which is designed to effectively reduce the power consumption of multimedia signal processor. The DVS control technique of the system capitalizes the microscopic, i.e., frame-wise, variations of processing requirement for the application of reduced supply voltage and frequency levels. The Xscale processor based DVS system is implemented and performs an MPEG-2

audio/video decoder algorithm for experimental verification of the power saving. [C1266]

"OS-aware tuning: improving instruction cache energy efficiency on system workloads"

Low power has been considered as an important issue in instruction cache (I-cache) designs. Several studies have shown that the I-cache can be tuned to reduce power. These techniques, however, exclusively focus on user-level applications, even though there is evidence that many commercial and emerging workloads often involve heavy use of the operating system (OS). This study goes beyond previous work to explore the opportunities to design energy-efficient I-cache for system workloads. Employing a full-system experimental framework and a wide range of workloads, we characterize user and OS I-cache accesses and motivate OS-aware I-cache tuning to save power. We then present two techniques (OS-aware cache way lookup and OS-aware cache set drowsy mode) to reduce the dynamic and the static power consumption of I-cache. The proposed OS-aware cache way lookup reduces the number of parallel tag comparisons and data array read-outs for cache accesses to save dynamic I-cache power in a given operation mode. The proposed OS-aware cache set drowsy mode puts I-cache regions that are only heavily used by another operation mode to reduce leakage power. The proposed mechanisms require minimal hardware modification and addition. Simulation based experiments show that with no or negligible impact on performance, applying OS-aware tuning techniques yields significant dynamic and static power savings across the experimented applications. To our knowledge, this is the first work to explore cache power optimization by considering the interactions of application-OS-hardware. It is our belief that the proposed techniques can be applied to improve the I-cache energy efficiency on server processors mostly targeting on modern and commercial applications that heavily invoke OS activities [C1267]

"On Mining Moving Patterns for Object Tracking Sensor Networks"

In this paper, we propose a heterogeneous tracking model, referred to as HTM, to efficiently mine object moving patterns and track objects. Specifically, we use a variable memory Markov model to exploit the dependencies among object movements. Furthermore, due to the hierarchical nature of HTM, multi-resolution object moving patterns are provided. The proposed HTM is able to accurately predict the movements of objects and thus reduces the energy consumption for object tracking. Simulation results show that HTM not only is able to effectively mine object moving patterns but also save energy in tracking objects. [C1268]

"EEDS/spl I.bar/NR: an online energy-efficient I/O device scheduling algorithm for hard real-time systems with non-preemptible resources"

The challenge in conserving energy in embedded real-time systems is to reduce power consumption while preserving temporal correctness. Much research has focused on power conservation for the processor, while power conservation for I/O devices has received little attention. In this paper, we analyze the problem of online energy-aware I/O scheduling/or hard real-time systems based on the preemptive periodic task model with non-preemptible shared resources. We extend the concept of device slack to support non-preemptible shared resources; and propose an online energy-aware I/O scheduling algorithm: energy-efficient device scheduling with non-preemptible resources (EEDS_NR). The EEDS_NR algorithm utilizes device slack to perform device power state transitions to save energy, without jeopardizing temporal correctness. An evaluation of the approach shows that it yields significant energy savings [C1269]

"An energy-efficient data-dissemination protocol in wireless sensor networks"

A typical data-dissemination sensor network consists of a large number of sensor nodes, which are normally energy-constrained and unlikely to be recharged in field. Redundant sensor nodes are often deployed to increase network robustness, and to extend network lifetime. Target and inquirer mobilities further bring more challenges to large-scale sensor networks. Frequent location updates for multiple inquirers and targets can drain the limited onboard energy excessively. We present EEDD, an energy-efficient data-dissemination protocol to address both the target and inquirer mobility problem and the energy conservation problem. We extend network lifetime by adopting a virtual-grid-based two-level architecture to schedule the activities of sensor nodes. Furthermore, we propose an adaptive scheduling scheme and a data dissemination scheme to reduce sensing delay and packet forwarding delay. The simulation results show that our protocol saves up to twelve times energy without much increased delay when compared with protocol not considering energy efficiency [C1270]

"Lowering total cost of ownership with breakthrough magnetic torque transfer technology"

Maintenance, unscheduled downtime, and energy costs are three of the highest budget items for any facility. Plants across North America are significantly reducing these costs through the use of magnetic torque transfer technology. This paper provides an overview of magnetic torque transfer technology and examines the savings potential that can be achieved with existing equipment. Magnetic torque transfer technology transmits torque

from the motor to the load through an air gap. It works on the principle of magnetic induction and torque is generated as a function of slip between the input and output members. A magnetic coupling consists of two separate components that have no physical contact. Precision machined aluminum rotors containing high energy neodymium-iron-boron permanent magnets are mounted on the load shaft, and a conductor consisting of a steel housing with copper disks is mounted on the motor shaft. The coupling's ability to transmit torque is created by the relative motion between the copper conductor and the magnets. This motion creates a magnetic field in the copper that interacts with the permanent magnets, thus transmitting torque though the air gap between the components. The motor is completely isolated from the load, which eliminates vibration between the units. The resulting decrease in vibration increases equipment life and reduces maintenance costs for such items as bearings, mechanical seals, couplings, etc. Further, isolation of motor and load eliminates the need for time consuming alignments. Unscheduled down time is reduced due to increased equipment reliability. An adjustable speed control device can be obtained using this same technology. Varying the width of the air gap changes the coupling force between the motor and load, producing an infinitely variable and controlled output speed. In industrial fluid or air handling systems, up to 67% energy savings have been realized by slowing the speed of the pump or fan rather than using control valves or dampers to achieve the desired flow. The unrestricted flow saves energy by reducing the load on the motor. The same maintenance and reliability benefits described in the magnetic coupling are also associated with the magnetic adjustable speed drive. Users throughout industry can maximiz- e existing asset value by increasing equipment reliability and up time, reducing maintenance costs, and lowering energy consumption. Magnetic torque transfer technology is providing these benefits to many plants today, for new construction and retrofit applications. Overall, thousands of systems (up to 3,000 HP at 1800 RPM) are currently utilizing this technology. [C1271]

"Energy Efficient Sleep Schedule for Achieving Minimum Latency in Query based Sensor Networks"

Energy management in sensor networks is crucial to prolong the network lifetime. Though existing sleep scheduling algorithms save energy, they lead to a large increase in end-to-end latency. We propose a new sleep schedule (Q-MAC) for query based sensor networks that provides minimum end-to-end latency with energy efficient data transmission. Whenever there is no query, the radios of the nodes sleep more using a static schedule. Whenever a query is initiated, the sleep schedule is changed dynamically. Based on the destination's location and packet transmission time, we predict the data arrival time and retain the radio of a particular node, which has forwarded the query packet, in the active state until the data packets are forwarded. Since our dynamic schedule alters the active period of the intermediate nodes in advance by predicting the packet arrival time, data is transmitted to the sink with low end-to-end latency. The objectives of our protocol are to (1) minimize the end-to-end latency by alerting the intermediate nodes in advance using the dynamic schedule (2) reduce energy consumption by activating the neighbor nodes only when packets (query and data) are transmitted. Simulation results show that Q-MAC performs better than S-MAC by reducing the latency up to 80% with minimum energy consumption [C1272]

"A low power pipelined maximum likelihood detector for 4/spl times/4 QPSK MIMO wireless communication systems"

The authors present a maximum likelihood (ML) detector for multiple-input multiple-output (MIMO) wireless communication systems. The ML detector has been specifically designed to reduce the implementation complexity without significant degradation in bit error rate (BER) performance. In order to identify the optimized fixed-point representation, the ML detector has been simulated with various representations for the received data. The computation process of the channel matrix and constellation symbols in ML detector is simplified by using normalized symbols. Simulation results are provided showing 42% saving in area usage and 68% saving in power consumption compared to a conventional architecture [C1273]

"Leakage-aware SPM management"

Increasing use of scratch-pad memories (SPMs) in embedded systems makes it imperative to consider optimizations tailored to their needs. Since these memories are managed by software, they present unique opportunities to the designer/compiler writer as far as energy optimizations are concerned. This paper proposes and quantifies the benefits of a compiler-directed energy optimization scheme for banked SPMs used to store the data manipulated by an application program. In contrast to most of the prior efforts on SPMs, which focus mainly on performance and dynamic energy consumption, the approach proposed in this paper is leakage oriented. Specifically, it tries to reduce the amount of SPM space (the number of banks) used to strike a balance between leakage and dynamic energy savings, with the goal of minimizing the total energy consumption due to data accesses. This paper presents an ILP (integer linear programming)-based formulation of this problem and evaluates the proposed approach using a set of eight embedded application codes [C1274]

"A computer vision system for monitoring the energy efficiency of intermodal trains"

Intermodal trains are typically the fastest trains operated by North American freight railroads. It is thus ironic that these trains tend to have the poorest aerodynamic characteristics. Because of constraints imposed by equipment design and diversity, there are often large gaps between intermodal loads and these trains incur greater aerodynamic penalties and increased fuel consumption compared to other trains. We conducted train energy analyses of the most common intermodal train configurations operated in North America. It was found that matching intermodal loads with cars of appropriate length reduces the gap length thereby improving airflow. Properly matching cars with loads also avoids use of cars that are longer and thus heavier than necessary. For double stack containers on well cars, train resistance may be reduced by as much as 9% and fuel savings by 0.52 gallon per mile per train. Proper loading of intermodal trains is therefore important to improving energy efficiency. We have developed a wayside machine vision system that automatically scans passing trains and assesses the aerodynamic efficiency of the loading pattern. Machine vision algorithms are used to analyze these images and detect and measure gaps between loads and develop a quantitative index of the loading efficiency of the train. Integration of this metric that we call "slot efficiency" can provide intermodal terminal managers feedback on loading performance for trains and be integrated into the software support systems used for loading assignment [C1275]

"WSN14-3: Honeycomb Architecture for Energy Conservation in Wireless Sensor Networks"

Reducing energy consumption has been a recent focus of wireless sensor network research. Topology control explores the potential that a dense network has for energy savings. One such approach is geographic adaptive fidelity (GAF) [1]. GAF is proved to be able to extend the lifetime of self-configuring systems by exploiting redundancy to conserve energy while maintaining application fidelity. However the properties of the grid topology in GAF have not been fully studied. In this paper it is shown that there exists an unreachable corner in the GAF grid architecture. Using an analytical model, we are able to calculate the unreachable probability and analyse its impacts on data delivery. After investigating a couple of lossless topologies, we propose to use the honeycomb virtual mesh (GAF-h) to replace the square grid. GAF-h is proved to be able to achieve zero loss with little extra cost compared to the original GAF scheme. An efficient honeycomb cell placement and node association algorithm is also proposed. It integrates nicely with the original GAF protocol with little computing overhead. [C1276]

"WSN14-4: Energy-efficient Reliable Transmission Protocol with Outsourcing in WSNs"

Energy has been identified as a crucial resource in wireless sensor networks (WSNs). Since it is usually difficult to recharge the sensors deployed in a remote or hostile environment, reducing the energy consumption is the key to prolong the lifetime of the network. In this paper, we investigate an energy-saving strategy, called outsourcing, which allows a sensor to outsource tasks to others in order to reduce the overall energy consumption as well as the energy consumption of the sensors with low remaining energy. Based on this strategy, we designed an energy-efficient reliable transport protocol that intelligently distributes the task of data recovery. Both analysis and simulations show the significant reduction in energy consumption. In addition, the implementation of the proposed scheme requires minor modification to the existing protocols. [C1277]

"Low power and power aware fractional motion estimation of H.264/AVC for mobile applications"

In this paper, the low power design techniques from algorithm to architecture levels are proposed for fractional motion estimation in H.264/AVC. The proposed AMPD algorithm can reduce 50.8% power with up to 0.1 dB quality drop. The proposed parallel architecture with efficient memory hierarchy can efficiently reuse data and save 61.6% power. Furthermore, the power aware functionality is included. Our design can gracefully vary the quality degradation of 0.1-3.9 dB in response to the 22.58-1.64 mW power consumption. This power-oriented design is very efficient for different mobile applications in various power situations [C1278]

"WLC24-2: Selective Power Management in IEEE 802.11 infrastructure WLANs"

In IEEE 802.11 infrastructure LANs with Distributed Coordination Function (DCF), the power saving algorithm works as follows: the stations with no frames to transmit may switch to the doze mode to save power; all these stations are informed by the Access Point (AP) at the beginning of each beacon interval if there are pending frames; these stations then start contending the channel to receive these pending frames from the AP, if any. In this work, we propose a different strategy based on giving the AP the power of deciding which stations with pending frames to notify. Indeed, there are several circumstances with high channel traffic in which it is better to defer the transmission so as to reduce the expected energy consumption. The reduction in energy consumption is obtained at the expense of an increase in the transmission latency. The AP notification decision is then taken

in view of the total average energy consumption and the introduced latency. Simulations have shown that the performance of the proposed method may lead to an overall energy saving of about 63% respect to the standard algorithm. [C1279]

"WLC30-6: Admission Control in Power Constrained OFDM/TDMA Wireless Mesh Networks"

We investigate connection-level, packet-level, and energy-saving performances in a power constrained (e.g., solar-powered) OFDM/TDMA wireless mesh network. When a mesh router goes to the sleep mode to reduce energy consumption, packet-level performances (as observed by a mesh client) will be degraded since in sleep mode, a mesh router can neither receive nor transmit packets. An analytical model is developed to analyze the relationship among the packet-level and the connection-level performances. Based on the analytical model, the system performance is analyzed in terms of system utility. To this end, an optimization problem is formulated by using a Markov decision process to choose the optimal policy on sleep management and maximum number of admissible connections at a mesh router so that the system utility is maximized. [C1280]

"WLC41-6: Cooperative Relay Networks Using Fountain Codes"

We investigate a cooperative communications scheme with Nparallel relays, where both the transmissions from the source to the relays and from the relays to the destination use fountain codes. Receivers for fountain codes can accumulate mutual information, while traditional energy collection methods, such as repetition or cooperative space-time codes, only accumulate energy. As a consequence, using fountain codes can reduce the total energy required for transmitting data from the source to the destination. We first analyze the scenario where the source stops transmitting and the relay nodes start transmitting after Lrelay nodes have successfully decoded the source data. We optimize L, and also give closed-form equations for the energy savings that can be achieved by the use of mutual-information-collection at the receiver instead of traditional energy-collection methods. We then analyze an alternate scenario where each relay node starts its transmission to the destination as soon as it has decoded the source data, and helps the other relay nodes that are still in reception mode. Doing so further reduces the total transmission time and energy consumption. [C1281]

"Low Power Trellis Decoder with Overscaled Supply Voltage"

This paper is interested in applying voltage over-scaling (VOS) to reduce trellis decoder energy consumption, where the key issue is how to minimize the decoding performance degradation due to VOS-induced errors. Based on the fact that the integrity of different bits in the trellis state metric has (largely) different effect on the overall trellis decoding performance, we proposed an importance-aware clock skew scheduling technique that assigns those more important bits with longer timing slacks and hence better immunity to VOS-induced errors. This will provide system-level tolerance to VOS-induced errors in trellis decoders. With Viterbi and Max-Log-MAP decoders as test vehicles, we demonstrated that about 30% energy savings on trellis state metric computation can be realized with negligible decoding performance degradation [C1282]

"Efficient Memory Reuse and Sub-Pixel Interpolation Algorithms for ME/MC of H.264/AVC"

This paper presents efficient memory reuse and sub-pixel interpolation algorithms for ME (motion estimation)/MC (motion compensation) of H.264/AVC ME is a computationally intensive task and its number of memory accesses is quite high. Moreover, sub-pixel interpolation requires many additions and multiplications. The proposed memory reuse algorithm utilizes the position similarity of the MVp (motion vector prediction) among neighboring Sub-MBs (macro blocks). It can reduce a large number of memory accesses and can save power consumption by sharing SR (search range) of the current block. In addition, simplifying weights of sub-pixel interpolation can eliminate multiplications. Thus, this algorithm can reduce its complexity and power consumption. Therefore, the proposed memory reuse and sub-pixel interpolation algorithms can be employed for low power video compression [C1283]

"Data-Driven Techniques for Low-Energy Video Processing"

The explosive growth of portable video applications has elevated needs for low-energy video processing hardware. This paper presents algorithmic and architectural techniques capable of reducing the energy dissipation of video codec considerably. The focus is put on adaptive approaches, which dynamically adjust the number of operations, the operational bit-width, and voltage supply to varying picture content. We describe the strengths of techniques in terms of energy savings and design complexity and overview issues of their practical use. [C1284]

"Isochronous MAC using Long-Wave Standard Time Code for Wireless Sensor Networks"

This paper proposes isochronous-MAC (I-MAC), which utilizes low-frequency radio waves time synchronization for sensor networks. Using IMAC, based on the low power listening (LPL), all sensor nodes wake and listen channel periodically and synchronously. Since a sender can easily predict wakeup time of an intended receiver, it can shorten the length of preamble to make the receiver prepare for reception of the following data packet. This saves power consumption for the sender to rendezvous with the receiver. In the paper, we use an analytical model to investigate the impact of the data transmission frequency, the number of neighboring nodes, the wakeup period, the clock drift, and the time-synchronization frequency on the power consumption for consideration of the power overhead to perform the time synchronization. Those results demonstrate that I-MAC allows determination of any arbitrary wakeup period without much difficulty, whereas LPL requires a much more careful setting of the wakeup period because its optimum wakeup period is sensitive to the frequency of data transmission as well as to the number of neighboring nodes. Therefore, IMAC has a great potential to reduce the power consumption in most situations compared with LPL, in spite of the overhead to perform time synchronization. [C1285]

"Efficient Relaying of Video Packets over Wireless Ad hoc Devices"

Wireless channels in ad hoc networks are essentially erroneous, unstable, and restricted in capacity, which does challenge video communication. In this paper, the authors introduce a novel design for ad hoc devices that relay real-time video packets. Transiently "caching" packets allows an intermediate node to respond to ARQ requests, which obviously enhances the reliability of retransmission and reduces cumulative power consumption. Additionally, each node smartly selects packets to forward once the channel cannot accommodate all of them. The authors also propose a jointly discarding mechanism in which stale packets and their dependent ones can be detected and destroyed to save energy and bandwidth. The framework has been realized over a real-life testbed, clearly showing its soundness. [C1286]

"A Low-Power Folded Programmable FIR Architecture"

Based on the radix-4 Booth algorithm, a scheme that integrates tap folding and coefficient folding is proposed to design a programmable finite impulse response (FIR) architecture with low power dissipation. In addition, without increasing hardware complexity and degrading computational performance, the effective selection on input data is realized to lower the operating frequencies of the latches and multiplexers involved with the input data. With the reduction on the frequency of the input data being selected to the Booth decoders, the power consumed in the Booth decoders can be also minimized. The proposed and conventional FIR architectures are implemented using the TSMC 0.18 mum CMOS technology. The areas and power consumption of these architectures are analyzed and compared. Under the same specifications and throughput rate, the results revealed that in comparison to the conventional architectures, the proposed FIR architecture not only saves about 18.18% to 39.19% of area occupied, it also reduces 14.23% to 25.56% in power consumption [C1287]

"Functional Unit Selection in Superscalar Microprocessors for Low Power"

A novel technique is introduced to reduce power consumption in functional units (FU). Extra slower FU with lower per-execution energy consumption are added into a processor. Thus, through code scheduling, instructions whose results are not immediately referenced after completion are issued to these power-frugal FU. Simulation suggests a prospect of saving 20% to 30% energy consumption in addition instructions while still improving the performance [C1288]

"A Novel Low-Power and High-Speed Master-Slave D Flip-Flop"

A novel low-power and high-speed master-slave D flip-flop (MSDFF) is proposed in this paper. Without clocked inverter on critical path, the flip-flop operation speed has been improved. Employing the pseudo-NAND logic in the slave stage, the flip-flop has a smaller clock capacitance load, which helps to reduce the power consumption. The proposed flip-flop is verified with GSMC 1.5 V-0.15 mum CMOS technology. Compared with the widely used conventional D flip-flop, 48% power-delay-product (PDP) saving can be achieved, and both the power consumption and transition delay performance are better than many other flip-flops [C1289]

"A New Thermal-Conscious System-Level Methodology for Energy-Efficient Processor Voltage Selection"

In this paper, we propose a thermal-conscious system-level methodology to make energy-efficient voltage selection (VS) for nanometer processors under real-time constraints. New modeling parameters, such as power composition ratio (PCR), thermal resistance, are integrated and considered in our system models, and their impacts on energy consumption are explored. The interdependence between temperature and power is modeled in an iterative way and two nonlinear programming formulations are presented to determine the optimal energy-

efficient supply voltages. Our experiment results show that the energy estimation discrepancy given by the thermal-conscious and traditional system models can reach up to 50% in 65nm PTM CMOS technology, which again underscores the necessity of a thermal-aware power model. Furthermore, our thermal-conscious voltage selection (TCVS) approach can achieve up to 12% further energy savings and much lower peak temperature than the traditional approach. Finally, our specific temperature voltage selection (STVS) approach can reduce the computation complexity greatly with acceptable energy overheads compared with TCVS [C1290]

"Traffic Allocation in Delay-Tolerant Wireless Ad Hoc Networks"

We analyze the problem of minimizing the energy required to send a faced amount of data subject to delay constraints on portable networks. We develop a traffic allocation algorithm based on dynamic programming using a finite time horizon, and assuming that the network topology is uncertain. We demonstrate that portability reduces the energy consumption of wireless networks compared with stationary configurations. The proposed traffic allocation algorithm adaptively finds the optimal allocation strategy for the delay-constrained traffic by exploiting the statistics of portability in wireless networks. The quantitative results show that the proposed algorithm saves a total energy of up to 55% over a strategy which allocates a constant amount of traffic per stage [C1291]

"Energy and Channel Aware Geographic Forwarding Algorithms for Wireless Sensor Networks"

In this paper we investigate energy efficiency and performance of a multi-hop communication in a wireless sensor network where energy efficient geographic forwarding algorithms are implemented. Starting from a reference case, based on geographic information only, which optimizes the advancement toward the destination, we introduce here adaptive strategies that exploit channel and energy information and try to optimize the energy consumption or the energy-to-advancement ratio. We also propose an integrated MAC algorithm, which uses forwarding metrics to control the contention of the channel, and explore the possible benefits that can be gained by the use of coding which reduces the power requirements in the transmission of the data packets. The results show that the use of channel and energy information in the forwarding process improves the energy efficiency, but the gain achievable is heavily influenced by the fixed energy cost of MAC operations. However, the proposed MAC design keeps the energy cost limited and independent of the node density. It is also shown, that the use of coding does not reduce energy consumption when the required processing is energy consuming. The best energy behavior is achieved by the forwarding algorithm that minimizes the energy-to-advancement ratio which saves 20-40% of energy with respect to the reference case [C1292]

"Decomposing Data-Centric Storage Query Hot-Spots in Sensor Networks"

Arising when a large percentage of queries is accessing data stored in few sensor nodes, query hot-spots reduce the quality of data (QoD) and the lifetime of the sensor network. All current in-network data-centric storage (IN-DCS) schemes fail to deal with query hot-spots resulting from skewed query loads as well as skewed sensor deployments. In this paper, we present two algorithms to locally detect and decompose query hot-spots, namely zone partitioning (ZP) and zone partial replication (ZPR). We build both algorithms on top of the DIM scheme, which has been shown to exhibit the best performance among all INDCS schemes. Experimental evaluation illustrates the efficiency of ZP/ZPR in decomposing query hot-spots while increasing QoD as well as energy savings by balancing energy consumption among sensor nodes [C1293]

"NGL02-2: Ethernet Adaptive Link Rate (ALR): Analysis of a Buffer Threshold Policy"

Rapidly increasing energy use by computing and communications equipment is a significant problem that needs to be addressed. Ethernet network interface controllers (NICs) consume hundreds of millions of US$ in electricity per year. Most Ethernet links are underutilized and link power consumption can be reduced by operating at lower data rates. An output buffer threshold policy to change link data rate in response to utilization is investigated. Analytical and simulation models are developed to evaluate the performance of Adaptive Link Rate (ALR) with respect to mean packet delay and time spent in low data rate with Poisson traffic and 100 Mb/s network traces as inputs. A Markov model of a state-dependent service rate queue with rate transitions only at service completion is developed. For the traffic traces, it is found that a link can operate at 10 Mb/s for over 99% of the time yielding energy savings with no user-perceivable increase in packet delay. [C1294]

"NIS05-5: Energy Efficient Wireless Encryption"

The current encryption standard for wireless networks recommend using the AES cipher in the counter (CTR) mode for confidentiality and in the cipher block chaining (CBC) mode for authentication. In the counter mode, a 128 bit counter is encrypted using the AES into 128 bit keystream which is then XORed with 128 bits of plaintext before transmission. This operation is repeated for the entire frame and results in heavy energy consumption for

larger frames. In this paper, we propose a novel cipher called High Diffusion (HD) cipher that securely expands a given 128 bit counter value to a larger 288 bit keystream during encryption, thus reducing the number of encryptions per frame compared to the AES. We show that the HD cipher is as secure as the AES under differential, linear cryptanalysis and the Square attack. Using an experimental set up consisting of a laptop with 1.8 GHz Pentium 4 processor and an Intrinsyc CerfCube with 233 MHz ARM processor we measure the energy consumption of both the AES and the HD cipher encryption operation. We observe that using HD cipher instead of AES for encryption will result in about 40% saving in energy consumption on both the laptop and the CerfCube. We also observe that energy efficiency due to HD cipher is significant for larger frame lengths. [C1295]

"WLC17-5: Improving Mobile Station Energy Efficiency in IEEE 802.16e WMAN by Burst Scheduling"

In this paper, we tackle the packet scheduling problem in IEEE 802.16e wireless metropolitan area network (WMAN), where the Sleep Mode is applied to save energy of mobile stations (MSs). Our objective is to design an energy efficient scheduling policy which works closely with the sleep mode mechanism so as to maximize battery lifetime in MSs. To the best of our knowledge no power saving scheduling algorithms based on sleep mode defined in IEEE 802.16e have been proposed so far in the literature. We propose a longest virtual burst first (LVBF) scheduling algorithm which schedules packets of MSs in a virtual burst mode where there is one primary MS and multiple secondary MSs sharing the wireless link resource. LVBF prolongs MSs' lifetime by reducing the average time when MSs stay in the idle state and the number of state transitions between the awake and sleep states. Simulation results show that, in comparison with the round robin scheduling scheme, LVBF can produce significant overall energy saving, while guaranteeing the QoS requirements of MSs in terms of their minimum data rates. [C1296]

"A Novel Hardware Architecture for Low Power and Rapid Testing of VLSI Circuits"

During built-in self-test (BIST), the set of patterns generated by a pseudo-random pattern generator may use longer time and more power consumption in testing. In this paper, we propose a novel hardware architecture base on "LBIST Controller" to reduce test application time and test power consumption. Give a test cubes for stuck-at faults contain unspecified bit generated by a sequential automatic test pattern generator (ATPG). Use our propose algorithm in section III can group test cubes to several section schemes. Then mapping to our propose hardware architecture in section II. While "Section Counter" is more then zero, scan in could through MUX and bypass the flip-flops in "Fixed Group". And we can save power consumption and test application time in this time. According to our simulation result, we reduce about 20% ~ 60% power consumption and 50% ~ 80% test application time in some ISCAS'89 benchmarks [C1297]

"A Scheduling Algorithm for Reducing Energy Based on Dynamic Switch-off WNICAdaptively"

This paper presents a scheduling algorithm of dynamic switch-off WNIC for power saving. How to make sure the switch time for WNIC 's power mode transition is a crucial issue in the proposed scheduling algorithm. We use grey model to predict idle period for WNIC. A self-adaptive rolling prediction is implemented to improve the accuracy of predicted results by adjusting parameters dynamically. The simulation result shows it works well with good prediction accuracy and small computational capability. [C1298]

"Uncertain Data Management for Wireless Sensor Networks Using Rough Set Theory"

The wireless sensor networks (WSN) is a new emerging field with many sensor nodes deployed in a wide sphere to carry out a certain task. Considering the features of limited energy and densely deployed sensor nodes, the key challenge in wireless sensor networks is to reduce the power consumption and the high information redundancy. Furthermore, communication is widely viewed as the dominating power cost in many sensor networks applications, so it is obvious that it will save energy if data is aggregated before being sent to the sink node. As the illustrative examples are shown, rough set theory is a useful tool for local redundancy information de-correlation and can eliminate redundant transmission so as to provide a solution to uncertain data management for wireless sensor networks [C1299]

"Statistical analysis of Power Delay Estimation in adder circuit using non-clocked pass gate families"

In the present paper we have designed a 16-bit adder circuits with basic pass transistor circuit approach and different topology for implementation. The proposed multiplexing control input techniques of the adder circuits are developed by the carry save adder (CSA) technique. The different logic cells, used for various pass gates circuit

design styles are evaluated in terms of area, propagation delay, power dissipation and propagation delay product. The design styles are compared by performing detailed transistor-level simulations on a benchmark circuit (CSA adder) using DSCH3 and Microwind3. We have analysed the results in a statistical way. We have compared our results with the various published results of adder circuits. We found that the speed of the proposed circuit is enhanced and power consumption as well as the area has reduced tremendously due to multiplexing control input technique. Comparing the simulated results with other pass logic designs, it was observed that in all existing logic CPL is a promising candidate for future logic design. [C1300]

"A Low Power SRAM Architecture Based on Segmented Virtual Grounding"

A novel architecture for the reduction of both dynamic and static power consumption of static random access memories (SRAM) is presented. The scheme is based on the segmented virtual grounding (SVGND) of the SRAM cells. Substantial leakage reduction is achieved by increasing the threshold voltage of the cell transistors through body effect. The write and read energy consumptions are reduced significantly by decreasing the bitline voltage swing and the number of bitlines affected in each transaction. Unlike recently reported low-power schemes, SVGND allows multiple words to be placed in each row while keeping the dynamic power low. This feature is achieved by introducing an additional operation mode to the SRAM cells. The architecture is implemented in a 130nm CMOS technology. Using this scheme, the read and write array energy consumption can be saved by 44% and 84% respectively. Measurement results portraits 15 times leakage reduction compared to the conventional scheme [C1301]

"Power-Conscious Configuration Cache Structure and Code Mapping for Coarse-Grained Reconfigurable Architecture"

Coarse-grained reconfigurable architecture aims to achieve both performance and flexibility. However, power consumption is no less important for the reconfigurable architecture to be used as a competitive processing core in embedded systems. In this paper, we show how power is consumed in a typical coarse-grained reconfigurable architecture. Based on the power breakdown data, we suggest a power-conscious configuration cache structure and code mapping technique, which reduce power consumption without performance degradation. Experimental results show that the proposed approach saves much power even with reduced configuration cache size [C1302]

"Reducing Power through Compiler-Directed Barrier Synchronization Elimination"

Interprocessor synchronization, while extremely important for ensuring execution correctness, can be very costly in terms of both power and performance overheads. Unfortunately, many parallelizing compilers are very conservative in inserting barrier synchronizations at the end of each and every parallel loop. This can lead to significant power consumption in chip multiprocessor based execution environments. This paper proposes a compiler-directed approach for eliminating such synchronization calls between neighboring parallel loops. It achieves its goal by partitioning loop iterations across processors such that each processor executes iterations from both the loops that access the same set of array elements. We implemented the proposed approach using an experimental compilation framework and made experiments with ten SPEC benchmark codes. Our experiments clearly show that the proposed compiler-directed approach is very effective and reduces energy overheads due to synchronizations by about 75.5%, and this corresponds to around 5.48% saving on average in overall energy consumption [C1303]

"Energy-efficient Motion Estimation using Error-Tolerance"

Presented is an energy-efficient motion estimation architecture using error-tolerance. The technique employs overscaling of the supply voltage (voltage overscaling (VOS)) to reduce power at the expense of timing errors, which are then corrected using algorithmic noise-tolerance (ANT) techniques. Referred to as input subsampled replica ANT (ISR-ANT), the proposed technique incorporates an input subsampled replica of the main sum of absolute difference (MSAD) block for obtaining the motion vectors in the presence of errors induced by VOS. Simulations show that the proposed technique can save up to 60% power over an optimal error-free present day system in a 130nm CMOS technology. Power savings increase to 79% in a 45nm predictive process technology [C1304]

"Reducing Cache Traffic and Energy with Macro Data Load"

This paper presents a study on macro data load, an efficient mechanism to enhance loaded value reuse. A macro data load brings into the processor a maximum-width data value the cache port allows, saves it in an internal structure, and facilitates reuse by later loads. A comprehensive limit study using a generalized memory value reuse table (MVRT) shows the significantly increased reuse opportunities provided by macro data load. We also describe a modified load store queue design as an implementation of the proposed concept. Our

quantitative study shows that over 35% of L1 cache accesses in the SPEC2k integer and MiBench programs can be eliminated, resulting in a related energy reduction of 24% and 35% on average, respectively [C1305]

"Power Reduction of Multiple Disks Using Dynamic Cache Resizing and Speed Control"

This paper presents an energy-conservation method for multiple disks and their cache memory. Our method periodically resizes the cache memory and controls the rotation speeds under performance constraints. The cache memory stores the data from the disks for reuse. Enlarging the cache memory reduces disk accesses and disk utilization. This allows the disks to reduce their speeds and conserve energy because the disks' power consumption is quadratic to their speeds. However, the cache memory itself consumes power to retain data. Shrinking cache memory can save memory power while increasing disk accesses and degrading performance. Choosing proper cache sizes and rotation speeds can reduce the energy consumption of both memory and disks with satisfactory performance. We model cache resizing and speed setting as an optimization problem with minimizing the power consumption as objective and limiting disk utilization as constraints. We compare our method with the methods resizing cache based on request rates. The simulation results show that our method achieves better energy-savings while limiting disk access latency [C1306]

"Selective Microarchitecture-Level Scaling for Energy Savings"

Scaling the clock frequency and supply voltage during every cache miss has been shown to substantially reduce the energy dissipation of the processor, while incurring a modest performance penalty. However, not all cache misses have the same effect on performance. Modern superscalar processors may idle during some cache misses, but continue to execute other instructions during other cache misses. Slowing the CPU on these latter cache misses saves little energy, while adversely affecting the overall performance. In this paper we present a small, accurate table-based approach to speculatively identify those cache misses that do and do not benefit from scaling. By judiciously slowing down only those memory instructions for which the processor has a large idle time, we are able to capture most of the energy savings while avoiding much of the performance penalty. Our approach achieves an energy savings of 16% on average through frequency scaling, with a performance penalty of only 6%. [C1307]

"A novel low-power physical design methodology for MTCMOS"

The optimization of virtual supply network plays an important role in MTCMOS low power design. Existing low power works are mainly on gate-level without any optimization on physical design level, which can lead to large amount of virtual supply networks. This paper presents (1) a low power driven physical design flow; (2) a novel low power placement to simultaneously place standard cells and sleep transistors and (3) sleep transistor relocation technique to further reduce the virtual supply networks. Experiment results are promising for both achieving up to 28.15% savings for virtual supply networks and well controlling the increase of signal nets [C1308]

"Power Management Mechanism for routing in Ad-Hoc Wireless Networks"

Power control techniques are used in wireless communications to reduce interference and save energy. This strategy has particularly interesting applications in a multihop MANET(mobile ad-hoc networks), because the transmission power required for the communication between two nodes is increased exponentially with their distance, and the total power required to transmit a packet via multihop may be less than the energy required to transmit it directly. In this paper, we propose a new power saving mechanism in a tree constructed by TDA (topology discovering algorithm) (Zabian and Bonuccelli, 2005). The idea is the reduction of power consumption in each node (when it is possible) by adjusting the transmission range that allows a significant power saving in all the network. Our results show that, the power consumption in a tree like that constructed by TDA is related to the height of the tree and tightly related to the packet size. [C1309]

"DS2IS: Dictionary-based Segmented Signal Inversion Scheme for Low Power Dynamic Bus Design"

As technology scales down to nanometer technology, coupling effects between neighboring wires have a significant impact on power consumption and signal integrity on on-chip interconnects. Especially, on-chip inductive effects need to be taken into account due to low-resistance metal interconnection and fast signal transition times in nowadays IC design. In this paper, we propose a low power bus encoding scheme which reduces the capacitive and inductive effects between bus wires simultaneously by the measurement of real RLC model. The experimental results showed that our approach can save power consumption of the bus up to 15%. [C1310]

"Genetic Algorithm Based Idle Length Prediction Scheme for Dynamic Power Management"

Reducing energy consumption has become one of the most important challenges in designing computing systems. Dynamic power management policies exploit components' idle periods to save energy. If one idle period of some component is long enough, the component can be put into low power state during this period in order to reduce energy consumption. Many dynamic power management policies are based on predicting lengths of components' future idle periods. The more accurate the prediction is, the more efficient the policy is. This paper proposes a novel idea of using genetic algorithm to predict lengths of future idle periods. We take K adjacent idle periods and active periods as a load-gene and define some kinds of relationships between adjacent load-genes, then use genetic algorithm to predict future load-genes that most accords with the relationships. Experimental results show that the proposed scheme is more efficient than the exponential-average approach [C1311]

"Selective Placement Data Cache for Low Energy Embedded System"

This paper proposes a process aware selective placement scheme for N-way set associative cache with the help of a victim set. In this work, we consider the data cache subsystem, as it is one of the most power consuming microarchitectural parts of an embedded system and set associative cache, being one of the popular mapping schemes for data cache. We propose a selective placement scheme to reduce tag comparison and power consumption using victim set. We show that, this scheme has reduced the tag comparison by 70% and power saving by 72% as compared to conventional caching scheme. Experimental results are obtained using Simplescalar 2.0 cache simulator for SPEC95benchmark suite. [C1312]

"Simulation and Efficient Implementation of Low Power Time Diversity Receiver for Mobile Communications"

This paper presents a novel and efficient implementation of a CDMA Rake receiver, analysis and simulation of his operation. A Rake structure is used to resolve the time diversity due to the multipath propagation. The focus has been on doing an implementation with small memory footprint and low power consumption and simulation of the realized structure. Also, another aim of this paper was to incorporate a new signal detection technique within the Rake receiver of the Code Division Multiple Access (CDMA) system, which is able to identify every "important" multipath in the unknown channel using the Least Mean Square (LMS) algorithm. By moving the time alignment of the "fingers " (multipath components) from the beginning of a Rake receiver to the end, it is shown that not only will be saved area, but also it is reduced the power consumption. And by using techniques like clock gating, the power consumption and area are reduced even more. [C1313]

"Comparative Study of Energy Assessment from Apparel Industries: The Context of Sri Lanka"

Industrial sector consumes significant proportion of world's energy for their construction, operation, maintenance, renovation, demolition and disposals. There is a continued increase in demand for energy to meet the growing industrial needs of rapidly increasing population. To cater the future demand, it is important to conserve energy by efficient use of resources and equipments. Apparel sector is one of the energy intensive sectors of the country. The cost of energy substantiates a significant component of its total operational cost. Therefore, study of energy consumption and identification of the potential for energy conservation is crucial to ensure industrial competitiveness on a global scale. This paper has aimed to assess the energy consumption of apparel sector in terms of equipments used and functional areas occupied. The methodological approach of this study includes walk through audits, detail audits, and interviews with selected management staff. From the study, it has been found that the major energy consumer is air conditioner which records average percentage of 46 % of the total energy consumed. Whereas, the areas wise assessment reveals that sewing area consume major part of the energy which is in the range from 40-65% of the total energy consumed. It has also been found that the potential for energy saving in this sector is in the region of 15-30%. Therefore, this study has attempted to make some recommendation for the energy efficiency by doing a cost benefit analysis for the energy efficiency measures. This in turn will reduce the cost of energy and products and help to achieve the competitive advantage [C1314]

"Power Optimized Dictionary Coding for Test Data Compression"

To handle large volume of test data required for testing a System-on-a-Chip (SoC) demands test data compression techniques. Again power consumption during testing is becoming a major concern. Our paper presents a method of reducing power taking into consideration the dictionary based compression technique proposed in literature, where indices of the dictionary are used for compressing test data. Paper shows how power can be reduced by judicious allocation of dictionary indices to the coded words and the prefix bit selection

to differentiate dictionary and non-dictionary entries. The power reduction achieved does affect neither the compression ratio nor the Test Application Time (TAT). It also does not increase the hardware overhead. Experimentation with ISCAS89 benchmark circuits shows up to 71% saving in power. [C1315]

"Efficient Motion Estimation Accelerator for H.264/AVC"

This paper presents efficient memory reuse and sub-pixel interpolation algorithms for ME (motion estimation)/MC (motion compensation) of H.264/AVC. ME is a computationally intensive task and its number of memory accesses is quite high. Moreover, sub-pixel interpolation requires many additions and multiplications. The proposed memory reuse algorithm utilizes the position similarity of the MVp (motion vector prediction) among neighboring Sub-MBs (macro blocks). It can reduce a large number of memory accesses and can save power consumption by sharing SR (search range) of the current block In addition, simplifying weights of sub-pixel interpolation can eliminate multiplications. Therefore, the proposed memory reuse and sub-pixel interpolation algorithms can be employed for low power video compression. In addition, the proposed ME accelerator uses the proposed algorithms. Performance comparisons show a significant improvement compared with existing ME accelerators. [C1316]

"A Block Scaling FFT/IFFT Processor for WiMAX Applications"

This paper presents a low-power design of a two-stream MIMO FFT/IFFT processor for WiMAX applications. A novel block scaling method and a new ping-pong cache-memory architecture are proposed to reduce the power consumption and hardware cost. With these schemes, half the memory accesses and 64-Kbit memory can be saved. Furthermore, by proper scheduling of the two data streams, the proposed design achieves better hardware utilization and can process two 2048-point FFTs/IFFTs consecutively within 2052 cycles. A test chip of the proposed FFT/IFFT processor has been designed using UMC 0.13 mum 1P8M process with a core area of 1332times1590 mum2. The SQNR performance of the 2048-point FFT/IFFT is over 48 dB for QPSK and 16/64-QAM modulations. Power dissipation of two 2048-point FFT computations is about 17.26 mW at 22.86 MHz which meets the maximum throughput rate of WiMAX applications. [C1317]

"Decomposing Data-Centric Storage Query Hot-Spots in Sensor Networks"

Arising when a large percentage of queries is accessing data stored in few sensor nodes, query hot-spots reduce the quality of data (QoD) and the lifetime of the sensor network. All current in-network data-centric storage (IN-DCS) schemes fail to deal with query hot-spots resulting from skewed query loads as well as skewed sensor deployments. In this paper, we present two algorithms to locally detect and decompose query hot-spots, namely zone partitioning (ZP) and zone partial replication (ZPR). We build both algorithms on top of the DIM scheme, which has been shown to exhibit the best performance among all INDCS schemes. Experimental evaluation illustrates the efficiency of ZP/ZPR in decomposing query hot-spots while increasing QoD as well as energy savings by balancing energy consumption among sensor nodes. [C1318]

"Algorithmic Design of High-Precision Low-Power Multi-Stage Decimation Filters"

An algorithm for design of high-precision low- power decimation filters for DeltaSigma analog-to-digital converters is described. This algorithm has been applied to decimation filters with oversampling ratios of 32 to 256, passband ripples of 2 to 0.0003 dB, stopband attenuation of -30 to -120 dB, and passband edge of 0.35 fs to 0.454 fs, where fs is the output sampling rate. This paper then goes forward by presenting a multiplierless, low- power multi-stage digital filter for decimation in DeltaSigma converters. A four-stage decimation filter with down-sampling factor of 64 is developed. A multi-stage CIC (Cascaded Integrator-Comb) filter which reduces the sampling rate by 8 is used for the first stage. Two halfband filters and an FIR droop correction filter follow the CIC filter each reducing the sampling rate by two. Techniques to simultaneously achieve high performance and low power consumption are discussed in details. The minimum stopband attenuation of the decimator is more than -120 dB and the passband ripple is less than 0.0003 dB. The designed decimation filter is synthesized on standard cells of a 0.18 mum CMOS library. The designed and synthesized decimation filter contributes to a power consumption saving of 10.6% compared to the previous successful filters implemented on the same library. [C1319]

"Mobility controllable relays for conserving power in a network of mobile wireless sensors: Usage and issues"

We investigate the idea of using nodes with controllable mobility as intermediate relays for reducing the power consumption in a network of mobile wireless sensors. We present the relay deployment problem, which is to optimally position the relay nodes in the network so as to minimize the power consumed in communication. We discuss and evaluate a localized solution methodology that computes the optimal position and movement of the

relay nodes based on the information pertaining to the active data flows and the mobility patterns of the sensors in the network. Results from a preliminary simulation study indicate that deployment of relay nodes can result in considerable energy savings. We also outline some of the issues that need to be addressed in deploying such mobility-controllable relay nodes in a real network. [C1320]

"Energy-Efficient Dynamic Instruction Scheduling Logic through Instruction Grouping"

Dynamic instruction scheduling logic is quite complex and dissipates significant energy in microprocessors that support superscalar and out-of-order execution. We propose a novel microarchitectural technique to reduce the complexity and energy consumption of the dynamic instruction scheduling logic. The proposed method groups several instructions as a single issue unit and reduces the required number of ports and the size of the structure for dispatch, wakeup, select, and issue. The present paper describes the microarchitecture mechanisms and shows evaluation results for energy savings and performance. These results reveal that the proposed technique can greatly reduce energy with almost no performance degradation, compared to the conventional dynamic instruction scheduling logic [C1321]

"Application of Results of Ceramic Tiles Life Cycle Assessment due to Energy Savings and Environment Protection"

The production of ceramic tiles has significant influence to environment due to consumption of energy sources, raw material, emission and waste that emerges throughout the production. The life cycle assessment method is used to show and test the possibility of decreasing the influence of contemporary manufacturing process of ceramic tiles to environment. The ceramic tiles are produced in monofiring production technology as a part of integrated management system using international accepted standards for quality ISO 9001 and for management environment ISO 14001. The influence of life cycle phases of ceramic tiles and total influence to environment is determined by usage of EKO indicator 99. We tested the possibility of using data obtained by evaluation to management decisions about the decreasing the influence of production process as a life cycle phase through the decreasing of energy consumption and natural resources. The consumption of energy sources as gas and electricity was reduced by using the projects for increasing the power efficiency. The savings in gas consumption are achieved by building in unit for supplying with waste warm from oven to atomizer and electronic equipment for atomizer automatic control. The procedures for decreasing the electricity consumption are also used. [C1322]

"A Low Power Pulsed Edge-Triggered Latch for Survivor Memory Unit of Viterbi Decoder"

A low power pulsed edge-triggered latch based on the static edge-triggered latch (ETL) is presented for survivor memory (SMU) unit of Viterbi decoder for low power high speed wireless local area network (WLAN) applications. By reducing clock loading and transistor number, the proposed low swing static ETL has less clock loading, smaller cell area and power-delay product compared to traditional master-slave register. Moreover, a stage-reduced SMU is introduced later for saving both area and power consumption. The proposed low swing static ETL and stage-reduced SMU are designed and simulated in TSMC 0.13 um standard CMOS process, and the operating clock frequency is at 1GHz. [C1323]

"A Reduced Clock Delay Approach for High Performance Mesochronous Pipeline"

A mesochronous pipeline scheme is described in this paper. In a conventional pipeline scheme each pipeline stage operates on only one data set at a time. In the mesochronous scheme, pipeline stages operate on multiple data sets simultaneously. The clock period in conventional pipeline scheme is proportional to the maximum pipeline stage delay while in mesochronous pipelining, it is proportional to the maximum pipeline stage delay difference, which means higher clock speeds are possible and number of pipeline stages is significantly less. In mesochronous approach the clock distribution network is simple and load on it is less resulting in significant power savings. Also, the variations in supply current drawn by clock network is significantly less in mesochronous scheme, thus power supply noise (IR drop and Ldi/dt noise) is less. An 8times8-bit multiplier using carry-save adder technique has been implemented in conventional and mesochronous pipeline approach using TSMC 180 nm (drawn length 200 nm). The over all power dissipation in mesochronous approach is less than 50% of the power dissipation in conventional approach. In conventional approach, the power dissipation in clock network and pipeline registers is close to 80% of total power dissipation, while in mesochronous approach logic dissipates more power. [C1324]

"The Studies on Energy Control of Protocols inWireless Sensor Networks"

Energy control is the most important problem for wireless sensor networks, and the primary performance objectives are energy conservation and the design of an efficient energy strategy for prolonging the whole

networks' lifetime. As the applications of wireless sensor networks increase, the network protocols become more and more complex. But all the protocols have to aim chiefly to saving energy. The focus of the paper is to present the energy control strategy in energy-efficient MAC and routing protocols for wireless sensor networks. Then some open issues are provided for further studies for solving the problems of reducing the energy consumption in wireless sensor networks [C1325]

"Modified Hotspot Cache Architecture: A Low Energy Fast Cache for Embedded Processors"

The cache memory plays a crucial role in the performance of any processor. The cache memory (SRAM), especially the on chip cache, is 3-4 times faster than the main memory (DRAM). It can vastly improve the processor performance and speed. Also the cache consumes much less energy than the main memory. That leads to a huge power saving which is very important for embedded applications. In today's processors, although the cache memory reduces the energy consumption of the processor, however the energy consumption in the on-chip cache account to almost 40% of the total energy consumption of the processor. In this paper, we propose a cache architecture, for the instruction cache, that is a modification of the hotspot architecture. Our proposed architecture consists of a small filter cache in parallel with the hotspot cache, between the L1 cache and the main memory. The small filter cache is to hold the code that was not captured by the hotspot cache. We also propose a prediction mechanism to steer the memory access to either the hotspot cache, the filter cache, or the L1 cache. Our design has both a faster access time and less energy consumption compared to both the filter cache and the hotspot cache architectures. We use Mibench and Mediabench benchmarks, together with the simplescalar simulator in order to evaluate the performance of our proposed architecture and compares it with the filter cache and the hotspot cache architectures. The simulation results show that our design outperforms both the filter cache and the hotspot cache in both the average memory access time and the energy consumption [C1326]

"A Route-Oriented Sleep Approach in Wireless Sensor Network"

In resource-limited wireless sensor network, significant energy savings and longer life time of sensors can be achieved by having an effective energy management forcing sensors to sleep as long as they can. In this paper, we propose a route-oriented sleep (ROS) approach which allows sensors to sleep based on routing information and the level of network's activities. The scheme lets sensors switch their roles in the network according to the critical probability of the percolate theory without losing their sensing and communication connection coverage. This technique takes advantages of routing decisions and implements an effective sleep scheme at the network level, which allows some of sensors along the route path to sleep and wake up when they are a part of specific route. This produces balanced and low energy consumption for each node. ROS does not only achieve significant energy savings, but also reduces the communication interferences in the data transmissions, thus reduces the latency of data transmissions. The simulation results show that the proposed ROS approach significantly saves the sensor energy consumption more than 50% [C1327]

"A Novel Adaptive Energy Saving Mode in Ieee 802.16E System"

Minimizing energy consumption is crucial for portable wireless devices because they operate on a limited battery supply. In this paper, an adaptive energy consumption mechanism for the IEEE 802.16e broadband wireless access (BWA) network was proposed. A mobile subscriber station goes to sleep mode after negations with the base station and temporarily wake-up periodically for a short interval to check whether there is downlink traffic to it to decide whether it goes to awake mode or continues to be in the sleep-mode. The sleep interval is increased exponentially if there is no incoming or outgoing packet during that period. Moreover, the initial sleep interval and maximum interval is adaptive according to the traffic condition. We analytically model the sleep-mode scheme and compare the performance of our scheme with that of traditional energy saving mode by simulations. The result shows that our scheme not only reduces the power consumption dramatically, but also decreases the packet response time [C1328]

"Evaluation of stride permutation networks"

By exploiting the inherent parallelism in digital signal processing algorithms, significant savings in area and power consumption may be achieved. Completely parallel computation can lead to excessive area, thus mapping the algorithm onto reduced computational resources becomes beneficial. As a drawback, data interconnections become more complex and require storage in order to maintain computationally correct processing. We have proposed a systematic design methodology for managing data interconnections called stride permutations. These stride permutations are found in several algorithms, including fast Fourier transforms and Viterbi decoding. The proposed methodology leads to regular and scalable permutation networks which support power-of-two strides. In addition, the networks reach the lower bound in the number of registers indicating area-efficiency. In this

paper, the proposed networks are evaluated in terms of control, area, power consumption, and timing [C1329]

"A case-study on multimedia applications for the XiRisc reconfigurable processor"

Embedded real-time multimedia applications pose several challenges in order to satisfy increasing quality of service (QoS) and energy consumption constraints, that are hardly matched by the capabilities of general-purpose standard processors. Reconfigurable processors, coupling the flexibility of software-programmable devices with the computational efficiency of application specific architectures, represent an appealing trade-off for next generation devices in the digital signal processing application domain. In this paper, we present a benchmarking application for the XiRisc reconfigurable processor, based on a public release of the MPEG-2 video encoder. The introduction of the reconfigurable logic gives a 5times performance improvement and a 66% energy saving [C1330]

"Overview of Power-Efficient MAC and Routing Protocols for Wireless Sensor Networks"

Energy conservation is a primary concern in sensor networks. Firstly, we introduce the necessary of power saving in wireless sensor network. Then we analyze and summarize the main MAC protocols and routing protocols that are designed specially for energy conservation. Further, the methods for reducing energy consumption of node and increasing lifetime of networks are highlighted. Moreover, we make a comprehensive comparison between every protocol in performance of networks. Finally, we point out the future research directions and challenges that must be overcome on this topic [C1331]

"Jitter Characteristic in Resonant Clock Distribution"

This paper presents a detailed clock jitter characteristic analysis of a fully integrated 1.5-GHz resonant clocking fabricated in 130-nm CMOS, with 57% total clock power saving, compared to the conventional clocking implemented in the same test-chip. The jitter measurement result is in good agreement with the jitter analysis. Furthermore, a jitter-suppression technique based on injection locking phenomenon has been utilized to reduce the clock jitter and to solve the jitter peaking problem. Measurements show about 50% peak-to-peak clock jitter reduction from 28.4 ps to 14.5 ps after the activation of the injection locking [C1332]

"A-B Nodes Classification for Power Estimation"

In this paper, an optimization for the classical statistical power estimation method is proposed. This technique is applied to the individual nodes. The optimization is based on two observations. Firstly, a small percentage of both the nodes and the estimated power requires nearly a half of the total simulation time. On the other hand, the statistical method produces results with better accuracy than those specified by the user. This additional precision enables to reduce the run time for the slow convergence nodes with no loss of accuracy. A simple partitioning of the nodes into two groups, A and B, with normal and high computational cost respectively, leads to a modified stopping criterion with dramatic savings in the run time. [C1333]

"Alternative Vehicle Fuels Strategy in China: Well-to-Wheel Analysis on Energy Use and Greenhouse Gases Emission"

Oil consumption and import of China increase very quickly in recent years. Because of vehicle population growing in a tremendous speed, nearly 40% of oil has already used in transportation sector in today's China. Many kinds of alternative fuel vehicles are introduced, demonstrated and used in cities to reduce the traditional gasoline and diesel not only to reduce the regulated emissions, but also to improve the oil security of China. When the Kyoto Protocol became effective in last year, Chinese government and experts began to focus on greenhouse gas (GHG) emissions of alternative vehicle fuels. In order to comprehensively evaluating energy and global warming impact lead by production and utilization of alternative vehicle fuels in China, Well-to-Wheel analysis is used in this paper to quantitatively calculate energy use and GHG emissions of recovery, production, transportation and distribution, and end-use of compressed natural gas (CNG), liquefied petroleum gas (LPG), ethanol, methanol, dimethyl ether (DME) and Fischer-Tropsch diesel (FTD). The feedstock of ethanol includes corn and wheat. The energy use and GHG emissions of alternative vehicle fuels are compared with traditional gasoline and diesel. The results show that CNG and LPG is good choice from energy saving and GHG reduction in China. NG-based and coal-based methanol, DME and F-T diesel have lower lifecycle petroleum consumption than traditional gasoline and diesel, so that they may be an answer to Chinese oil security. The lifecycle total energy use, fossil energy use and GHG emissions of NG-based synthesized fuels are lower than coal-based fuels, but obviously higher than traditional gasoline and diesel, so that utilization of them will lead to potential pressure to China GHG reduction responsibility. The GHG emissions performance of China ethanol fuel is not as good as U.S. ethanol. The main reason is abuse of agriculture chemical in corn farming, especial the nitrogenous fertilizer, which is caused- great N20 emission [C1334]

"Adaptive, Transparent Frequency and Voltage Scaling of Communication Phases in MPI Programs"

Although users of high-performance computing are most interested in raw performance, both energy and power consumption have become critical concerns. Some microprocessors allow frequency and voltage scaling, which enables a system to reduce CPU performance and power when the CPU is not on the critical path. When properly directed, such dynamic frequency and voltage scaling can produce significant energy savings with little performance penalty. This paper presents an MPI runtime system that dynamically reduces CPU performance during communication phases in MPI programs. It dynamically identifies such phases and, without profiling or training, selects the CPU frequency in order to minimize energy-delay product. All analysis and subsequent frequency and voltage scaling is within MPI and so is entirely transparent to the application. This means that the large number of existing MPI programs, as well as new ones being developed, can use our system without modification. Results show that the average reduction in energy-delay product over the NAS benchmark suite is 10%-the average energy reduction is 12% while the average execution time increase is only 2.1% [C1335]

"A Low-Power 8-bit Folding A/D Converter with Improved Accuracy"

In this paper, an accuracy improving method for calibration of mismatch-induced errors in folding A/D converter is presented. With dynamic auto-zero calibration for the folder, the transistor size of folding differential input pairs can be reduced considerably while keeping integral nonlinearity (INL) low. Using this technique, an 8-bit folding A/D converter is designed and simulated in MATLAB. Because of the calibration, conventional preamplifiers and offset averaging network before the folders are removed, saving a large power consumption and chip area. Results are demonstrated, showing the improved accuracy and the good agreement with the theoretical prediction [C1336]

"Predictive Dynamic Power Management Policy with Consideration of Outlying Data"

Reducing energy consumption has emerged as one of the key issues in designing electronic system. This paper proposes a predictive dynamic power management policy. The policy uses AR model to predict the upcoming idle period and introduces a mechanism that processes the outlying data of idle periods to improve the prediction accuracy. Simulation results show that the proposed policy achieves a high degree of power saving and good stability [C1337]

"A low complexity, low power, programmable QRS detector based on wavelet transform for Implantable Pacemaker IC"

This paper presents a QRS detector operating in multi-mode with low complexity, power saving consumption for implantable pacemaker IC. The complexity of detector is optimized after testing dynamic range of internal signals. Correspondingly, static power consumption is reduced significantly. The dynamic power consumption is saved by using down-sampling rate structure and turning off de- active filter banks bases on noise estimation. This QRS detector is evaluated with MIT-BIH Arrhythmia database archives >99% detection ratio. A soft IP core is prototyped on FPGA and synthesized by Samsung 0.18um standard library. [C1338]

"Geometric Tiling for Reducing Power Consumption in Structured Matrix Operations"

This work focuses on reducing power consumption while maintaining the efficiency and accuracy of matrix computations using both algorithmic and architectural means. We transform the algorithms, in adaptation to application specifics, to translate the matrix structures into power saving potential via geometric tiling. Instead of using blind tiling, we index and partition matrix elements according to the underlying geometry to claim a better estimate and control of numerical range within and across geometric tiles, which can then be exploited for power saving. [C1339]

"Calculation and Test for Voltage Regulation Power-saving"

Power transmission voltage is higher than the rated voltage according to the standard, in order to avoid the voltage drop because of the power loss and the overload. However when the load in the power network is light, the excessively high electrical network voltage may cause the load equipment to give off heat, and reduce service life. At the same time the power consumption and electrical bill disbursement increase. So adjusting the voltage for steady power supply and saving power is an important content of improving electrical network performance, ensuring power supply quality, and reducing waste. The basic structure and principle of saturable controllable reactor is studied in this paper. To adjust and stabilize the voltage of power system by a new type saturable controllable reactor is advanced. According to the characteristic of loads, the voltage is adjusted to

stabilize the power supply and saving power [C1340]

"Reducing Tag Activities for Power Efficiency in I-cache Memory"

As the clock frequency and cache size increase in modern microprocessors, the excessive power consumption in cache memory attracts more and more attention and research interest. This paper proposes a software and hardware co-design method to reduce the tag activities for power efficiency with little performance penalty. Using the run-time profile data, we trace the object code dynamically and extract the loops, subroutines, branches etc., and predict the point of time when tag checks are not needed for instruction fetching from I-cache memory. With support from simple logic circuits, the tags could be disabled and enabled timely to save power. The overhead of power consumption in the tag controller is negligible due to its simplicity and the low frequency of tag switches. Our experimental results using a subset of SPEC 2000 benchmarks showed that this strategy could reduce 20.6% of energy consumption in a 16 K I-cache on average with only 0.13% of performance loss. [C1341]

"Low-Power Content Addressable Memory Using 2N-2N2P Circuits"

In this paper, we present a novel low power adiabatic content-addressable memory (CAM). It consists of a CAM-cell array, address decoders, read/write control circuits, sense amplifiers, read/write drivers and compare circuits. An AC power supply is used for driving the match-lines to reduce the energy consumption in adiabatic manner. The rest circuits employ 2N-2N2P circuits to recover the charge of node capacitances on address decoders, bit-lines and word-lines. The power consumption of compare operation is significantly reduced because the energy transferred to the capacitance buses is mostly recovered. The energy and functional simulations of a 16 x 16 CAM are performed. SPICE simulations indicate that the proposed CAM attains energy savings of 60% to 80% as compared to the conventional CMOS implementation for clock rates ranging from 25 to 200 Mhz. [C1342]

"Combining Genetic Algorithms Based Task Mapping and Optimal Voltage Selection for Energy-Efficient Distributed System Synthesis"

Energy consumption has become one of dominant design concerns in distributed embedded systems. Dynamic voltage scaling (DVS) techniques have been proved to be quite effective in reducing both dynamic and static power consumption simultaneously. Thus, integrating processing elements (PEs) supporting DVS techniques into distributed embedded systems synthesis becomes an imperative way to make an energy-efficient design budget. In this paper, we propose a synthesis framework, which integrates task mapping, scheduling and voltage selection together to minimize energy consumption of distributed systems. Genetic algorithms based task mapping are deployed to do task mapping in the outer loop, which can maximize the energy saving possibilities. A nonlinear programming based optimal voltage selection engine is then used in the inner loop. Unlike previous approaches, this combination is the first time to be implemented, and relevant experiment results show that, comparing to separate synthesis flows, up to 40% more energy savings are achieved [C1343]

"Cross-Layer Analysis of Error Control in Wireless Sensor Networks"

Severe energy constraints and hence the low power communication requirements amplify the significance of the energy efficient and preferably cross-layer error control mechanisms in wireless sensor networks (WSN). In this paper, a cross-layer methodology for the analysis of error control schemes in WSNs is presented such that the effects of multi-hop routing and the broadcast nature of the wireless channel are investigated. More specifically, the cross-layer effects of routing, medium access and physical layers are considered. This analysis enables a comprehensive comparison of forward error correction (FEC) and automatic repeat request (ARQ) in WSNs. FEC schemes improve the error resiliency compared to ARQ. In a multi-hop network, this improvement can be exploited by reducing the transmit power (transmit power control) or by constructing longer hops (hop length extension), which can be achieved through channel-aware routing protocols. The results of our analysis reveal that for certain FEC codes, the hop length extension decreases both the energy consumption and the end-to-end latency subject to a target PER compared to ARQ. Thus, FEC codes can be regarded as an important candidate for delay sensitive traffic in WSNs. On the other hand, transmit power control results in significant savings in energy consumption at the cost of increased latency. Moreover, the cases where ARQ outperforms FEC codes are indicated for various end-to-end distance and target PER values [C1344]

"Circular-Layer Algorithm for Ad Hoc Sensor Networks to Balance Power Consumption"

In senor networks, the data traffic from the sensors are directional towards a data sink and are therefore uneven. The areas nearer the data sink experience higher data traffic and will run out of energy sooner. Circular-layer geometry takes into account the radial data traffic towards the data sink. We may construct an algorithm to divide the network into equal-area circular-layers, which are analogous to the square design in geographical

adaptive fidelity (GAF). However, the circular-layer geometry alone has not taken into account the uneven data traffic. This paper proposes a circular-layer algorithm that schedules the sensors into active and sleep states in such a way as to evenly distribute the power consumption throughout the sensor networks. We divide the network into circular layers with the data sink at the center. The algorithm equalizes the lifetime time of all layers so that the nodes near the data sink will not run out of energy sooner. Energy is also wasted in reactive routing where the sensors flood the network with omni-directional route discovery messages to find a suitable route towards the data sink. This algorithm reduces such flooding by directing the route request messages towards the data sink, resulting in more energy saving. The circular-layer geometry alone is serving to save energy. In addition, balancing the power consumption throughout the network yields an additional lifetime extension of 21% in our simulation results of a four-layer scenario [C1345]

"A Power-saving Scheme for IEEE 802.11 Ad hoc Networks"

In the wireless local area networks (WLANs), the terminals are often powered by battery, so the power-saving performance of the wireless network card is a very important issue. For IEEE 802.11 ad hoc networks, a power-saving scheme is presented in medium access control (MAC) layer to reduce the power consumption by allowing the nodes enter into the sleep mode, but the scheme is based on time-drive scheme (TDS) whose power-saving efficiency becomes lower and lower with the network load increasing. This paper presented a novel energy-saving mechanism, called as hybrid-drive scheme (HDS), which introduces into a message-drive scheme (MDS) and combines MDS with the conventional TDS. The MDS could obtain high efficiency when the load is heavy; meanwhile the TDS has high efficiency when the network load is small. The analysis shows that the proposed HDS could obtain high energy-efficiency whether the network load is light or heavy and have higher energy-saving efficiency than conventional scheme in the IEEE 802.11 standard [C1346]

"Scheduling Data Delivery in Heterogeneous Wireless Sensor Networks"

In this paper we present a proxy-level scheduler that can significantly improve QoS in heterogeneous wireless sensor networks while at the same time reducing the overall power consumption. Our scheduler is transparent to both applications and MAC in order to take the advantage of the standard off-the-shelf components. The proposed scheduling reduces collisions through a generalized TDMA implementation, and thus improves throughput and QoS, by activating only a subset of stations at a time. Power savings are achieved by scheduling transfer of larger bursts of IP packets followed by longer idle periods during which node's radio can either enter sleep or be turned off. Our simulation and measurement results show significant power savings with an improvement in QoS. On average we get 18% of saturation throughput enhancement for real traffic and 79% of power reduction in a highly loaded network [C1347]

"A security-energy trade-off for authentic aggregation in sensor networks"

To reduce energy consumption, aggregation takes place in a wireless sensor network. All measured data is collected and preprocessed multiple times on its way towards a data sink, e.g., a base station. However, aggregation implies new challenges to security: as the sink Anally receives aggregated data, it is difficult to verify not only the aggregate's correctness, but also the origin of the data the aggregate was computed from. In the presence of an attacker in the network, data transmissions and aggregation could have maliciously been modified. Yet, it turns out that in-network aggregation and data authenticity are contradictory communication properties. This research examines the possibility of finding a trade-off between security (authenticity) and energy-savings (aggregation). If the user is willing to accept data's authenticity with ples100% probability, he can still save large amounts of energy compared to authentic communication without aggregation. [C1348]

"Sensor-Enhanced Mobility Prediction for Energy-Efficient Localization"

Energy efficiency and positional accuracy are often contradictive goals. We propose to decrease power consumption without sacrificing significant accuracy by developing an energy-aware localization that adapts the sampling rate to target's mobility level. In this paper, an energy-aware adaptive localization system based on signal strength fingerprinting is designed, implemented, and evaluated. Promising to satisfy an application's requirements on positional accuracy, our system tries to adapt its sampling rate to reduce its energy consumption. The contribution of this paper is three-fold. (1) We have developed a model to predict the positional error of a real working positioning engine under different mobility levels of mobile targets, estimation error from the positioning engine, processing and networking delay in the location infrastructure, and sampling rate of location information. (2) In a real test environment, our energy-saving method solves the mobility estimation error problem by utilizing additional sensors on mobile targets. The result is that we can improve the prediction accuracy by as much as 37.01%. (3) We implemented our energy-saving methods inside a working localization infrastructure and conducted performance evaluation in a real office environment. Our performance

results show as much as 49.76 % reduction in power consumption [C1349]

"Genetic Algorithm Based Idle Length Prediction Scheme for Dynamic Power Management"

Reducing energy consumption has become one of the most important challenges in designing computing systems. Dynamic power management policies exploit components' idle periods to save energy. If one idle period of some component is long enough, the component can be put into low power state during this period in order to reduce energy consumption. Many dynamic power management policies are based on predicting lengths of components' future idle periods. The more accurate the prediction is, the more efficient the policy is. This paper proposes a novel idea of using genetic algorithm to predict lengths of future idle periods. We take K adjacent idle periods and active periods as a load-gene and define some kinds of relationships between adjacent load-genes, then use genetic algorithm to predict future load-genes that most accords with the relationships. Experimental results show that the proposed scheme is more efficient than the exponential-average approach [C1350]

"Design and implementation of a reconfigurable heterogeneous multiprocessor SoC"

This paper introduces a novel heterogeneous shared memory multiprocessor architecture based on a reconfigurable processor and a standard RISC processor. The work aims at increasing further the computational density of a reconfigurable device by the integration of the reconfigurable hardware into a heterogeneous multi-core architecture. Though a RISC processor has a lower inner computational density than a reconfigurable processor, this work demonstrates that coupling a reconfigurable core to a RISC core leads to a computational density increase by a factor of up to 1.7times on signal processing applications. Moreover, this approach also achieves up to 37% energy savings on the same applications. The multi-core SoC architecture was implemented in 0.13mum technology, achieving a 166MHz clock frequency with an average 340mW power consumption [C1351]

"Minimizing Power Consumption of the DVB-H Receiver"

Although the DVB-T transmission system has proven its ability to serve fixed, portable and mobile terminals, handheld terminals (defined as small and lightweight battery powered devices) require specific set of features from the transmission system serving them. Reduced average power consumption of the receiver is one of them. This paper contains some methods specific to DVB-H transmission system used to achieve this goal [C1352]

"An on-board Monitoring System for Electrical Railway Traction Systems"

Energy saving in electrical railway traction systems has gained more and more relevance in the last years. As a matter of fact, the need for increasing speed in order to provide better quality services, implies an increase in energy consumption, and in operational costs. To keep the latter at the lowest level possible, it is possible to adapt the train's operating conditions according to appropriate rules based on measurements of characteristic train's and system's quantities. In this way, it is possible to have thorough information about train's course, and then take decisions in order to improve service and reduce consumptions at the same time. In the following is presented an on-board monitoring system that measures electrical quantities of the train and sends acquired data to a control station through network connection. The application of such system to the optimization of the train course protocol is also presented [C1353]

"Cache Miss Clustering for Banked Memory Systems"

One of the previously-proposed techniques for reducing memory energy consumption is memory banking. The idea is to divide the memory space into multiple banks and place currently unused (idle) banks into a low-power operating mode. The prior studies-both hardware and software domain-in memory energy optimization via low-power modes do not take the data cache behavior explicitly into account. As a consequence, the energy savings achieved by these techniques can be unpredictable due to dynamic cache behavior at runtime. The main contribution of this paper is a compiler optimization, called the bank-aware cache miss clustering, that increases idle durations of memory banks, and as a result, enables better exploitation of available low-power capabilities supported by the memory system. This is because clustering cache misses helps to cluster cache hits as well, and this in turn increases bank idleness. We implemented our cache miss clustering approach within a compilation framework and tested it using seven array-intensive application codes. Our experiments show that cache miss clustering saves significant memory energy as a result of increased idle periods of memory banks [C1354]

"Energy Management for Real-Time Embedded Systems with Reliability Requirements"

With the continued scaling of CMOS technologies and reduced design margins, the reliability concerns induced by transient faults have become prominent. Moreover, the popular energy management technique dynamic voltage and frequency scaling (DVFS) has been shown to have direct and negative effects on reliability. In this work, for a set of real-time tasks, we focus on the slack allocation problem to minimize their energy consumption while preserving the overall system reliability. Building on our previous findings for a single real-time application where a recovery task was used to preserve reliability, we identify the problem of reliability-aware energy management for multiple tasks as NP-hard and propose two polynomial-time heuristic schemes. We also investigate the effects of on-chip/off-chip workload decomposition on energy management, by considering a generalized power model. Simulation results show that ordinary energy management schemes could lead to drastically decreased system reliability, while the proposed reliability-aware heuristic schemes are able to preserve the system reliability and obtain significant energy savings at the same time [C1355]

"Formal Model of Data Reuse Analysis for Hierarchical Memory Organizations"

In real-time data-dominated communication and multimedia processing applications, due to the manipulation of large sets of data, a multi-layer memory hierarchy is used to enhance the system performance and also to reduce the energy consumption. Savings of dynamic energy can be obtained by accessing frequently used data from smaller memories rather than from large background memories. The optimization of the hierarchical memory architecture implies the addition of layers of smaller memories to which heavily used data can be copied. This paper presents a formal model for data reuse analysis which identifies those parts of arrays more intensely accessed, taking also into account the relative lifetimes of the signals. Tested on a two-layer memory hierarchy, this model led to savings in the dynamic energy from 40% to over 70% relative to the energy used in the case of a flat memory design [C1356]

"The Analysis and Handling of A 35kV Transformer Fault"

Based on a typical fault occurring on a 35 kV transformer, we synthesized three specialties in this this paper: the high voltage test, the relay protection and the oiling testing, and carried on the analysis from the different angle to the identical fault, thus obtained the effective means to handle this kind of trouble. Also this paper proposed how to prevent such accident occurring and safeguard the secure and steady operation of electrical equipment, and to improve energy saving and energy consumption reducing of equipment. [C1357]

"Scheduler Optimization by Exploring Wakeup Locality"

In a high-performance superscalar processor, the instruction scheduler often comes with poor scalability and high complexity due to the expensive instruction wakeup operation. Using detailed simulation-based analyses, we find that the wakeup distances between two dependent instructions are short. By exploiting this wakeup locality, an effective wakeup design is proposed to improve the speed, power, and scalability of the dynamic scheduler. By limiting the wakeup range of instructions, load capacitance and match activities on the scheduler's critical path can be reduced. The architectural level simulation and circuit-level timing analyses show that the proposed design saves 65-76% of the power consumption, reduces 44-78% in the wakeup latency with negligible (less than 1%) performance degradation. The results also show that the proposed design is excellent in scalability [C1358]

"A Low-Power Implementation of 3D Graphics System for Embedded Mobile Systems"

For mobile 3D graphics systems, even though performance requirements are met, an efficient power management is even more important for battery-powered mobile devices since they require a large number of arithmetic operations as well as a high frequency of memory accesses. According to the analysis of the power consumption of mobile 3D graphics pipelines and the slacks across the pipeline stages, we describe intra-frame and inter-frame DVS low-power techniques reducing the power consumption of mobile devices based on a variable voltage processor. Our implementation on a PDA development board shows that the proposed DVS techniques achieve an energy saving of up to 46% over a non-DVS implementation [C1359]

"PSBP: Power Saving Backoff Prediction in IEEE802.11"

Batteries are a primary resource in wireless networks for many mobile devices. Minimizing energy consumption without affecting communication activities is crucial to prolong the lifetime and improve the robustness of the wireless connection. One effective way to reduce energy consumption is to put the entire, or part of the system in a low power state whenever possible. A power saving protocol that uses network information to estimate the congestion level, allows stations to predict the time they will wait before accessing the channel in IEEE802.11. By estimating the time a station will wait to access the channel, the station does not need to stay awake sampling the medium and instead can enter a low power sleep mode for a portion of this time, for particular

usage scenarios. Adopting this scheme allows considerable power savings without any adverse effect on network throughput [C1360]

"Transport Protocol Behavior and Energy-Saving Potential"

We investigate the energy-saving potential of transport protocols. We seek an answer to strategic issues of maximizing energy and bandwidth exploitation, without damaging the dynamics of multiple-flow equilibrium. We claim that (i) an energy-saving strategy of the transport level needs to be associated with some energy potential index which, unlike energy expenditure, is not device-specific and (ii) system-wise an energy-efficient system of flows is not always a better choice: we show that a less energy-efficient system may be more reliable in terms of packet multiplexing and, in turn, may reduce the probability that some flows may expend their energy with zero gain. We present results using a real testbed [C1361]

"Energy-efficient Interleaving for Error Recovery in Broadcast Networks"

We analyze the performance of MAC-layer Reed-Solomon error recovery in the CDMA2000 1xEV-DO broadcast and multicast services (BCMCS) environment, with respect to the size of the error control block (ECB) and the air-channel condition, and establish the relationship between ECB size, error-recovery capacity and energy consumption. Real-time traffic, such as voice and video streaming, is very sensitive to delay, but can stand a certain level of packet loss. We therefore propose an energy-efficient size of the ECB to reduce the average energy consumption during error recovery while minimizing the reduction in service quality for real-time multimedia applications. Extensive simulation results suggest that a significant amount of energy can be saved with negligible performance degradation by selecting the appropriate ECB size for the bit error-rate of the forward traffic channel, instead of always choosing the largest possible ECB, with the sole aim of increasing error recovery performance [C1362]

"Joint Design-Time and Post-Silicon Minimization of Parametric Yield Loss using Adjustable Robust Optimization"

Parametric yield loss due to variability can be effectively reduced by both design-time optimization strategies and by adjusting circuit parameters to the realizations of variable parameters. The two levels of tuning operate within a single variability budget, and because their effectiveness depends on the magnitude and the spatial structure of variability their joint co-optimization is required. In this paper we develop a formal optimization algorithm for such co-optimization and link it to the control and measurement overhead via the formal notions of measurement and control complexity. We describe an optimization strategy that unifies design-time gate-level sizing and post-silicon adaptation using adaptive body bias at the chip level. The statistical formulation utilizes adjustable robust linear programming to derive the optimal policy for assigning body bias once the uncertain variables, such as gate length and threshold voltage, are known. Computational tractability is achieved by restricting optimal body bias selection policy to be an affine function of uncertain variables. We demonstrate good run-time and show that 5-35% savings in leakage power across the benchmark circuits are possible. Dependence of results on measurement and control complexity is studied and points of diminishing returns for both metrics are identified [C1363]

"Energy Conscious Simultaneous Voltage Scaling and On-chip Communication Bus Synthesis"

Due to the ever increasing trend of system complexity and technology scaling, synthesizing on-chip communication architecture appears to be a challenging task for the system designers. The traditional approaches are mostly based on the simulation of an entire system. However, the resulting architecture may not fulfil the requirements such as the performance, energy, size etc. and the computational cost of simulation based techniques is infeasible when exploring a large design space. This paper presents a simultaneous on-chip communication bus synthesis and voltage scaling approach, which is modeled in NLP (nonlinear programming) and finds an energy efficient minimum number of bus(es) and an optimal size of bus width by simultaneously performing resource selection, scheduling, binding and voltage scaling of an on-chip bus. The voltages (supply and body bias) are scaled to reduce the total energy consumption of a bus by exploiting the slack of each on-chip module. The experimental results conducted on real-life examples, demonstrate the synthesis of an energy efficient communication bus with total energy saving up to 57.1% by scaling its supply and body bias voltages [C1364]

"Energy-Effcient Scheduling for Autonomous Mobile Robots"

An autonomous robot has to sense its environment and prevent collision. Stereovision is a widely used technology for distance calculation and collision prevention. While a robot is moving, it has to detect an obstacle before a collision. This result in a real-time constraint and it may be adjusted by slowing down the motor. Since

mobile robots usually carry limited energy, energy conservation is crucial. Stereovision requires substantial amounts of computation and causes much energy consumption. This paper presents a new approach for energy conservation for a mobile robot. We consider the energy consumed by both the on-board processor and the motor. Our method controls both the processor's frequency and the motor's speed to reduce energy while preventing collision. We formulate the problem as non-linear optimization and demonstrate that more energy can be saved by adjusting both the frequency and the speed simultaneously [C1365]

"Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design"

For the most recent CMOS feature sizes (e.g., 90nm and 65nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. ITRS reports that leakage power dissipation may come to dominate total power consumption as presented in ITRS by Semiconductor Industry Association, 2005. We propose a novel approach, named "sleepy keeper," which reduces leakage current while saving exact logic state. Sleepy keeper uses traditional sleep transistors plus two additional transistors-driven by a gate's already calculated output-to save state during sleep mode. Dual Vthvalues can be applied to sleepy keeper in order to dramatically reduce subthreshold leakage current. In short, like the sleepy stack approach, sleepy keeper achieves leakage power reduction equivalent to the sleep and zigzag approaches but with the advantage of maintaining exact logic state (instead of destroying the logic state when sleep mode is entered). Based on experiments with a 4-bit adder circuit, sleepy keeper approach achieves up to 49% less delay and 49% less area than the sleepy stack approach. Unfortunately, sleepy keeper causes additional dynamic power consumption, approximately 15% more than the base case (no sleep transistors used at all). However, for applications spending the vast majority of time in sleep or standby mode while also requiring low area, high performance and maintenance of exact logic state, the sleepy keeper approach provides a new weapon in a VLSI designer's arsenal [C1366]

"Checkerboard-Type Filtering for a Low-Power Gradient-Based Optical Flow Estimation System"

In this paper, we propose a checkerboard-type filtering algorithm for a low-power gradient-based optical flow estimation (OFE) system. A gradient-based optical flow algorithm estimates optical flow field using gradient values of images. The conventional filtering stages in OFE that are used to calculate gradient values are composed of a 3D prefiltering/smoothing stage and three 1D parallel derivative filtering stages. To reduce power consumption using pixel-wise parallel processing in analog spatial transform imager, we suggest a checkerboard-type filtering based on convolution theorem and common data sharing. We describe the equivalence of our filtering scheme with the conventional smoothing and derivative filtering schemes and present some comparison in terms of the number of operations and power savings. We show that our approach is promising for low-power implementation of gradient-based OFE system under proper data scanning direction [C1367]

"Performance Analysis of Integral Receiver/Dryer Condenser for Automobile"

The important problems from the point of view of preventing global warming are to save the power consumption of automotive air-conditioning systems and reduce the refrigerant amount used. To achieve those requirements, integral receiver/ dryer(R/D) condensers were developed recently. Typical integral condensers have extra headers that play the role of R/D. Except an extra header and somewhat complex tube array resulting from the extra header, the most integral R/D condensers have almost the same specification as common condensers. When integral R/D condensers are applied, it is known that the refrigerating effect increases, resulting from the increase of subcooling degree in condenser, and the refrigerant amount used saves. In spite of several merits, integral condensers have not been used a lot. That is why there is an uncertainty in performance, using those condensers. The objective of this study is to theoretically optimize the tube array (tube per pass) in an integral R/D condenser that is really being applied to some vehicles. Through computer simulation, we could see that the tube array, 14-6-3-5-3-4, in the same condenser was the best, comparing heat release rate, pressure drop, etc. to the real array, 17-5-3-3-2-5. It should be noted that the optimization is based on the condenser performance only. [C1368]

"Main Memory Energy Optimization for Multi-Task Applications"

In order to minimize the energy consumed by the main memory in embedded systems, several solutions are proposed. An architectural solution is particularly effective in reducing this memory consumption part. It consists of multi-banking the addressing space instead of a monolithic memory. The main advantage in this approach is the capability of independently setting banks in low power modes when they are not accessed, such that only the accessed bank is maintained in active mode. In this paper, the authors investigate how the power management capability built into modern DRAM devices can be handled for real-time and multitasking applications. The authors aim to find, at system level design, both an efficient allocation of application's tasks to

memory banks, and the memory configuration that lessen the energy consumption: number of banks and the size of each bank. Experiments show an energy savings of 15% for the considered two benchmarks [C1369]

"Efficient Power Management Scheme Considering Inter-User QoS in Wireless LAN"

In wireless LAN, power saving is the essential issue to the node since the node has the limited battery. Hence, the nodes can use the Power Saving (PS) mode unless transmitting or receiving packet exists for the certain period. For the PS node to receive the buffered packet in Access Point (AP), the PS nodes periodically check the Traffic Indication Map (TIM) field in the beacon frame that contains the information about buffered packet. If the buffered packet exists, they must transmit the PS. POLL to the AP. The AP transmits the buffered packet to the node that succeeds to transmit the PS_POLL. However, when the node transmits the PS-POLL, the transmission order is determined without any priority. Therefore, we propose the efficient power management scheme to support inter-user QoS and reduce the power consumption in wireless LAN. In the proposed scheme, the node with high priority transmits PS_ POLL earlier than that with low priority, so the node with high priority receives the buffered packet faster than that with low priority, and reduces the power consumption by converting the mode from Active Mode (AM) to Power Saving (PS) for remaining beacon interval (BI). Through the analysis and simulation, we show that the proposed scheme reduces power consumption and guarantees inter-user QoS compared to conventional scheme. [C1370]

"Mobility Support for Cooperative Wireless Networks"

In a cooperative network, by combining multiple copies of the same packet that are received either simultaneously (i.e., same time-slot) or non-simultaneously (i.e., different time-slot), the aggregate power level of the cooperatively transmitting set, required to achieve reliable reception at the receiver node, can be considerably lowered. This approach is especially advantageous for networks, where the number of nodes in the network, the network density, or the potential for wireless broadcasting advantage is high. In such networks, required transmit energy can be considerably reduced by routing packets over cooperative paths. Since the success of cooperation strictly depends on the selection of the appropriate power levels for each cooperating node, cooperative routing becomes difficult in networks where the nodes are mobile. In such networks, we need to select paths that can maximize the energy savings averaged over the connection time rather than the ones that only maximize savings at the current time. For this reason, we need to design routing protocols that takes into account the mobility characteristics within the network. In this paper, we propose a cooperative routing protocol that can improve the reliability level in the network against mobility variations. [C1371]

"Adaptive Complexity Equalization for the Downlink in WCDMA Systems"

We consider the issue of terminal reconfigurability in the downlink of WCDMA. For the purpose of optimizing power consumption in mobile terminals, we propose an adaptive- complexity equalization algorithm, which adapts the equalization length to the environment. A simple approach in WCDMA systems consists of computing the equalizer coefficients in frequency domain, and carry out channel equalization in time domain. The equalizer can be easily computed in frequency domain from channel estimates, which are generally obtained through pilot symbols. In our work, we decouple the task of adaptive complexity equalization in two parallel operations: variable length equalization and equalization length control. We propose a practical scheme to reduce equalization complexity by prewindowing in frequency domain and performing IFFT of variable length. An element of length control monitors the equalizer coefficients, updating the equalizer length at each stage. Both simulation and experimental results in outdoor-to- indoor scenarios show good performance and significant power savings with respect to full length equalization. [C1372]

"An Adaptive Discontinuous Reception Mechanism Based on Extended Paging Indicator for Power Saving in UMTS"

In this paper, we propose the ADRX (adaptive discontinuous reception) mechanism with the EPI (extended paging indicator) for power saving in the UMTS (universal mobile telecommunications system). Regardless of various traffic patterns and network situations, the conventional FDRX (Fixed DRX) mechanism currently specified by 3GPP (third generation partnership projects) employs only fixed DRX period with a given DRX cycle length of the same length in which each UE (User Equipment) is to have one paging occasion with the uniquely allocated PI. However, improvement of power saving performance cannot be expected since this FDRX does not support longer DRX periods to save more power consumed in the UE for intermittent data packets. In the proposed ADRX mechanism, to solve this problem and efficiently reduce the power consumption, DRX period is easily controlled by the EPI which is decided by Node B considering the current traffic situation. In addition to its original functions to indicate paging messages, the proposed EPI also includes four extended functions; preservation, increase, decrease, and reset of the DRX periods. Simulation results reveal that the proposed

ADRX mechanism achieves remarkable improvement of power saving performance as compared to the conventional FDRX mechanism. Furthermore, it is also observed that the proposed ADRX based on the EPI has a trade-off relationship between power saving performance and packet transmission reliability. [C1373]

"Improvement of Slots Utilization with a Stealing-TDMA Protocol for Ad Hoc Network"

Using time division multiple access (TDMA) scheme to access the shared medium in communication systems has been well studied in literature. The major problems of TDMA system are how to efficiently schedule the time slots for nodes so that fit their actual needs of bandwidth and how to allocate an adequate time period for data transmissions according to the varied amount of traffic by time. Recently many TDMA schemes had been proposed such as the topology-unaware TDMA method, which uses the probabilistic method to access medium, to enhance the performance of TDMA system. However, this method would lead to heavy collisions while the traffic load and the neighbors are increasing accordingly. To tackle this drawback, we propose a stealing-TDMA (sTDMA) protocol using ACK mechanism to reserve time slots for solving collision problems. The performance analysis shows the significant improvements in reducing collision probability and power saving. [C1374]

"Energy-efficient rate adaptation MAC protocol for ad hoc wireless networks"

Resource constraints in ad hoc wireless networks require that they are energy efficient during both transmission and rate adaptation. In this paper, we propose a novel energy-efficient rate adaptation protocol that selects modulation schemes online to maximize throughput based on channel state while saving energy. This protocol uses the distributed power control (DPC) algorithm (M. Zawodniok et al., 2004) to accurately determine the necessary transmission power and to reduce the energy consumption. Additionally, the transmission rate is altered using energy efficiency as a constraint to meet the required throughput, which is estimated with queue fill ratio. Moreover, back-off scheme is incorporated to prevent energy wastage and to avoid retransmissions in the event of congestion. The back-off scheme employs backpressure mechanism to emulate congestion control. Consequently, the nodes will conserve energy when the traffic is low, offer higher throughput when needed and save energy during congestion by limiting transmission. [C1375]

"Optimal resource allocation and leaky bucket based power control for CBR MIMO systems"

Supporting high-quality video transmission across wireless networks demands not only high but also constant bit rate (CBR). In order to provide a CBR channel, large modifications in transmitting power requirement would normally be necessary to inverse extremely high variation in channel fading. However, with a multiple input and multiple output (MIMO) system, sub-channel diversity can "smooth out" aggregate channel fluctuation, making it possible to support a CBR channel with efficient power control. We have devised an optimal antenna transmitting power and bits-per-symbol allocation algorithm that can reduce significantly, the total power consumption required to maintain CBR channels. We also utilize a secondary power control based on leaky bucket paradigm for smooth battery drain and to make peak power utilization to within system requirements. Simulation results reveal that under practical power fluctuation constraints, the scheme can achieve power savings of up to 10 dB with a 4Ч4 antenna system. [C1376]

"Energy-efficient task scheduling for wireless sensor nodes with multiple sensing units"

It is critical to design efficient power management and scheduling techniques for wireless sensor nodes that operate with limited battery power. The design of these techniques becomes more challenging especially when each sensor node has multiple sensing units and the occurrences of their events of interest are not known in advance. This paper proposes an event-driven task scheduling algorithm, called MSUS (multiple sensing unit scheduling). MSUS determines the best power state based on the timing and priority requirements, the event-misses, and the existing and the predicted future tasks for all the sensing units of a sensor node with multiple sensing units. Simulation results show that MSUS leads energy savings up to 49% and reduces event misses by 56% when compared to the greedy technique that puts the sensor node components into the lowest power consumption level whenever there is no available task to process. [C1377]

"Area and power efficient trellis computational blocks in 0.13µm CMOS"

Improved add-compare-select and branch metric units are presented to reduce the complexity in the implementation of trellis-based decoding architectures. These units use a complementary property of the best rate 1/2 convolutional codes to reduce both area requirements and power consumption in a silicon implementation with no loss in decoding performance. For a 0.13µm CMOS process, synthesized computational blocks for decoders that can process codes from memory 2 up to 7 show up to 17% savings in both cell area and power consumption. [C1378]

"High-density wireless sensor networks: a new clustering approach for prediction-based monitoring"

We propose a new cluster-based approach that simplifies prediction-based monitoring for homogeneous, high-density wireless sensor networks composed of a large number of small, power-restricted nodes. Prediction-based monitoring can increase the autonomous lifetime of the network by reducing communication. In our clustering approach, the cluster-heads spatio-temporally correlate and predict the measurements of the cluster-members by executing their prediction model. Routing is only done by the gateway nodes at the circumference of the clusters while the nongateway nodes, which are positioned between the cluster-heads and their gateway nodes, are allowed to turn off their radio communication as long as their measurements satisfy the predictions of their cluster-head. Turning off radio communication results in high energy savings and can greatly improve system lifetime. Our main contribution is the description of this clustering approach while the prediction models are beyond the scope of this paper. [C1379]

"Prediction-based object tracking algorithm with load balance for wireless sensor networks"

Power efficiency is one of the major concerns of wireless sensor networks applications. Most existing power efficient routing algorithms for wireless sensor networks concentrates on finding efficient ways to forward data. Yet not much work has been done on collecting local data, tracking the detected objects, predicting the future motion, and then generating the data report. This paper presents the effect of object tracking prediction on power saving for wireless sensor networks. An object tracking prediction method, i.e., prediction-based object tracking algorithm with load balance (POTL) has been proposed to achieve significant power savings by reducing unnecessary transmission. Performance analysis, based on numerical analysis for one dimensional case, demonstrates that our scheme can dramatically reduce the power consumption and improve the lifetime of the overall network system. [C1380]

"Power management in wireless ad hoc networks using AODV"

This paper describes our proposed power management schemes, directional local recovery and dynamic power management, to reduce and balance power consumption. We introduce the power variance as a metric to evaluate the performance of power balancing. Using ns-2 and the ad hoc on-demand distance vector routing (AODV) protocol, we compare the performance of AODV with our extension against the original AODV. Simulation results show that our schemes provide substantial energy savings and thus prolong the battery life of mobile nodes while introducing limited increase in end-to-end delay. [C1381]

"PowerFITS: Reduce Dynamic and Static I-Cache Power Using Application Specific Instruction Set Synthesis"

Power consumption, performance, area, and cost are critical concerns in designing microprocessors for embedded systems such as portable handheld computing and personal telecommunication devices. In previous work [A. Cheng et al., (2004)], we introduced the concept of framework-based instruction-set tuning synthesis (FITS), which is a new instruction synthesis paradigm that falls between a general-purpose embedded processor and a synthesized application specific processor (ASP). We address these design constraints through FITS by improving the code density. A FITS processor improves code density by tailoring the instruction set to the requirement of a target application to reduce the code size. This is achieved by replacing the fixed instruction and register decoding of general purpose embedded processor with programmable decoders that can achieve ASP performance, low power consumption, and compact chip area with the fabrication advantages of a mass produced single chip solution to amortize the cost. Instruction cache has been recognized as one of the most predominant source of power dissipation in a microprocessor. For instance, in Intel's StrongARMprocessor, 27% of total chip power loss goes into the instruction cache [J. Montanaro et al., (1996)]. In this paper, we demonstrate how FITS can be applied to improve the instruction cache power efficiency. Experimental results show that our synthesized instruction sets result in significant power reduction in the instruction cache compared to ARM instructions. For 21 benchmarks from the MiBench suite [M. Guthaus et al., (2001)], our simulation results indicate on average: a 49.4% saving for switching power; a 43.9% saving for internal power; a 14.9% saving for leakage power; a 46.6% saving for total cache power with up to 60.3% saving for peak power [C1382]

"Performance of routing strategy (bit error based) in fading environments for mobile adhoc networks"

In wireless adhoc networks, typical limitations of routing protocols include high power consumption, low bandwidth and high error rates. A greater performance loss is experienced due to multipath fading and shadowing, when the path between source and destination node is obstructed. These problems, while receiving

some attention, have not yet been much investigated. We have adopted probabilistic modeling to model the effect due to multipath fading and shadowing. The BER for each link affected by fading is estimated using the proposed model. A wireless routing protocol (WRP) maintains the BER associated with a particular link, a packet (data) is routed by the optimum BER route from a set of routes discovered by the protocol. It is found that the proposed model is capable of reducing the number of packet retransmissions, saves battery energy and also reduces overloading of a particular path by routing the packet through an optimal path (in terms of BER). [C1383]

"Adaptive low-power analog/digital converters for wireless sensor networks"

The paper addresses the problem of power consumption of sensor nodes in a wireless network. An integrated low-power analog/digital converter (ADC) is presented that is particularly suited for wireless sensor applications. The converter makes use of information theoretic redundancy in the input signal for reducing the conversion workload and performing data compression on-the-fly during conversion (entropy-coding A/D converter). Thus, energy is saved both in signal conversion and transmission. Experimental results from a prototype chip are presented. The converter is especially suitable for sensor networks that maintain a global data model. This is further illustrated on an exemplary scenario of distributed wave detection. It is shown that sensor signal detection and acquisition in this type of applications can be carried out very efficiently with entropy-coding converters used in the sensor nodes. [C1384]

"Localized Low-Power Topology Control Algorithms in IEEE 802.15.4-Based Sensor Networks"

Sensor networks have emerged as a promising technology with various applications, and power consumption is one of the key issues. Since each full function device can act as a coordinator or a device in IEEE 802.15.4 standard, 802.15.4-based sensor networks have various possible network topologies. In this paper, we try to construct network topologies with small number of coordinators while still maintaining network connectivity. By reducing the number of coordinators, the average duty cycle is reduced and the battery life is prolonged. Three topology control algorithms are proposed in this paper. Self-pruning is the simplest one with O(l) running time. Ordinal pruning significantly improves self-pruning in terms of power saving with O(n) running time. Layered pruning is a tradeoff between the first two pruning algorithms with O(radicn) running time and a little higher power consumption than ordinal pruning. Furthermore, all three algorithms are independent of the physical radio propagation characteristics [C1385]

"PCF: on exploiting spatial reuse and power conservation opportunities with power control and fairness mechanism for 802.11 WLAN"

Exploiting spatial reuse opportunities allows more parallel transmissions and improve the throughput of wireless networks. Power control is one of the major mechanisms used to exploit both spatial reuse and power conservation opportunities. Increasing the transmitting power prevents the receiver from interference but consume power and create additional interference to other communicating nodes. On the contrary, reducing the transmitting power reduces the interference to other communicating pairs and save sender's power consumption, but result a lower SNR (signal to noise ratio) at receiver side. This article presents power control MAC protocol to exploit the spatial reuse and power conservation opportunities for 802.11 wireless LAN. The proposed protocol evaluates the interference and adopts power control mechanism on both sender and receiver sides, trying to allow more communications proceeding simultaneously. In addition, a fairness control mechanism is also proposed to reduce the average communication delay and alleviate the packet lost phenomenon. Performance results reveal that the proposed protocol improves the throughput and power consumption of WLAN while the fairness among communicating pairs can be maintained. [C1386]

"Improving TCP performance for multihop wireless networks"

In this paper, we present a comprehensive performance evaluation of TCP NewReno and TCP Vegas with and without ACK thinning for static multihop wireless IEEE 802.11 networks. Opposed to previous studies, we consider not only IEEE 802.11 operating in ad hoc mode with 2 Mbit/s bandwidth, but also with 5.5 Mbit/s and 11 Mbit/s bandwidths. Simulation results using ns-2 show that TCP Vegas achieves between 15% and 83% more goodput and between 57% and 99% fewer packet retransmissions than TCP NewReno. Considering fairness among multiple TCP flows, we show that using TCP Vegas results in between 21% and 95% fairness improvement compared to TCP NewReno. The reduced amount of packet retransmissions of TCP Vegas also leads to significant savings of energy consumption. The paper gives insight on the particular reasons for such performance advantages of TCP Vegas in comparison to TCP NewReno. [C1387]

"Development of PV/T system in Thailand"

This paper reports the development of a photovoltaic/thermal (PV/T) system in Thailand. The system uses amorphous silicon (a-Si) solar cells as the sunlight absorber. The system was first developed in Thailand by NSTDA (National Science and Technology Development Agency). The objective of developing PV/T system in Thailand is to reduce the total energy consumption in Thailand by using free energy such as solar radiation. The advantages of PV/T system are generating both electricity and heat at the same time by the same unit. The initial cost of the system can be reduced over 25% when compared with the conventional PV and thermal generation system. Therefore, the pay back period is faster for this system. Another objectives are to study the energy saving by using a-Si PV/T solar collector system which use a-Si instead of the black chrome coated absorber, which is expensive and to study its performance under tropical climate such as Thailand. Up to now, three pilot PV/T systems were installed at government divisions in Thailand by difference type of applications. [C1388]

"Optimal module and voltage assignment for low-power"

Reducing power consumption through high-level synthesis has attracted a growing interest from researchers due to its large potential for power reduction. In this work we study functional unit binding (or module assignment) given a scheduled data flow graph under a dual-Vddframework. We assume that each functional unit can be driven by a low Vddor a high Vdddynamically during run time to save dynamic power. We develop a polynomial-time optimal algorithm for assigning low Vddto as many operations as possible under the resource and time constraint, and in the same time minimizing total switching activity through functional unit binding. Our algorithm shows consistent improvement over a design flow that separates voltage assignment from functional unit binding. We also change the initial scheduling to examine power-latency tradeoff scenarios. Experimental results show that we can achieve a 21% power reduction when latency bound is tight. When latency is relaxed by 10 to 100%, the power reduction is 31 to 73% compared to the synthesis results for the case of single high Vddwithout latency relaxation. We also show comparison data of energy consumption under the same experimental setting. [C1389]

"On multiple-voltage high-level synthesis using algorithmic transformations"

This paper presents a multiple-voltage high-level synthesis methodology for low power DSP applications using algorithmic transformation techniques. Our approach is motivated by maximization of task mobilities in that the increase of mobilities may raise the possibility of assigning tasks to low-voltage components. The mobility means the ability to schedule the starting time of a task. It is defined as the distance between its as-late-as-possible (ALAP) schedule time and its as-soon-as-possible (ASAP) schedule time. To earn task mobilities, we use loop shrinking, retiming and unfolding techniques. The loop shrinking can first reduce the iteration period bound (IPB) and, then, the others are employed for shortening the minimum achieved sample period (MASP) as much as possible. The minimization of MASP results in high task mobilities. Thereafter, we can assign tasks with high mobilities to low-voltage components and minimize energy dissipation under resource and latency constraints. With considering the overhead of level conversion, our approach can achieve significant power reduction. For instance, as the experimental results, we can save the power consumption up to 54.77% for the case of the third-order IIR filter. [C1390]

"Development of a recyclable PV-module-expansion to multi-cells modules"

By recycling PV cells, we can save the significant amount of energy consumed in the manufacture of PV cells, and reduce the total cost of PV modules as a consequence. We are developing a recyclable PV-module called "double encapsulation module (DEM)", in which a transparent nonadhesive film to PV cell is placed between PV cell and EVA. We have reported experimental results of the DEMs using single cell modules in the previous papers. To show the feasibility of this concept for practical use, we made 9-cells DEMs and extracted problems from the assembling and disassembling processes. Examination of the reliability for 9-cell DEMs was also made. Furthermore, module disassembly and cell recovery examination were conducted. We confirmed that successful recovery of PV cells from the 9-cell DEMs is possible. [C1391]

"A clustering topology control algorithm for heterogeneous wireless network"

A critical issue in designing sensor topology control algorithms is to minimize the energy consumption for longevity. Most existing algorithms on topology control assume homogeneous wireless nodes with uniform maximum transmission ranges, and cannot be directly applied to heterogeneous wireless multi-hop networks in which the maximum transmission range of each node may be different. We present a localized topology control algorithm for heterogeneous networks: directed relative neighborhood graph based on clustering (DRNGC). In this algorithm, each node in the same cluster selects a set of neighbors based on the locally collected information. Simulation results show that DRNGC reduces the average degree of cluster-heads by up to 75%

and translates the power of cluster-heads by up to 75%, implying that there is a significant amount of energy-saving in collecting sensed data and of reducing cluster-head workload. [C1392]

"A framework for performance modeling of wireless sensor networks"

Energy conserving design is the research focus to prolong the lifetime of sensor networks. A simple and effective way to save energy is to place nodes in sleep mode, however, sleep mode corresponds to low power consumption as well as to reduced operation capacity and increased latency. We derive a queuing model for the sensor node and performance models for the whole sensor network. We use our models to study the node and network performance metrics in terms of throughput, energy consumption and packet delivery delay. Our analytical models enable us to explore the trade-off existing between sensor sleep/active dynamics and those performance metrics. We validate our analytical results through extensive simulations and simulation results match well with our analysis and show the accuracy of our framework. [C1393]

"Constructing battery-aware virtual backbones in sensor networks"

A critical issue in wireless sensor networks is to construct energy efficient virtual backbones for routing, broadcasting and data propagating. The minimum connected dominating set (MCDS) has been proposed as a backbone to reduce power dissipation and prolong network lifetime. However, we find that an MCDS cannot guarantee maximum network lifetime as it does not consider the battery discharging behavior. Recent study in battery technology reveals that the discharging of a battery is not linear. Batteries tend to discharge more power than needed, and reimburse the over-discharged power later if they have sufficiently long recovery time. In order to optimize network performance and construct an energy efficient virtual backbone in sensor networks, battery-awareness should be considered. In this paper we first study the mathematical battery discharging model and provide a simplified battery model suitable for implementation in sensor networks. We then introduce the concept of battery-aware connected dominating set (BACDS) and show that in general the BACDS can achieve longer lifetime than the MCDS. Then we show that finding a minimum BACDS (MBACDS) is NP-hard and give a distributed approximation algorithm to construct the BACDS. The resulting BACDS constructed by our algorithm is at most $(8+\Delta)$opt size where Δ is the maximum node degree and opt is the size of an optimal BACDS. The time and message complexities of the algorithm are $O(n)$ and $O(n(\sqrt{n}+\log n+\Delta))$, respectively, where n is the number of nodes in the network. The simulation results show that the BACDS constructed by our algorithm can save a significant amount of energy and achieve up to 30% longer network lifetime than the MCDS. To the best of our knowledge, this is the first work considering battery-awareness in the construction of connected dominating sets. [C1394]

"p-MANET: Efficient Power Saving Protocol for Multi-Hop Mobile Ad Hoc Networks"

In this paper, we propose an efficient power saving protocol for multi-hop mobile ad hoc networks, called p-MANET. Our design is expected as a new foundation MAC layer power saving protocol. The main goals of p-MANET protocol are to reduce significant power consumption and transmission latency, and to achieve efficient power saving. Each mobile node in p-MANET only needs to become active during one beacon interval for every n interval where n is the size of a super frame. Thus, efficient power saving is expected. p-MANET also yields low transmission latency because that every mobile node is aware of the active beacon intervals of its neighbors such that it can easily choose a neighbor in active mode or with the least remaining time to wake up to forward packets. Simulations are also conducted to show the efficiency of the proposed p-MANET [C1395]

"Power minimization techniques on distributed real-time systems by global and local slack management"

Recently, a static power management with parallelism (P-SPM) technique has been proposed to reduce the energy consumption of distributed systems to execute a set of real-time dependent tasks (Mishra et al., 2003). The authors claimed that the proposed P-SPM outperforms other known methods in energy reduction. However, how to take advantage of the local static slack for further energy optimization remains as an open problem. In this paper, we propose the static power management with proportional distribution and parallelism scheme (PDP-SPM) that not only answers this open problem, but also exploits the parallelism. Simulations on task graphs derived for DSP applications and TGFF benchmark suite suggest that PDP-SPM achieves 64% energy saving over the system without power management, and 15% over the P-SPM scheme. [C1396]

"Power analysis of link level and end-to-end data protection in networks on chip"

We provide a power analysis for the communication in the Nostrum NoC concluding that power consumption is dominated by the links between switches while the switches and network interfaces contribute with a mere few percent to the power consumption. Further, we analyze link level low power encoding techniques with the

conclusion that they spend several times more power than no encoding at all, if normalized for the same performance, which is done by adjusting supply voltage and frequency. Data protection schemes also have the potential to reduce power if voltage levels can be reduced and certain faults can be tolerated. We experiment with link level and end-to-end data protection schemes. They only moderately increase power consumption and have indeed the potential to save power. However, this potential strongly depends on the application traffic patterns and fault models of future technology generations. [C1397]

"A three-level toggle-avoid bus signaling scheme"

Coupling capacitances between bus lines are dominant in deep-submicron technologies, as a result, both power dissipation and worst-case delay are increased due to coupling transitions. Based on the observation that the toggling sequences 01->10 or 10->01 between two adjacent lines result in four times more coupling energy than other coupling events, we propose a toggle-avoid signaling scheme. By applying a three-level signaling on buses with a choice for representing logic "1", toggling events are reduced with no extra bus lines. We achieve 32% total power savings and 40% worst-case delay reduction with a small power overhead. [C1398]

"Architectural design of fractal image coder based on kick-out condition"

In recent years, fractal image coding has been applied in many applications. Fractal encoding needs a large search and comparison time, so it is therefore required to implement the encoder in hardware to improve the speed. This paper is intended to propose a novel architectural design of fractal image coder based on the predetermined kick-out condition which can reduce the computational load. We devise a technique to encode the mean of the range block by the fractal image coding format to save a bit which is used to indicate whether the range block is encoded by its mean or fractal image coding. We also present the order of eight isometric transformations to save the power consumption of multipliers when computing the product term to obtain the optimal contrast scaling factor. Finally, experimental results are demonstrated to show the effectiveness of the fractal image coder design. [C1399]

"Pipelining technique for energy-aware datapaths"

This paper presents a novel method to improve the energy awareness of the pipelined datapaths for varying throughputs. It activates the pipeline registers only when necessary; i.e. a data item can bypass the pipeline registers when the operation is free of race from the succeeding one, and when the glitch is minimal. Then, the clock pulses of the unused pipeline registers are gated to reduce the energy dissipation. Compared to the conventional clock gating approach, our proposed on-demand pipelining eliminates all redundant clock pulses whenever the peak datarate is not reached. Moreover, our method has a constant input-to-output latency for all operation modes, which significantly simplifies the integration tasks. In our simulations, the proposed on-demand pipelining saves up to 80% energy of conventional pipelined datapaths, and it can reduce about 34% 39% energy dissipation of those with gated-clock only. [C1400]

"Pre-capturing static pulsed flip-flops"

The paper presents pre-capturing static pulsed flip-flops (PCSPFF), which are composed of a pulse generator and a static flip-flop with equal toggling delays. The pre-capturing technique makes PCSPFF faster than other high-performance flip-flops. Power consumption of the PCSPFF is observed to be the lowest among high-performance flip-flops. HSPICE simulation results at a frequency of 400 MHz show that the proposed PCSPFF exhibits power-delay-product reductions of 39.7% and 29%, respectively, compared to the hybrid-latch flip-flop and the conditional-capture flip-flop. Moreover, in practical circuits, the proposed PCSPFF shows power reduction of more than 50% and 32%, respectively, compared to the hybrid-latch flip-flop and conditional-capture flip-flop. A double-edge triggering feature can be added to the proposed flip-flops to reduce the clock frequency by 50%. Using double-edge triggering in the proposed flip-flops, an energy saving of 94% is achieved on the clock distribution network. Incorporating the double-edge triggering technique along with sharing pulse generation among flip-flops presents up to 68% power reduction in an 8-bit counter. [C1401]

"A multiplication-accumulation computation unit with optimized compressors and minimized switching activities"

A low-power multiplication-accumulation computation (MAC) unit using the radix-4 Booth algorithm is proposed; its architectural complexity is reduced and switching activities are minimized. However, to maintain a high performance, the critical delays and hardware complexities of MAC units are explored to derive a MAC unit with high performance and low hardware complexity. A carry-save addition operation with optimized compressors is proposed to omit the use of half adders to reduce the hardware complexity further. A scheme to reduce switching

activity is also proposed to lower the power consumption of the MAC unit. In performing a MAC for XЧY+Z, the effective dynamic ranges of X and Y are detected; the one with the smaller effective dynamic range is processed for Booth decoding so as to increase the probability of the partial products being zero, and thus the switching activity is reduced. Also, the effective dynamic range of the result from this multiplication is estimated and compared with the effective dynamic range of the datum, Z. The larger effective dynamic range of the two data is considered as the effective word length for an addition operation. Pipelined latches are used to make the noneffective operation maintain the status of the previous operation so as to reduce the switching activities from the addition performed in MAC. After the addition operation, sign extension is performed on the result from the effective sign bit copied to non-effective bits to derive at a correct output datum. Compared to conventional MAC units, the proposed one is able to reduce 21.09% to 43.74% of power consumption. Additionally, the proposed MAC unit outperforms conventional ones in comparing the product of critical delay, area, and power consumption. [C1402]

"Exploiting temporal idleness to reduce leakage power in programmable architectures"

One of the biggest challenges that programmable devices like FPGAs are facing in ultra deep sub-micron regime is the exponential rise in leakage power consumption. As technology shrinks below 90nm, a new design paradigm has to evolve to tackle the issue of leakage power consumption. In this work we focus on a new design methodology for reducing leakage power by exploiting temporal locality in designs and accordingly group them into clusters that can be switched on and off. We propose a power state controller based method, which controls the switching of the clusters from one state to another. We show our technique using data flow graphs where temporal locality can be effectively explored. Our results show that substantial leakage savings can be achieved if temporal idleness of designs can be exploited effectively. [C1403]

"A fixed-point 3D graphics library with energy-efficient cache architecture for mobile multimedia systems"

A 3D computer graphics (3DCG) library with energy-efficient cache architecture is implemented for mobile multimedia systems. The developed library is based on fixed-point arithmetic for low energy consumption. To achieve high performance, the library is optimized at both the assembly and the algorithm levels on 3 different advanced RISC machine (ARM) processors. In order to enhance energy-efficiency as well as performance, a series of simulations have been performed on application programs with various cache configurations. We find that a 2-way set associative cache consumes low energy with negligible performance degradation. In this cache system, the optimized library can achieve 66.1% performance improvement and 25.3% energy saving on average compared with the conventional 4-way set associative cache system. Software and hardware co-optimization achieves 67 K polygons/s with low energy consumption. We verified the graphics library with proposed cache architecture by implementing a mobile graphics LSI. [C1404]

"An application-level methodology to guide the design of intelligent-processing, power-aware passive RFIDs"

We provide a methodology for reducing the power consumption in wireless sensor networks based on wireless active nodes (also implementing RFID reading ability) and sensor/processing-integrated passive RFIDs. Information acquired by the low cost, redundant, passive units is suitably compressed with an integrated sensor fusion algorithm based on neural networks, hence reducing the data to be transmitted to (and stored in) the reading unit. The methodology, by exploiting the application needs, also identifies the minimum number of bits to be transmitted to the reader (communication bit rate) as well as those required at each neuron output (information which immediately impacts on its complexity and electronics design) composing the sensor fusion algorithm. Simulation results applied to a comfort monitoring application in buildings show the effectiveness of the method with an energy saving factor of about 55% in the considered application. [C1405]

"Joint power management of memory and disk"

The paper presents a scheme to combine memory and power management for achieving better energy reduction. Our method periodically adjusts the size of physical memory and the timeout value to shut down a hard disk for reducing the average power consumption. We use Pareto distributions to model the distributions of idle time. The parameters of the distributions are adjusted at run-time for calculating the corresponding timeout value of the disk power management. The memory size is changed based on the inclusion property to predict the number of disk accesses at different memory sizes. Experimental results show more than 50% energy savings compared to a 2-competitive fixed-timeout method. [C1406]

"A way memoization technique for reducing power consumption of caches in application specific

integrated processors"

This paper presents a technique for eliminating redundant cache-tag and cache-way accesses to reduce power consumption. The basic idea is to keep a small number of most recently used (MRU) addresses in a memory address buffer (MAB) and to omit redundant tag and way accesses when there is a MAB-hit. Since the approach keeps only tag and set-index values in the MAB, the energy and area overheads are relatively small even for a MAB with a large number of entries. Furthermore, the approach does not sacrifice the performance. In other words, neither the cycle time nor the number of executed cycles increases. The proposed technique has been applied to the Fujitsu VLIW processor (FR-V) and its power saving has been estimated using NanoSim. Experiments for 32 kB 2-way set associative caches show the power consumption of I-cache and D-cache can be reduced by 40% and 50%, respectively. [C1407]

"An adaptive locality-conscious process scheduler for embedded systems"

A critical component of a real-time operating system (RTOS) is its process scheduler. While the prior research on process scheduling focuses mostly on meeting hard/soft deadlines, preemption and priory assignment related issues, problems arise from existence of cache memories are largely ignored. Focusing on data accesses and a cache based embedded system, this paper proposes an adaptive locality-conscious process scheduling algorithm. The main goal of the proposed algorithm is to exploit (reuse) the contents of the on-chip cache memory to the highest extent possible. The algorithm tries to achieve its goal by determining the order in which the processes get scheduled such that the successively-executing processes share a large number of data elements. We implemented our scheduler within a customized simulation platform and simulated it using a set of benchmark codes. Our experimental results reveal that the proposed scheduling algorithm is very successful in practice, and reduces process completion times significantly for both rate-monotonic scheduling (RMS) and earliest-deadline-first scheduling (EDF). We also explain how process code transformations can be used for increasing the savings achieved by the locality-conscious scheduler, and show how the proposed approach operates with a base scheduler such as RMS and EDF. [C1408]

"A New Energy Efficient Protocol for Minimizing Multi-Hop Latency in Wireless Sensor Networks"

In wireless sensor networks, efficient usage of energy helps in improving the network lifetime. As the battery of a sensor node, in most cases, cannot be recharged or replaced after the deployment of the sensors, energy management becomes a critical issue in such networks. In order to detect an event, a sensor network spends majority of the time in monitoring its environment, during which a significant amount of energy can be saved by placing the radio in the low-power sleep mode. This can be achieved by using a dual frequency radio setup. However, such energy saving protocols increase the latency encountered in setting up a multihop path. We, in this paper, propose a reservation scheme, latency minimized energy efficient MAC protocol (LEEM), which is a novel hop-ahead reservation scheme in a dual frequency radio to minimize the latency in the multihop path data transmission by reserving the next hop's channel a priori. Thus, in a multihop sensor network, a packet can be forwarded to the next hop, as soon as it is received by a sensor node, which helps in eliminating the delay incurred for setting up the path. Simulation results show that LEEM consumes lesser power and reduces end-to-end latency by around 50% than that of the existing schemes [C1409]

"Quasi-static voltage scaling for energy minimization with time constraints"

Supply voltage scaling and adaptive body-biasing are important techniques that help to reduce the energy dissipation of embedded systems. This is achieved by dynamically adjusting the voltage and performance settings according to the application needs. In order to take full advantage of slack that arises from variations in the execution time, it is important to recalculate the voltage (performance) settings during run time, i.e., online. However voltage scaling (VS) is computationally expensive, and thus significantly hampers the possible energy savings. To overcome the online complexity, we propose a quasi-static voltage scaling scheme, with a constant online time complexity O(1). This allows us to increase the exploitable slack as well as to avoid the energy dissipated due to online recalculation of the voltage settings. We conduct several experiments that demonstrate the advantages of the proposed technique over the previously published voltage scaling approaches. [C1410]

"Nonuniform banking for reducing memory energy consumption"

Main memories can consume a large percentage of overall energy in many data-intensive embedded applications. The past research proposed and evaluated memory banking as a possible approach for reducing memory energy consumption. One of the common characteristics/assumptions made by most of the past work on banking is that all the banks are of the same size. While this makes the formulation of the problem easy, it also restricts the potential solution space. Motivated by this observation, this paper investigates the possibility of employing nonuniform bank sizes for reducing memory energy consumption. Specifically, it proposes an integer

linear programming (ILP) based approach that returns the optimal nonuniform bank sizes and accompanying data-to-bank mapping. It also studies how data migration can further improve over nonuniform banking. We implemented our approach using an ILP tool and made extensive experiments. The results show that the proposed strategy brings important energy benefits over the uniform banking scheme, and data migration across banks tends to increase these savings. [C1411]

"Reducing the power consumption of FPGAs through retiming"

High power dissipation is one of the major disadvantages of FPGAs. A main part of the power consumed is caused by glitches. This paper analyzes the effect of retiming to reduce the power dissipation of a Xilinx Virtex-II FPGA. The authors introduce a method to insert staging registers into large designs, that are constructed from a high abstraction level language algorithmic description. Results obtained by measurements suggest a high potential for power savings through retiming. [C1412]

"Tag overflow buffering: an energy-efficient cache architecture"

We propose a novel energy-efficient memory architecture which relies on the use of a cache with a reduced number of tag bits. The idea behind the proposed architecture is based on moving a large number of the tag bits from the cache into an external register (tag overflow buffer) that identifies the current locality of the memory references; additional hardware allows us to dynamically update the value of the reference locality contained in the buffer. Energy efficiency is achieved by using, for most of the memory accesses, a reduced-tag cache. This architecture is minimally intrusive for existing designs, since it assumes the use of a regular cache, and does not require any special circuitry internal to the cache such as row or column activation mechanisms. Average energy savings are 51% on tag energy, corresponding to about 20% saving on total cache energy, measured on a set of typical embedded applications. [C1413]

"Exploiting dynamic workload variation in low energy preemptive task scheduling"

A novel energy reduction strategy to maximally exploit the dynamic workload variation is proposed for the offline voltage scheduling of preemptive systems. The idea is to construct a fully preemptive schedule that leads to minimum energy consumption when the tasks take on approximately the average execution cycles yet still guarantees no deadline violation during the worst-case scenario. End-time for each sub-instance of the tasks obtained from the schedule is used for the on-line dynamic voltage scaling (DVS) of the tasks. For the tasks that normally require a small number of cycles but occasionally a large number of cycles to complete, such a schedule provides more opportunities for slack utilization and hence results in larger energy saving. The concept is realized by formulating the problem as a nonlinear programming (NLP) optimization problem. Experimental results show that, by using the proposed scheme, the total energy consumption at runtime is reduced by as much as 60% for randomly generated task sets when compared with the static scheduling approach only using worst case workload. [C1414]

"Feedback-based dynamic voltage and frequency scaling for memory-bound real-time applications"

Dynamic voltage and frequency scaling is increasingly being used to reduce the energy requirements of embedded and real-time applications by exploiting idle CPU resources, while still maintaining all application's real-time characteristics. Accurate predictions of task run-times are key to computing the frequencies and voltages that ensure that all tasks' real-time constraints are met. Past work has used feedback-based approaches, where applications' past CPU utilizations are used to predict future CPU requirements. Mispredictions in these approaches can lead to missed deadlines, suboptimal energy savings, or large overheads due to frequent changes to the chosen frequency or voltage. One shortcoming of previous approaches is that they ignore other 'indicators' of future CPU requirements, such as the frequency of I/O operations, memory accesses, or interrupts. This paper addresses the energy consumptions of memory-bound real-time applications via a feedback loop approach, based on measured task run-times and cache miss rates. Using cache miss rates as indicator for memory access rates introduces a more reliable predictor of future task run-times. Even in modern processor architectures, memory latencies can only be hidden partially, therefore, cache misses can be used to improve the run-time predictions by considering potential memory latencies. The results shown in this paper indicate improvements in both the number of deadlines met and the amount of energy saved. [C1415]

"Behavioral synthesis of data-dominated circuits for minimal energy implementation"

This paper presents a power estimation and optimization approach in the early stage of behavioral synthesis for unscheduled data-dominated circuits. A methodology for estimating the power consumption of every module in the system is developed using an automatic construction of a novel switching table and the power table. An integer linear programming model is presented to reduce the energy consumption of the circuit through

concurrent module selection, binding, and scheduling for a non-scheduled data path. Experimental results of six data-dominated benchmarks show that our technique achieves an average of 29.8% energy savings compared to a traditional area optimal synthesis algorithm where energy is not considered. Additionally, this approach consumes on the average 24.0% and 20.3% less energy compared to two other power-oriented optimization strategies respectively. [C1416]

"Evaluation of speed and area of clustered VLIW processors"

Splitting a wide-issue VLIW processor in clusters decreases the clock period, area and power consumption. Previous studies of the physical benefits from clustering focused on the scalability of the register file, based on speculative analytical models. In contrast, we evaluate speed and area of the whole VLIW datapath, including the register files, FUs, and bypasses through realistic physical layout experiments. Our baseline is an optimized for speed 8-issue-slot VLIW pipeline, derived from a commercial media processor. Despite the frequent prior-art assumption that the register file defines the clock frequency of a clustered VLIW processor, we discovered it is the FU bypass network that limits the clock speed. After a drastic 1.75 clock frequency speedup from clustering the unicluster into two clusters, subsequent clustering brings modest 2.05 and 2.17 speedups for the 4- and 8-cluster VLIWs, respectively. Combined with cycle count increase trends due to clustering, this leads to the conclusion that excessive clustering does not speed up the processor. Furthermore, clustering reduces area of the VLIW datapath. In our experiments the area savings due to clustering reach 14.2%, 43.5% and 50.5% for the 2-, 4-, and 8-cluster VLIWs, respectively. [C1417]

"Energy storage on board of railway vehicles"

The proposed energy storage on board of a railway vehicle leads to a big step in the reduction of consumed energy. Up to 30% energy saving are measured in a prototype light rail vehicle, at the same time reducing the peak power demand drastically. Additionally, operation without catenary for several hundred meters was successfully demonstrated with the prototype light rail vehicle driving with switched off pantograph. This prototype vehicle is in passenger operation since September 2003, the implemented software is optimized on energy savings. About two years experience is available and the results are convincing. Applying the energy storage to diesel-electrical multiple units leads to fuel savings and provides a "booster" effect on the acceleration performance. The stored energy is adding additional power on top of the diesel engine power during acceleration. Compared to original diesel power, this additional power can be provided with a relatively low additional weight. Finally, the energy savings of up to 30% and the corresponding emission reduction will already fulfill the targets of various local and global energy saving programs set up by e.g. European Union and big railway operators [C1418]

"Level-shifter free design of low power dual supply voltage CMOS circuits using dual threshold voltages"

Usage of dual supply voltages in a digital circuit is an effective way of reducing power consumption due to the quadratic relation of supply voltage to power consumption. But the need for level shifters when a low voltage gate drives a high voltage gate has been a limiting factor preventing widespread usage of dual supply voltages in digital circuit design. The overhead of level shifters forces designers to increase the granularity of dual voltage assignment, reducing the maximum obtainable savings. We propose a method of applying dual supply voltages at gate level granularity without using level shifters. We modify the threshold voltage of the high voltage gates that are driven by low voltage gates in order to obtain the level shifting operation together with the logic operation. Using our method, we obtained an average of 20% energy savings for ISCAS'85 benchmark circuits. [C1419]

"Dynamically exploiting frequent operand values for energy efficiency in integer functional units"

We propose a design methodology for exploiting certain frequently occurring operand subword values to reduce energy consumption in integer functional units (FUs). Our methodology partitions an FU into subunits that operate on disjoint operand subwords; a subunit saves energy when its input is an "exploitable" subword value combination. In practice, the applicability and energy optimization of such a method depend significantly upon a number of factors ignored in previous work: the function implemented the hardware topology of the FU, and the application. Our methodology considers all these factors. We use a fast, energy-optimal partitioning algorithm based on an accurate energy model derived from detailed circuit-level simulations and apply it to several different integer FUs. Our results show average energy savings between 20% and 28% (an improvement of 28-40% with respect to previous techniques) across several SPEC CPU2000 benchmarks for different FUs with negligible delay and reasonable area overheads. [C1420]

"Gibraltar: Application and Network Aware Adaptive Power Management for IEEE 802.11"

IEEE 802.11 power save mode and other power management mechanisms while reducing the power consumption of a wireless subsystem may significantly degrade application performance increasing overall system power. A new power management algorithm, codenamed Gibraltar, which adapts to application level network behavior and current network conditions, has been developed to reduce 802.11 power consumption and to limit application delays. Gibraltar algorithm was implemented as an NDIS intermediate driver for the Intel PRO/Wireless 2200BG miniPCI card and experiments were conducted for web browsing and email applications. Measured results demonstrated that Gibraltar is very effective in managing power of a wireless subsystem and limiting application delay. For example, for web browsing when compared to 802.11 power save mode, Gibraltar reduces power consumption by 28% and delay by 19%. Further, Gibraltar is able to consistently reduce system energy consumption across applications and device types providing a viable solution for 802.11 power management. [C1421]

"On the limits of leakage power reduction in caches"

If current technology scaling trends hold, leakage power dissipation soon becomes the dominant source of power consumption. Caches, due to the fact that they account for the largest fraction of on-chip transistors in most modern processors, are a primary candidate for attacking the leakage problem. While there has been a flurry of research in this area over the last several years, a major question remains unanswered. What is the total potential of existing architectural and circuit techniques to address this important design concern? In this paper, we explore the limits in which existing circuit and architecture technologies may address this growing problem. We find that by using perfect knowledge of the address trace to carefully apply sleep and drowsy modes, the total leakage power from the instruction cache may be reduced to mere 3.6% of the unoptimized case, and the total from the data cache reduced to only 0.9%. We also present a complete parameterized model to determine the optimal leakage savings while the implementation technology changes over time. We further suggest how such limits might be approached using a form of prefetching for low power. [C1422]

"Variable input delay CMOS logic for low power design"

Modern digital circuits consist of logic gates implemented in the complementary metal oxide semiconductor (CMOS) technology. The time taken for a logic gate output to change after one or more inputs have changed is called the delay of the gate. A conventional CMOS gate is designed to have the same input to output delay irrespective of which input caused the output to change. We propose a new gate design that has different delays along various inputs to output paths within the gate. This is accomplished by inserting selectively sized "permanently on" series transistors at the inputs of the logic gate. We demonstrate the use of the variable input delay CMOS gates for a totally glitch-free minimum dynamic power implementation of a digital circuit. Applying a previously described linear programming method to the c7552 benchmark circuit, we obtained a power saving of 58% over an un-optimized design. This power consumption was 18% lower than that for an alternative low power design using conventional CMOS gates. All circuits had the same overall delay. Since the overall delay was not allowed to increase, the glitch elimination with conventional gates required insertion of delay buffers on non-critical paths. The use of the variable input delay gates drastically reduced the required number of delay buffers. [C1423]

"A novel bus encoding scheme from energy and crosstalk efficiency perspective for AMBA based generic SoC systems"

Interwire coupling is a major source of power consumption and delay faults for on-chip buses implemented in UDSM SoC systems. Elimination or minimization of such faults is crucial to the performance and reliability of SoC designs. This paper presents a new on-chip bus encoding scheme targeting high performance generic SoC systems. In addition to its efficiency in terms of power, the scheme reduces delay faults by completely eliminating the most critical type of crosstalk coupling that causes three adjacent wires to undergo Miller-like transition simultaneously. The paper describes the technique, its implementation (using the widely adopted AMBA-AHB SoC bus standard) and provides results indicating between 24% to 38% energy saving for systems implemented in 0.18 μm CMOS technology. [C1424]

"Adaptive power management for mobile agent-based information retrieval"

Mobile agent technology has been used in wireless distributed information retrieval for many years. However, the energy-efficiency issue in such systems remains unexplored. In this paper, we proposed an adaptive application-driven power management (AADPM) protocol for mobile agent-based applications within the IEEE 802.11b infrastructure WLAN environment. Our goal is to minimize energy while achieving low round trip time (RTT)

delay. We discuss the protocol and evaluate its effectiveness using the network simulator NS2. We also draw horizontal comparisons among a variety of PM methods reported in the literature. Experimental results show that, compared to the power save mode supported by 802.11b, AADPM reduces the network interface card energy consumption by 65% while only introducing 3% RTT delay. [C1425]

"Low-power way-predicting cache using valid-bit pre-decision for parallel architectures"

Focusing on the way-predicting cache with sub-block placement, we propose a new cache scheme that uses the valid bits from data memory to pre-decide disabling the unnecessary tag-subarrays and data-subarrays. By valid-bit pre-decision, it significantly helps in improving the average energy saving of the conventional way-predicting cache without valid-bit pre-decision, especially for with large associativity and small sub-block size. Moreover, the proposed way-predicting cache can be applied to the parallel architecture systems to reduce the overall power consumption. [C1426]

"Design and implementation of a decimation filter for hearing aid applications"

In this paper we deal with the design and implementation of a decimation filter used for hearing aid applications. We implement the decimation filter using the canonic signed digit (CSD) representation. Each digital filter structure is simulated using Matlab, and its complete architecture is captured using DSP Blockset and Simulink. The filter has been implemented on Xilinx FPGA using Virtex-2 technology. The resulting architecture is hardware efficient and consumes less power compared to conventional decimation filters. Compared to the comb-FIR-FIR architecture, the designed decimation filter architecture contributes to a hardware saving of 69%; in addition, it reduces the power dissipation by 83%, respectively. [C1427]

"A power saving MAC protocol by increasing spatial reuse for IEEE 802.11 ad hoc WLANs"

Scarce resources of wireless medium (e.g., bandwidth, battery power, and so on) significantly restrict the progress of wireless local area networks (WLANs). Heavy traffic load and high station density are most likely to incur collisions, and further consume bandwidth and energy. In this paper, a distributed power-saving protocol, power-efficient MAC protocol (PEM), to avoid collisions and to save energy is proposed. PEM takes advantage of power control technique to reduce the interferences among transmission pairs and increase the spatial reuse of WLANs. Based on the concept of maximum independent set (MIS), a novel heuristic scheme with the aid of interference relationship is proposed to provide as many simultaneous transmission pairs as possible. In PEM, all stations know when to wake up and when they can enter doze state. Thus, stations need not waste power to idle listen and can save much power. The network bandwidth can be efficiently utilized as well. To verify the performance of PEM, a lot of simulations are performed. The experimental results show that with the property of spatial reuse, PEM not only reduces power consumption, but also leads to higher network throughput in comparison with the existing work, such as DCF, DCS, and DPSM. [C1428]

"Energy-efficient resource allocation for multiband UWB communication systems"

The emerging ultra-wideband (UWB) system offers a great potential for the design of high-speed short-range communications. However, UWB faces a significant challenge in achieving a low transmit power level, while assuring an adequate system performance. An efficient management of the limited power is thus a key feature to fully exploit the advantages of UWB. In this paper, a cross layer multiuser multiband UWB scheme is proposed to obtain the optimal subband and power allocation strategy. Optimization criteria involve minimization of power consumption under the constraints on the packet error rate, transmission rate, and FCC regulations. To reduce the problem complexity, which is found to be NP hard a computationally inexpensive suboptimal approach is developed. Simulation results under UWB channel model specified in the IEEE 802.15.3a standard show that the proposed algorithm achieves comparable performance to that of the complex optimal full search approach, and it can save up to 61% of transmit power compared to the multiband scheme in the standard proposal. [C1429]

"A low power embedded dataflow coprocessor"

Power consumption has become one of the most important concerns in microprocessor design. However, the potential for further power-saving in microprocessors with a conventional architecture is limited because of their unified architectures and mature low-power techniques. An alternative way is proposed in this paper to save power-embedding a dataflow coprocessor in a conventional RISC processor. The dataflow coprocessor is designed to execute short code segments very efficiently. The primary experimental results show that the dataflow coprocessor can increase the power efficiency of a RISC processor by an order of magnitude. [C1430]

"Energy efficient architectures for the log-MAP decoder through intelligent memory usage"

Turbo decoding generally employs maximum a posteriori (MAP) and the soft output Viterbi (SOVA) algorithm in its soft-input soft-output (SISO) component decoders. This paper reformulates the implementation of a low power Log-MAP decoder with reduced storage requirement and based on the optimized MAP algorithm that calculates the reverse state metrics in the forward recursive manner. As a result, the authors present new low power derivatives of this decoder through a variation in the percentage of memory savings. Three low power architectures of the Log-MAP decoder not employing the sliding window technique have been developed and post layout power savings of approximately 44%, 40% and 36% with respect to the conventional implementation have been observed. [C1431]

"Critical area attention in traffic aware dynamic node scheduling for low power sensor networks"

In many sensor network (SN) applications it is necessary to provide reliable, fast and full sensing coverage to a sensitive area while at the same time minimizing energy consumption. This paper proposes a new flexible medium-access control (MAC) protocol designed to address this problem. The primary objective of the SN is to achieve low-power consumption while latency is usually less important compare to traditional wireless networks. This characteristic of SN motivates the design of a new MAC layer so that power consumption is reduced. In this paper, a novel traffic-aware algorithm based on a distributed node schedule management (DMD) protocol is introduced that dramatically increases energy saving, especially in intermediate devices inside a multi-hop network. In addition, high QoS is providing for important areas. Support of QoS in MAC layer reduced the routing overhead significantly. The simulation results show noticeable power consumption improvements compared to 802.11-like, sensor MAC and dynamic SMAC protocols, especially in the large scale, which has been achieved by a tradeoff of more latency. [C1432]

"A replacement policy to save energy for data cache"

For a current processor, it has been reported that more than 50% of power has been consumed by an on-chip cache memory. To reduce power consumption for the cache memory, it is required to develop an effective replacement policy and mapping function, which would decide the cache memory accesses. In this paper, we introduce an ELRU-SEQ replacement policy with skewed mapping function to save energies for data caches. In addition, we develop an integrated power model by using Spectre and Cacti simulator to produce the experimental results. Our experimental results show that ELRU-SEQ with skewed mapping function works well in reducing power consumption compared to other conventional data caches. [C1433]

"High speed digital filter design using minimal signed digit representation"

This paper presents the design and implementation of novel decimation filter structure for high speed asymmetric digital subscriber line (ADSL). Existing ADSL circuits use comb-FIR-FIR decimation filter structures, which have low throughput, more hardware and high power consumption. Unlike existing ADSL circuits, we design a novel high speed filter architecture and implement it using the minimal signed digit (MSD) representation. The MSD representation is suitable for common subexpression elimination, and it significantly reduces the number of adders required for the filter synthesis. Each digital-filter structure is simulated using Matlab, and its complete architecture is captured using DSP Blockset and Simulink. The resulting filter architecture has higher throughput, less hardware and consumes less power than the comb-FIR-FIR and comb-IIR-FIR architectures. The filter has been implemented on Xilinx FPGA using Virtex-2 technology. Compared to the comb-FIR-FIR and the comb-IIR-FIR architectures, the designed decimation filter architecture contributes to a hardware saving of 82% and 74%, respectively; in addition, it reduces the power dissipation by 91% and 79%, respectively. [C1434]

"Exploring the Energy-Time Tradeoff in MPI Programs on a Power-Scalable Cluster"

Recently, energy has become an important issue in highperformance computing. For example, supercomputers that have energy in mind, such as BlueGene/L, have been built; the idea is to improve the energy efficiency of nodes. Our approach, which uses off-the-shelf, high-performance cluster nodes that are frequency scalable, allows energy saving by scaling down the CPU. This paper investigates the energy consumption and execution time of applications from a standard benchmark suite (NAS) on a power-scalable cluster. We study via direct measurement and simulation both intra-node and inter-node effects of memory and communication bottlenecks, respectively. Additionally, we compare energy consumption and execution time across different numbers of nodes. Our results show that a power-scalable cluster has the potential to save energy by scaling the processor down to lower energy levels. Furthermore, we found that for some programs, it is possible to both consume less energy and execute in less time when using a larger number of nodes, each at reduced energy. Additionally, we developed and validated a model that enables us to predict the energy-time tradeoff of larger clusters. [C1435]

"Software-Directed Disk Power Management for Scientific Applications"

Disk power consumption is becoming an increasingly important issue in high-end servers that execute large-scale data-intensive applications. In particular, array-based scientific codes can spend a significant portion of their power budget on the disk subsystem. Observing this, the prior research proposed several strategies, such as spining down to low-power modes or adjusting the speed of the disk in lower RPM, to reduce power consumption on the disk subsystem. A common characteristic of most of these techniques is that they are reactive, in the sense that they make their decisions based on the disk access patterns observed during execution. While such techniques are certainly useful and the published studies reveal that they can be very effective in some cases, one can conceivably achieve better results by adopting a proactive scheme. Focusing on array-intensive scientific applications, this paper makes two important contributions. First, it presents a compiler-driven proactive approach to disk power management. In this approach, the compiler analyzes the application code and extracts the disk access pattern. It then uses this information to insert explicit disk power management calls in the appropriate places in the code. It also preactivates a disk (placed into the low-power mode) before it is actually needed to eliminate the potential performance impact of disk power management. The second contribution of this paper is a code transformation approach that can be used to increase the savings coming from a disk power management scheme (whether reactive or proactive). Our experimental results with several scientific application codes show that both the proactive disk power management approach and the disk layout aware code transformations are beneficial from both power consumption and execution time perspectives. [C1436]

"Reducing power consumption during TLB lookups in a PowerPC™ embedded processor"

We present a microarchitectural-level low-power translation lookaside buffer (TLB) design for embedded system applications. High-performance embedded processors with small micro-TLBs frequently encounter a large number of micro-TLB misses and many types of context switches such as internal and external interrupts. Context switches flush the micro-TLBs and therefore cause a number of unified-TLB accesses for address translation. Our method presents a microarchitecture wherein the power dissipation associated with unified-TLB accesses is minimized. In addition, our technique enables large process ID register sizes which can reduce the operating system software overhead. Our experiments using specINT 2000 benchmarks show that we obtain an average power saving of 36% in the content addressable memory (CAM) comparisons for these accesses. [C1437]

"TFT-LCD application specific low power SRAM using charge-recycling technique"

We propose a novel low power charge-recycling SRAM (CR-SRAM) for portable TFT-LCD applications. In portable TFT-LCD applications, low power considerations are becoming more important for longer battery lifetime. To reduce the power consumption in SRAMs, the source-line, connected to the source terminals of the driver MOSFETs, is controlled, so that it is zero in the active mode and has a positive bias voltage in the stand-by mode. However, the overhead power consumed during the control of source-line voltage is considerable due to the large capacitive load on the source-line. Applying a charge-recycling technique to the source-line allows reduction of the power dissipation of the source-biased SRAM. Moreover, by exploiting the sequential access pattern of the TFT-LCD memory, the proposed CR-SRAM can efficiently reduce the power dissipation of the control circuit for charge recycling. The proposed CR-SRAM is implemented in a 0.18 μm technology and shows 68% and 14% power reduction compared to conventional SRAM (CON-SRAM) and source-biased SRAM (SB-SRAM), respectively. We also evaluate the power consumptions under various temperatures and row driver clock frequencies. Experimental results show that the percentage of power savings due to charge recycling increases with the higher frequency and achieved a maximum of 25% at 250 MHz. [C1438]

"Power Saving in Regular Interconnection Networks Built with High-Degree Switches"

Nowadays, high-degree switches are available as building blocks of the interconnection network of clusters of PCs. An alternative to take advantage of the high number of switch ports is to connect every pair of switches through not only one but several links (this is known as link trunking in other environments). This extra connectivity can be exploited by using adaptive routing algorithms, thus improving network throughput and reducing network congestion. However with low traffic loads, all the links that compose the trunk link will not be utilized, but this idle links continue consuming power. Power consumption reduction techniques are being applied everywhere in computer systems and the interconnection network is not an exception, as its contribution is not negligible. In this paper, we present a mechanism that dynamically switches on and off network links as a function of traffic. It is specially targeted to those networks where trunk links are used. The mechanism can switch off any link, provided that network connectivity is guaranteed, (i.e. every pair of switches should be connected through at least one active link). Indeed, this restriction makes possible to use the same routing algorithm regardless the power saving actions taken, thus simplifying router design. Our simulation results show that the network power consumption can be greatly reduced, at the expense of some increase in latency.

Nevertheless, it is shown that the power reduction is always higher that this latency increase. [C1439]

"Improvement of power-performance efficiency for high-end computing"

Left unchecked, the fundamental drive to increase peak performance using tens of thousands of power hungry components will lead to intolerable operating costs and failure rates. Recent work has shown application characteristics of single-processor, memory-bound non-interactive codes and distributed, interactive Web services can be exploited to conserve power and energy with minimal performance impact. Our novel approach is to exploit parallel performance inefficiencies characteristic of non-interactive, distributed scientific applications, conserving energy using DVS (dynamic voltage scaling) without impacting time-to-solution (ITS) significantly, reducing cost and improving reliability. We present a software framework to analyze and optimize distributed power-performance using DVS implemented on a 16-node Centrino-based cluster. Using various DVS strategies we achieve application-dependent overall system energy savings as large as 25% with as little as 2% performance impact. [C1440]

"Energy saving dynamic source routing for ad hoc wireless networks"

In this paper, energy saving dynamic source routing (ESDSR) protocol is introduced to maximize the life-span of a mobile ad hoc network (MANET). Many theoretical studies show that energy consumption in MANET can be significantly reduced using energy-aware routing protocols compared to fixed-power minimum-hop routing protocols. Two approaches are broadly suggested for energy-aware routing protocols-transmission power control approach and load sharing approach. ESDSR integrates the advantages of those two approaches. In ESDSR, the routing decision is based on a load balancing approach. Once a routing decision is made, link by link transmit power adjustment per packet is done based on a transmit power control approach. We modified dynamic source routing (DSR) protocol to make it energy aware by a network simulator (network simulator-2 of University of California). The simulation results show that the proposed ESDSR can save energy up to 40% per packet and it can send 20 % more packets to destinations by spending the same battery power in compare to DSR. [C1441]

"Dynamic Power-Aware Scheduling Algorithms for Real-Time Task Sets with Fault-Tolerance in Parallel and Distributed Computing Environment"

At present, saving energy consumption of modern processors and fault tolerance become major concerns due to the fact that high power consumption increases heat dissipation, which leads to decreased reliability of systems. Similarly, the faults of running tasks also reduce the reliability of systems. The algorithms proposed in this paper are based on the policy of shortest-task-first and combined with other efficient techniques, such as shared slack reclamation and checkpoint. Consequently, not only real-time tasks can be completed before deadline, but also reduction of the global power consumption and fault-tolerance will be satisfied dynamically. In this paper, we present four algorithms to cope with scheduling independent task sets and task sets with precedence relationship in homogeneous and heterogeneous systems, respectively. Moreover, we present dynamic fault-tolerant algorithm. Compared to the efficient algorithms presented so far, our algorithms show lower communicational complexity and much better scheduling performance in terms of makespan and energy consumption. [C1442]

"Reducing power with performance constraints for parallel sparse applications"

Sparse and irregular computations constitute a large fraction of applications in the data-intensive scientific domain. While every effort is made to balance the computational workload in such computations across parallel processors, achieving sustained near machine-peak performance with close-to-ideal load balanced computation-to-processor mapping is inherently difficult. As a result, most of the time, the loads assigned to parallel processors can exhibit significant variations. While there have been numerous past efforts that study this imbalance from the performance viewpoint, to our knowledge, no prior study has considered exploiting the imbalance for reducing power consumption during execution. Power consumption in large-scale clusters of workstations is becoming a critical issue as noted by several recent research papers from both industry and academia. Focusing on sparse matrix computations in which underlying parallel computations and data dependencies can be represented by trees, this paper proposes schemes that save power through voltage/frequency scaling. Our goal is to reduce overall energy consumption by scaling the voltages/frequencies of those processors that are not in the critical path; i.e., our approach is oriented towards saving power without incurring performance penalties. [C1443]

"Variable bandwidth allocation scheme for energy efficient wireless sensor network"

Increasing the lifetime of wireless sensors is essential for the proliferation of wireless sensor networks in various environments. In this paper, the relationship between bandwidth and energy consumption is exploited to increase

the lifetime of the sensors. A variable bandwidth allocation scheme that uses time-frequency slot assignment is proposed to reduce the energy consumption of a collaborative sensor network which has large spatial variation in node density and event rates. To assign the time-frequency slots to the sensor network, a novel algorithm is presented, which results in significant energy savings over the conventional constant bandwidth allocation scheme. [C1444]

"A Dynamic-cluster Energy-aware Routing Algorithm Based on Neural Structure in the Wireless Sensor Networks"

The function of neural network of human beings is quite similar to that of the sensor network, which is a cluster of firmly related individual units performing a special function. According to the architecture of neural network, a dynamic-cluster energy-aware routing algorithm (DCEAR) has been proposed in this paper. The nodes on the network have adopted an active routing based on event awaking. Firstly, the event data dynamically elects a temporary cluster-header. Then the temporary cluster-header handles all the data it receives, and the handled data reflects the general instance of the region. In this way it has decreased the information that has to be forwarded and has reduced the energy consumption of the entire network. The backbone of the network is originated by genetic-tree algorithm. It will timely update the trunk of the genetic-tree in order to trade off the energy consumption of the whole network. So it has prolonged the lifetime of the network greatly. The result of our simulation indicates that it is a quite effective energy saving routing algorithm [C1445]

"A novel hardware implementation of MP3 decoder for low power and minimum chip size"

The structure presented in this paper is for the hardware implementation of MP3 decoder. The purpose is to achieve a controller IC with low power consumption, small chip size and flexible choice of peripheral flash memory. DSP is not required in this design, but a simple 8-bit microcontroller is used instead. The specific hardware circuits can lower the system frequency to save power, and some techniques are applied to reduce the embedded memory [C1446]

"Closed-loop adaptive supply voltage scaling controller for low-power embedded processors"

This paper describes a hardware controller that reduces active power consumption in standard cell ASICs by adaptively adjusting the supply voltage to varying performance requirements. The hardware controller is embedded on the same die as the application ASIC. It consists of a hardware performance monitor, control logic and a serial interface logic. These functions combine to form a closed-loop that regulates the speed of the application. The proposed scheme has been implemented in a video processor designed in a 0.18 μm standard CMOS process. Experimental results demonstrate operation over a wide frequency range of 6 MHz to 48 MHz and up to 60% power savings when compared to an open-loop scheme. [C1447]

"Low power SRAM design using charge sharing technique"

This paper describes a low-power write scheme by adopting charge sharing technique. By reducing the bit lines voltage swing, the bit lines dynamic power is reduced. The memory cell's static noise margin (SNM) is discussed to prove it is a feasible scheme. Simulation results show compare to conventional SRAM, in write cycle this SRAM saves more than 20% dynamic power [C1448]

"Codes reallocation and prediction for power efficiency in I-cache memory"

To reduce energy consumption of cache memories is an important problem since this component spends a large portion of energy in a microprocessor. This paper proposes a compiler predicted strategy that dynamically turns off those unused cache lines to save power in architecture level. In our algorithm, the object codes of programs are reallocated in memory address map according to the I-cache structure so that the working sets are reduced in the cache memory. In addition, a few special cache-scaling instructions (CSIs) are added to the object codes to track the working set size. With the information from CSIs and the current system state, a hardware controller implements the decision of replacement algorithm and switching the power of each refill-line. Our experimental results indicate that the compiler-predicted algorithm can reduce 58.9% of energy in a 32K I-cache, while the average performance loss is only 2.7% [C1449]

"FSM decomposition for power gating design automation in sequential circuits"

Power gating is one of the most effective techniques for low power design because it reduces both dynamic and static power simultaneously. This paper proposes a circuit architecture to implement power gating in sequential circuits based on finite state machine (FSM) decomposition, which is implemented by partition the state transition graph (STG). The FSM is partitioned into two or more sub-machines, only one of which is active most

of the time, and the power supply of other sub-machines can be cut off to save energy. Since adjustment of supply voltage may not finish instantly, the voltage of the submachine that will be activated need to be raised ahead of time, which makes the problem complicated. We propose a simulated annealing algorithm to perform the decomposition without timing penalty. Experimental results have shown the effectiveness of our approach, and it is expected that power gating will show superior power saving to clock gating due to the increasing significance of static power. [C1450]

"A compiler-controlled instruction cache architecture for an embedded low power microprocessor"

Modern microprocessors have been improving their performance with deeper sub-micron technologies and larger on-chip cache memories. This trend leads to a dramatic increment of power consumption in such units and has prompted researchers to develop power efficient caches. Here we propose a method that dynamically turns off those unused cache lines to save power at architecture level. In our algorithm, the object codes of programs are reallocated in memory address map so that the working sets are reduced when they are loaded into I-cache. In addition, a few special cache-scaling instructions (CSIs) are added to the object codes to track the working set sizes. With the information from CSIs and the current system state, a hardware controller implements the decision of caching instructions and scales the size of cache memory. Experimental results using popular Windows-based applications show that the compiler-controlled resizable cache can reduce 55.8% of energy in a 32K I-cache with only 2.9% of performance degradation on average. [C1451]

"A hybrid static/dynamic DVS scheduling for real-time systems with (m, k)-guarantee"

Energy reduction is critical to increase the mobility and to extend the mission period in the development of today's pervasive computing systems. On the other hand, however, energy reduction must be subject to the requirements not to compromise the quality of service (QoS) that these systems need to provide. While most of the current research in energy-aware real-time scheduling has been focused on hard real-time systems, a large number of practical applications and systems exhibit more soft real-time nature. In this paper, we study the problem of minimizing energy for soft real-time systems with the requirements of QoS-guarantee. The QoS requirements are deterministically quantified with the (m, k)-constraints, which require that at least m out of any k consecutive jobs of a task meet their deadlines. To deal with the dynamic characteristics of such applications and systems, we propose a hybrid static/dynamic scheduling approach that can efficiently reduce the energy consumption while guaranteeing the (m, k)-constraints. The experimental results demonstrate that our proposed techniques outperform previous research significantly in terms of both the energy savings and QoS that can be achieved [C1452]

"Using cache to reduce power in content-addressable memories (CAMs)"

We propose using caching to save power in content-addressable memories (CAMs). By using a small cache along with the CAM, we avoid accessing the larger and higher power CAM. For a cache hit rate of 90%, the cache-CAM (C-CAM) saves 80% power over a conventional CAM, for a cost of 15% increase in silicon area. Even at a low hit rate of 50%, a power savings of 40% is achieved. The proposed C-CAM is employed in the design of a testchip demonstrating a 2.6 fJ/bit/search in a 0.18 mum CMOS process [C1453]

"Power Consumption Monitoring System for Personal Computers by Analyzing Their Operating States"

We focused on reducing the power consumption of information and communication technology (ICT) products as an effective measure because power consumption has expanded rapidly as these products have spread through offices and homes. A low motivation to save power is one reason preventing reduction in the power consumption of these products is considered. Therefore a system that monitors and displays the power consumption of ICT products by analyzing their operating states is developed. This system will enable more users to take advantage of power saving functions as the system requires no additional devices for measuring power consumption because it is completely implemented with software. Moreover, this system should motivate users to reduce power consumption by providing power consumption information [C1454]

"Energy Saving Refrigeration System for Supermarket"

The energy saving refrigeration system that is composed of a condensing unit and the refrigerated display cases has been developed. In this system, the DC inverter compressor controls the evaporating temperature and linear expansion valves control superheat at the outlet of evaporators in the refrigerated display cases. The target value of the evaporating temperature is calculated from the temperature difference between the refrigerated display cases and those cooling targets. The target value of superheat is set at 8 degrees that is the best value for energy conservation of the R404A refrigeration system. In this way, the electric power consumption of the

refrigeration system is reduced by 31% in comparison with the conventional system [C1455]

"Energy efficient multi-resolution visual surveillance on wireless sensor networks"

Visual surveillance with a distributed ad hoc sensor network enable reliable monitoring and control of a variety of applications that range from civil to military. However, due to the large volume of multimedia data associated with visual sensors, the surveillance scheme has to be architected with a goal of energy conservation and extending life expectancy. In this paper, we briefly discuss the computation and communication energy costs associated with a sensor node and explore the possibilities of extending battery life by choosing to perform local processing. We propose a discrete wavelet transform (DWT) based multi-resolution surveillance schema designed to reduce power requirement. We then compare and contrast the computational and communication power expended by a traditionally used JPEG-based scheme and illustrate the significant power savings achieved by the proposed surveillance system [C1456]

"High Speed Direct Digital Frequency Synthesizer(DDFS) Architecture With Reduced ROM Structure"

A low-power, high speed direct digital frequency synthesizer (DDFS) is presented. Some approximations are used to avoid using a large ROM look-up table to store the trigonometric values in a conventional DDFS. Significant saving in power consumption, due to the compressed ROM, renders the design more suitable for portable wireless communication applications. To demonstrate the proposed technique, a DDFS has been implemented using useful trigonometric equations. The spurious-free dynamic range is about 60 dB at low synthesized frequencies. [C1457]

"A low power baseband filter for DRM receivers"

In this paper, we proposed a design that is suitable for the VLSI implementation of digital filters in the digital radio mondiale (DRM) receivers. By using frequency-response masking (FRM) technique, the sequential quadratic programming (SQP) optimization method, and signed power-of-two (SPT) representation, the proposed filter not only achieved more savings in terms of multipliers, but also reduced the terms of coefficients word length in the filters. The VLSI implementation result shows that the proposed filter for mode C reaches the saving of 16% in power consumption and 77% in area cost compared with the conventional direct-form filter [C1458]

"Design of combinational logic digital circuits using a mixed logic synthesis method"

The main contribution of this paper is the proposition of a technology independent low power synthesis procedure at the logic (gate) level for combinational logic digital CMOS circuits without reconvergent fan-out nodes, implementing adjacent and/or non-adjacent Boolean functions. While many papers have been published describing power-saving techniques, trade-offs between the different design metrics are rarely discussed. In this paper, this issue is being addressed by means of a combined optimization parameter viz. Figure of merit (FoM), for evaluating the quality of logic circuits designed. The goal is to decrease the power consumption and simultaneously improve the overall figure of merit. Since the power dissipated by a combinational logic circuit is mainly dictated by the switching activities of all signals associated with the circuit, the main focus has been on reducing the signal activities to the minimal level required. A novel mathematical formulation has also been developed for a unique classification of gates. Experimental results obtained on the basis of the proposed strategy for 0.5-µm CMOS technology, report minimization in average power consumption by about 36.1 %, along with a substantial improvement in FoM to the tune of nearly 45.7 % on an average. [C1459]

"Power-composition profile driven co-synthesis with power management selection for dynamic and leakage energy reduction"

Recent research has shown that the combination of dynamic voltage scaling (DVS) and adaptive body biasing (ABB) yields high energy reductions in embedded systems. Nevertheless, the implementation of DVS and ABB requires a significant system cost, making it less attractive for many small systems. In this paper we demonstrate that it is possible to reduce this system cost and to achieve comparable energy saving to that obtained using combined DVS and ABB scheme through a co-synthesis methodology which is aware of the tasks' power-composition profile (the ratio of the dynamic power to the leakage power). In particular, the presented methodology performs a power management selection at the architectural level, i. e., it decides upon which processing elements to be equipped with which power management scheme (DVS, ABB, or combined DVS and ABB)-with the aim to achieve high energy savings at a reduced implementation cost. The proposed technique maps, schedules, and voltage scales applications specified as task graphs with timing constraints. Detailed

experiments including a real-life benchmark are conducted to demonstrate the effectiveness of the proposed methodology. [C1460]

"Simultaneous memory and bus partitioning for SoC architectures"

There has been a continued proliferation in the demand for application specific system on chip cores in the recent years. Meeting the power budget constraint continues to be a major challenge for the designers architecting such systems. In this work, we demonstrate that simultaneous partitioning of the bus and memory subsystem into smaller segments can be an effective mechanism for reducing the energy consumption of a SoC. We present a genetic algorithm based search mechanism to determine a system configuration that is energy-efficient and validate the effectiveness of the configuration using a cycle-accurate virtual platform for a multiprocessor SoC. Our results using various applications show that the proposed approach gives significant energy savings and accentuates the benefits of previously proposed bus and memory partitioning schemes applied individually or in combination. [C1461]

"Workload Clustering for Increasing Energy Savings on Embedded MPSoCs"

Voltage/frequency scaling and processor low-power modes (i.e., processor shut-down) are two important mechanisms used for reducing energy consumption in embedded MPSoCs. While a unified scheme that combines these two mechanisms can achieve significant savings in some cases, such an approach is limited by the code parallelization strategy employed. In this paper, we propose an integer linear programming (ILP) based workload clustering strategy across parallel processors, oriented towards maximizing the number of idle processors without impacting original execution times. These idle processors can then be switched to a low power mode to maximize energy savings, whereas the remaining ones can make use of voltage/frequency scaling. In order to check whether this approach brings any energy benefits over the pure voltage scaling based, pure processor shut-down based, or a simple unified scheme, we implemented four different approaches and tested them using a set of eight array/loop-intensive embedded applications. Our simulation-based analysis reveals that the proposed ILP based approach: (1) is very effective in reducing the energy consumptions of the applications tested; and (2) generates much better energy savings than all the alternate schemes tested (including a unified scheme that combines voltage/frequency scaling and processor shutdown) [C1462]

"Novel 7T sram cell for low power cache design"

Low-power on-chip cache is a crucial part in many applications. Conventional write operation depends on discharging/charging large bit lines capacitance which causes high power consumption. We propose a 7T SRAM cell that only depends on one of the bit lines during a write operation and reduce the write power consumption. HSPICE simulation shows that at least 49% write power saving, higher stability, and no performance degradation with additional 12.25% silicon area [C1463]

"Feedback scheduling of real-time control tasks in power-aware embedded systems"

Power awareness has become a critical issue in real-time scheduling of embedded systems. In the context of control applications, the goal of high control performance and low energy consumption are at odds with each other. While dynamic voltage/frequency scaling (DVS) has proved to be promising in energy saving while preserving task schedulability, traditional DVS algorithms use either open loop or ad hoc solutions, and hence cannot perform well for dynamic systems where the workload varies significantly. By targeting these systems, a novel scheme, namely DVS-FS, which combines DVS and feedback scheduling, is suggested. The objective is to save CPU energy as much as possible, while still providing control performance guarantees, which largely depends on successful schedule of the control task set. DVS-FS exploits feedback control methodology, and facilitates tradeoffs between energy consumption and control performance through controlling the CPU utilization at a considerably high level. Simulation experiments demonstrate that DVS-FS can easily reduce significant energy consumption at the expense of only minor control performance degradation. [C1464]

"A Compiler-Directed Energy Saving Strategy for Parallelizing Applications in On-Chip Multiprocessors"

As energy consumption becomes one of the key optimization objects in on-chip multiprocessor, compiling a parallelizing application combined with energy saving strategy is more significant. In this paper, we focus on an on-chip multiprocessors architecture, where each processor in on-chip multiprocessor can independently adjust its frequency and voltage for energy savings. Given an array-intensive application, we simulate parallelizing application and analyze probable load imbalance; then our energy saving strategy determines each processor's clock frequency and voltage level fit for each parallel fragment in terms of load imbalance. Here, parallel fragments mainly denote parallel loop nests. Further, we consider the serial code fragments as a severe load-

unbalanced parallel partitioning when the redundant processors can be shut down. Initial experiment proves our energy saving strategy is successful in reducing the energy consumption of the parallel programs [C1465]

"Performance-constrained Distributed DVS Scheduling for Scientific Applications on Power-aware Clusters"

Left unchecked, the fundamental drive to increase peak performance using tens of thousands of power hungry components will lead to intolerable operating costs and failure rates. High-performance, power-aware distributed computing reduces power and energy consumption of distributed applications and systems without sacrificing performance. Generally, we use DVS (Dynamic Voltage Scaling) technology now available in high-performance microprocessors to reduce power consumption during parallel application runs when peak CPU performance is not necessary due to load imbalance, communication delays, etc. We propose distributed performance-directed DVS scheduling strategies for use in scalable power-aware HPC clusters. By varying scheduling granularity we can obtain significant energy savings without increasing execution time (36% for FT from NAS PB). We created a software framework to implement and evaluate our various techniques and show performance-directed scheduling consistently saves more energy (nearly 25% for several codes) than comparable approaches with less impact on execution time (< 5%). Additionally, we illustrate the use of energy-delay products to automatically select distributed DVS schedules that meet users' needs. [C1466]

"Just In Time Dynamic Voltage Scaling: Exploiting Inter-Node Slack to Save Energy in MPI Programs"

Recently, improving the energy efficiency of HPC machines has become important. As a result, interest in using powerscalable clusters, where frequency and voltage can be dynamically modified, has increased. On power-scalable clusters, one opportunity for saving energy with little or no loss of performance exists when the computational load is not perfectly balanced. This situation occurs frequently, as balancing load between nodes is one of the long standing problems in parallel and distributed computing. In this paper we present a system called Jitter, which reduces the frequency on nodes that are assigned less computation and therefore have slack time. This saves energy on these nodes, and the goal of Jitter is to attempt to ensure that they arrive "just in time" so that they avoid increasing overall execution time. For example, in Aztec, from the ASCI Purple suite, our algorithm uses 8% less energy while increasing execution time by only 2.6%. [C1467]

"Cross-layer protocols for energy-efficient wireless sensor networking"

The Army's next generation distributed sensor networks provide stand-off situational awareness for future troops. A major factor for the performance and lifecycle of these sensor networks is their ability to conserve battery power. As advances in RF components reach the physical limits of energy efficiency, new network protocols operating at the link layer and above hold the greatest opportunities for additional improvements in energy efficiency. Recently, a number of power-saving solutions have been proposed that separately consider power-consumption of media access control (MAC) scheduling and routing algorithms, but have not considered the potential benefit of cross-layer optimization across these algorithms. In this paper, we present an approach that integrates pseudo-dynamic scheduling at the link-layer with diversity routing at the network-layer. The link-layer protocol also provides detailed control of the physical-layer's radio state. Our work focuses on reducing the energy loss due to idle listening, control signaling, congestion hot-spots, and packet collisions. We present analytical and simulation results that demonstrate the increased energy efficiency of this class of cross-layer protocols examine the throughput and latency impacts and define how parameters should be set to optimize the end-to-end performance. We anticipate that the technology presented here will have broad application to army sensor networks as well as public commercial wireless systems and plant automation [C1468]

"Reduced pull-in time of phase-locked loops with a novel nonlinear phase-frequency detector"

A novel nonlinear phase-frequency detector (PFD) is presented to achieve a fast-switching phase-locked loop (PEE) based frequency synthesizer. Compared with the conventional nonlinear PFD, the proposed topology can further reduce the PEE acquisition time while the loop stability remains unchanged. Moreover, the new topology can decrease the capacitance value and the charge-pump current to 1/k of a conventional one as the loop bandwidth increases k times, thus saving substantial chip area and power consumption. [C1469]

"Energy savings by intelligent interface idling in 802.11 based wireless networks"

In this paper we propose and analyze a new interface idling mechanism for improving carrier-sense energy expenditure of IEEE 802.11 based wireless network interfaces. A novel protocol state analysis technique is developed for detecting time windows during which a node consumes energy due to erroneous carrier sensing.

During this window, energy savings at the MAC layer is accomplished by forcing a wireless interface to a relatively low-energy idling state. At the end of this window, an interface is transitioned back to its regular receiving mode. Energy savings are realized by exploiting the difference in power consumption between the erroneous carrier sensing state and the idling state. We evaluate the proposed protocols using ns-2 simulator. Simulation experiments demonstrate that the proposed mechanisms are capable of significantly reducing erroneous carrier sensing expenditure for newer generation of 802.11 cards that support low-energy idling modes as described above. Our experimentation with Socket Communication Inc.'s low power 802.11 card demonstrate that the reduction in combined overhearing and erroneous carrier sensing expenditure can be up to 62% and can extend network life by up to 154%. Results also show that the proposed MAC layer idling is fairly insensitive to mobility [C1470]

"Energy macro-modeling of embedded microprocessor using SystemC"

System-on-chip (SoC) is increasingly adopted in VLSI world with the advancing silicon technologies. Integrating multiple functional IPs (intellectual property) onto a single die increases performance and saves power consumption by reducing interconnecting capacitance among these IPs. Embedded microprocessor acts as the central controlling unit of many SoCs to orchestrate all the other IPs to work harmoniously. Low and predictable energy consumption is often required for these systems. This paper proposes an empirical macro-modeling methodology allowing energy modeling at the system level. High-level macro-operations are characterized for energy consumption. This modeling framework is implemented for a MIPS-family microprocessor using SystemC, a system-level modeling and simulation environment. Using the JPEG encoder application as case study, a simulation speed-up of more than 200 times with the relative error of -6.70% on energy estimation is achieved compared to instruction-level simulators. Meanwhile, this model provides support to multiprocessor energy modeling, which is unavailable currently in the instruction-level energy simulators [C1471]

"A simplistic technique for power factor compensation capacity calculation in medium size industry"

There are a variety of techniques developed in order to improve the efficiency of electrical systems and reduce cost of providing electricity to the consumer. In this paper, a simplistic technique for power factor capacity calculation in medium-sized industrial/commercial setups is presented. Various loads of similar nominal power factor are categorized and demand factor of loads is so selected that it has engineering justifications. The proposed system works on principle of low voltage power factor correction, which substantially reduces electricity bill and increases electrical system loading capacity. It allows commercial and industrial consumers to save on their power cost appreciably. This work is augmented by application software, which takes a few inputs and produces numerous useful results. Adoption of this system helps user in computing compensation capacity, system KVA (size of transformer) and cost of compensation. A feature of this system is prediction of low PF penalty. Moreover, it also suggests the tentative payback period [C1472]

"An efficient Viterbi decoder design for DMB receiver"

The efficient Viterbi decoder that supports full data-rate output of DMB system was proposed. In this paper, SST scheme was adopted for Viterbi decoder with puncturing to reduce the power consumption. Puncturing vector tables are modified and re-arranged to be designed by hardwired logic to save the system area. New re-scaling scheme is proposed and the proposed re-scaling scheme optimizes the wordlength of path metric memory and greatly reduces the computational load for re-scaling by controlling MSB of path metric memory. Another saving of computation is done by proposed algorithm for branch metric calculation, which makes use of pre-calculated metric values. The designed Viterbi decoder was synthesized using SAMSUNG 0.35u standard cell library and occupied small area and showed low power consumption. [C1473]

"Aggregating processor free time for energy reduction"

Even after carefully tuning the memory characteristics to the application properties and the processor speed, during the execution of real applications there are times when the processor stalls, waiting for data from the memory. Processor stall can be used to increase the throughput by temporarily switching to a different thread of execution, or reduce the power and energy consumption by temporarily switching the processor to low-power mode. However, any such technique has a performance overhead in terms of switching time. Even though over the execution of an application the processor is stalled for a considerable amount of time, each stall duration is too small to profitably perform any state switch. In this paper, we present code transformations to aggregate processor free time. Our experiments on the Intel XScale and Stream kernels show that up to 50,000 processor cycles can be aggregated, and used to profitably switch the processor to low-power mode. We further show that our code transformations can switch the processor to low-power mode for up to 75% of kernel runtime, achieving up to 18% of processor energy savings on multimedia applications. Our technique requires minimal architectural

modifications and incurs negligible ([C1474]

"An efficient direct mapped instruction cache for application-specific embedded systems"

Caches may consume half of a microprocessor's total power and cache misses incur accessing off-chip memory, which is both time consuming and energy costly. Therefore, minimizing cache power consumption and reducing cache misses are important to reduce total energy consumption of embedded systems. Direct mapped caches consume much less power than that of same sized set associative caches but with a poor hit rate on average. Through experiments, we observe that memory space of direct mapped instruction caches is not used efficiently in most embedded applications. We design an efficient cache-a configurable instruction cache that can be tuned to utilize the cache sets efficiently for a particular application such that cache memory is exploited more efficiently by index remapping. Experiments on 11 benchmarks drawn from Mediabench show that the efficient cache achieves almost the same miss rate as a conventional two-way set associative cache on average and with total memory-access energy savings of 30% compared with a conventional two-way set associative cache. [C1475]

"A 3-mW, 270-Mbps, Clock-Edge Modulated Serial Link for Mobile Displays"

In this paper, a single channel clock-edge modulated serial link for mobile display interface is presented. Clock edge modulation (CEM) enables all necessary signals between a graphic processor and a LCD timing controller to be transferred over a single, DC-balanced differential channel, thus greatly saving the power and costs of the existing parallel lines. A simple DLL-based CEM decoder is described that recovers the data with low power consumption and high jitter tolerance. The use of a voltage-mode driver and a single-side termination further reduces the power. A prototype CEM transceiver was implemented in a 0.18mum CMOS process and dissipates 3.12mW when operating at 270-Mb/s and 1.2V [C1476]

"Design Exploration of a Spurious Power Suppression Technique (SPST) and Its Applications"

This paper presents the design exploration and application of a technique to suppress the spurious power dissipation existed in the data-paths for multimedia VLSI designs. The proposed technique adopts the design concept of separating the arithmetic units into most significant part (MSP) and least significant part (LSP), and then freezing the MSP whenever this part of circuits does not affect the computation result. This paper first explores three implementation approaches of realizing the SPST-based design concept to decide the most efficient one, and then uses this approach to reduce the spurious power of the multi-transform coding design in H.264 systems. The post-layout simulations show that the proposed SPST can save average 27.38% of power dissipation of the multi-transform design [C1477]

"The Split-Path AND-type Match-line Scheme for Very High-Speed Content Addressable Memories"

The proposed split-path AND-type non-pipelined match-line scheme achieves over 50% search speed improvement compared to the pipelined NOR-type current-saving controlled match-line scheme (Pagiamtzis et al., 2004). The highest world record of 1.6 ns search speed can also be traded for power saving by adopting voltage scaling. When the supply voltage is reduced to a level so that the energy efficiency of both kinds of design is almost equal, the new scheme still has 18% speed improvement over the conventional design. The authors also found that the new design has a smaller area compared to the conventional NOR-type design [C1478]

"A summary of the complex behaviour from simple power conserving protocols"

In this paper we examine the complex behavior that emerges from the implementation of an energy-aware system using a simple transmission power control algorithm that exploits overheard MAC-level information to reduce a device's energy consumption. We evaluate this simple algorithm using two radio systems and show that, in spite of the complexity, energy savings can be obtained using a scheme that takes advantage of overheard information [C1479]

"A Feasibility Analysis of Power Awareness in Commodity-Based High-Performance Clusters"

We present a feasibility study of a power-reduction scheme that reduces the thermal power of processors by lowering frequency and voltage in the context of high-performance computing. The study revolves around a 16-processor Opteron-based Beowulf cluster, configured as four nodes of quad-processors, and shows that one can easily reduce a significant amount of CPU and system power dissipation and its associated energy costs while still maintaining high performance. Specifically, our study shows that a 5% performance slowdown can be traded

off for an average of 19% system energy savings and 24% system power reduction. These preliminary empirical results, via real measurements, are encouraging because hardware failures often occur when the cluster is running hot, i.e, when the workload is heavy, and the new power-reduction scheme can effectively reduce a cluster's power demands during these busy periods [C1480]

"A theoretical framework on power consumption subject to information accuracy in wireless sensor networks"

Wireless sensor networks (WSNs) are characterized by dense tiny sensors that have only limited energy supply. One of the major challenges in constructing such networks is to achieve the pre-defined information accuracy while maintain long network lifetime. Therefore, a fundamental question is what is the lower bound for the power consumption of a sensor network collecting data subject to the pre-defined information accuracy. In this paper, we investigate the spatial correlation of sensor observations to model information accuracy. A theoretical framework is developed to model the power consumption for pre-defined information accuracy in WSNs. With a random sensor deployment, our analysis shows that the pre-defined information accuracy can be achieved with only a limited number of sensors jointly sensing the same event. Hence, a great of power of the whole network can be saved to prolong the network lifetime. Our results can be utilized in designing effective sensor scheduling algorithms to reduce energy consumption while maintain the predefined information accuracy [C1481]

"Power islands: a high-level synthesis technique for reducing spurious switching activity and leakage"

This work introduces a high-level synthesis (HLS) methodology that eliminates the spurious switching activity (SSA) and the leakage in a great portion of the resulting circuit through the use of power islands. A power island is a cluster of logic whose power can be controlled independent from the rest of the circuit, and hence can be completely powered down when all of the logic contained within it is idling. By powering down an island: (1) the spurious switching that results from the broadcast to idle components is silenced and (2) the power consumption due to leakage in inactive components are eliminated. Our experiments conducted on several synthesis benchmarks using a transistor-level simulator showed an average reduction of 11% in total power consumption due to the power islands without introducing any overhead. We can project that in future technologies, when leakage becomes a more dominant component of the overall power, significantly more savings can be gained from design with power islands [C1482]

"Utilization based duty cycle tuning MAC protocol for wireless sensor networks"

In this paper, we propose U-MAC, a medium access control protocol designed for wireless sensor networks. Nowadays, wireless sensor network are formed by a great quantity of sensor nodes, which are generally battery-powered and may not recharge easily. Consequently, how to prolong the lifetime of the nodes is an important issue while designing a MAC protocol. However, lowering the energy consumption may result in higher latency. Addressing on such tradeoff, U-MAC balances the tradeoff by utilization based tuning of duty cycle and selective sleeping after transmission. The experiment results show that our proposed U-MAC saves energy about 43% and reduce latency by 65% from S-MAC in a chain topology. In the cross topology, U-MAC also achieves 32% energy saving and 45% latency reduction from S-MAC [C1483]

"A low-power termination criterion for iterative LDPC code decoders"

This paper introduces a novel criterion for the termination of iterations in iterative LDPC Code decoders. The proposed criterion is amenable for VLSI implementation, and it is here shown that it can enhance previously reported LDPC code decoder architectures substantially, by reducing the corresponding power dissipation. The concept of the proposed criterion is the detection of cycles in the sequences of soft words. The soft-word cycles occur in some cases of low signal-to-noise ratios and indicate that the decoder is unable to decide on a codeword, which in turn results in unnecessary power consumption due to iterations that do not improve the bit error rate. The proposed architecture terminates the decoding process when a soft-word cycle occurs, allowing for substantial power savings at a minimal performance penalty. The proposed criterion is applied to hardware-sharing and parallel decoder architectures. [C1484]

"Control of Rubber Tyred Gantry Crane with Energy Storage Based on Supercapacitor Bank"

This paper proposes a hybrid energy system, which consists of a diesel-engine generator and a supercapacitor, for improving performance of a rubber tyred gantry crane (RTGC). The supercapacitor contributes to the energy recovery associated with regenerative braking in 'hoist-down' braking operation and to the rapid energy consumption related with acceleration in 'hoist-up' operation of the RTGC. Hence it does save energy, which is

conventionally wasted by a braking resistor. In addition, the large engine generator is replaced by the much smaller one, for the supercapacitor reduces high power demands away from it. For power conversion between the supercapacitor and the DC link, a 3 legs bidirectional DC-DC converter, which has the same structure as the commercially available 3-phase inverter, is used. Two kinds of simulations are performed to study the behaviors of the proposed system under the worst operating conditions. The performance of the proposed hybrid energy system is evaluated through several experiments with a real RTGC [C1485]

"Design of a 4-bit 1.4 Gsamples/s low power folding ADC for DS-CDMA UWB transceivers"

In this paper, we present a CMOS low power folding ADC (analog to digital converter) architecture, which takes advantage of the low resolution requirement of DS-CDMA UWB transceivers to reduce the power consumption. The high sampling rate is achieved by adopting current steering folding amplifiers instead of cross coupled differential pair based folding amplifiers. Our ADC adopts both resistive interpolation and multiplication to fold the input signal, thereby, reducing the number of folding amplifiers required. When this technique is applied to higher resolution converters, the power and area savings will be even more significant. A brief analysis on the operation of the folding amplifier and a systematic method for sizing preamplifiers, folding amplifiers and comparators is presented. The ADC has been designed in 0.13 μm IBM CMOS process. Post layout simulation shows that the spurious free dynamic range (SFDR) of our ADC is greater than 24 dB up to 540 MHz at 1.4 GS/s and consumes about 62 mW of power. The results also indicate that the proposed architecture consumes less power and achieves a higher sampling rate than existing folding ADCs. [C1486]

"Bounded clustering with low node-clusterhead separation in wireless sensor networks"

Clustering is an important technique for distributed coordination in sensor networks. Clusters of bounded size are of special interest for their effectiveness in reducing energy consumption by limiting the neighborhood of a node. Further energy saving can be achieved by reducing the average node to clusterhead separation as it allows nodes to transmit at lower power. In this paper, we propose a bounded clustering algorithm which reduces the average node-clusterhead separation for energy-efficient communication. Extensive simulation results show that the algorithm generates bounded clusters where average node-clusterhead separation is low. In addition, for about 80% of the nodes, the actual separation is less than the average. [C1487]

"Reducing idle mode power consumption of cellular/VoWLAN dual mode mobiles"

The integration of cellular and voice over WLAN (VoWLAN) systems recently has attracted considerable interest from both academia and industry. A cellular/VoWLAN dual mode system helps mobile users to access a low cost voice over IP (VoIP) service in a WLAN area and switch to a wide-coverage cellular system without WLANs. However, the system suffers the power consumption problem and the service continuity issue between cellular and WLAN systems. This study presents a network architecture for an enterprise or a dual mode service provider to permit service continuity between cellular and VoWLAN systems. This architecture is used as a basis for further elaborating a novel power saving mechanism, called PIANO (paging via another radio). By applying the proposed mechanisms to a dual mode mobile, the mobile can completely switch off its WLAN interface, only leaving the cellular interface awake to listen to paging signals. When a dual mode mobile receives a paging message from its cellular interface, it wakes up its WLAN interface and responds to the call via WLAN networks. Therefore, a dual mode mobile can reduce the idle mode power consumption, and can also obtain VoWLAN services. The simulation results illustrate that the proposed methods significantly extend the standby hours of a dual mode mobile [C1488]

"Adiabatic 4-2 compressors for low-power multiplier"

This paper presents two adiabatic 4-2 compressors with complementary pass-transistor logic (CPAL). One is based on basic CPAL gates, while the other is realized using CPAL full adders. The architecture of an 8Ч8-bit adiabatic multiplier using adiabatic 4-2 compressors is described. The proposed compressors are verified using 0.25μm TSMC CMOS process. The power consumption is significantly reduced, because the non-adiabatic energy loss of output loads has been eliminated using complementary pass-transistor logic for evaluation and transmission gates for energy-recovery. The simulation results show that the compressor using CPAL full adders consumes about 60% of the dissipated energy of the compressor using CPAL basic gates at 100MHz. Compared to the conventional CMOS implementation, the CPAL compressor attains energy savings of 85% to 95% for clock rates ranging from 25 to 150 MHz. [C1489]

"A low power decomposed hierarchical multiplier architecture embedding multiplexer based full adders"

This paper proposes a novel 4times4 multiplier architecture which is efficient in terms of power without a

significant increase in delay and area, especially designed for partition multipliers having a partition size of 4. The idea involves the generation of partial products in parallel using AND gates. The addition of these partial products will take log2 (2N), which in this case would take 3 steps since, the operand width N is 4. In the proposed multiplier, computation is divided into hierarchical levels saving significant amount of power, since, power is provided only to the level that is involved in computation and thereby rendering the remaining two levels inactive. In order to further reduce the power consumption, the proposed 4times4 multiplier architecture uses the recently proposed low-power multiplexer-based 1-bit full adder. To further improve on the power efficiency, novel 6 transistors half adder architecture is proposed. Furthermore, a low power AND gate is also designed for generation of partial products [C1490]

"Code compression combined with low-power encoding"

Compressing code is known to be one of the most effective methods of reducing the energy consumed in the interface between memory and processor. In this paper, we address the problem, which has not been tackled in the previous code compression techniques, of determining binary code of the instructions to be compressed. Our observation is that a careful assignment of binary code to the instructions to be compressed can lead to a considerable amount of power saving since the switching activity in instruction accesses varies significantly depending on the ways of assigning binary code to the instructions. To achieve the power saving, we analyze the problem and transform it into a graph optimization problem and solve it effectively by inventing an incremental node covering technique. From experiments using a set of benchmark programs, it is shown that the approach is quite effective, producing code with 17.3%-27.1% less power consumption in instruction accesses over a greedy (Gray-code based) low-power binary code assignment [C1491]

"A Combined Wide and Narrow Pulse Generators for Processing Microbes"

This paper proposes a wide pulse combined with narrow pulse generator for solid food sterilization. The proposed generator is composed of a full-bridge converter in phase-shift control to generate high dc-link voltage, and a full-bridge inverter associated with an L-C network and a transformer to generate wide pulses combined with narrow pulses. These combined pulses can prevent undesired strong air arcing in free space, reduce power consumption and save power components, while can sterilize food effectively. The converter and inverter can be operated at high frequencies and with PWM control, thus its weight and size can be reduced significantly and its efficiency can be correspondingly improved. Experimental results obtained from a prototype with plusmn10 kV wide pulses combined with plusmn10 kV narrow pulses and with 10 ~ 50 kW peak output power, depending on pulse width of the output pulses, have demonstrated its feasibility [C1492]

"Temperature dependent leakage power characteristics of dynamic circuits in sub-65 nm CMOS technologies"

The temperature dependent subthreshold and gate oxide leakage power characteristics of domino logic circuits are evaluated in this paper. The preferred input vectors and node voltage states that minimize the total leakage power consumption are identified at the lower and upper extremes of a typical die temperature spectrum. New low leakage circuit design guidelines are presented based on the results. The significantly increased gate dielectric tunneling current, as described in this paper, dramatically changes the leakage power characteristics of dynamic circuits in the sub-65nm CMOS technologies. Furthermore, the leakage power savings provided by the dual threshold voltage domino logic circuit techniques are all together reduced due to the significance of the gate dielectric tunneling in the nanometer CMOS technologies [C1493]

"Simultaneous capacitor sharing and scaling for reduced power in pipeline ADCs"

A technique for reducing power dissipation in pipeline analog-to-digital converters (ADCs) is presented. The technique stems from the observation that the amplifier of the first stage is used to charge the input capacitors of the subsequent stage. At the end of the amplification phase, the feedback capacitor of the first stage holds the residue voltage across it and can be reused in the second stage. The feedback capacitor is designed to be a network of capacitor and switches. With appropriate clocking, the network is re-configured to form the input sampling network of the second stage. This reuse is combined with scaling down of the capacitors to result in more power savings [C1494]

"Precharged SRAM cell for ultra low-power on-chip cache"

This paper proposes an ultra low-power technique to reduce dynamic and leakage power in SRAM. At write mode, the technique reduces the voltage swing required on the bit lines and depends on the cell itself to amplify the small swing to full swing. HSPICE simulation shows 94.2% write power saving in 0.18nm technology. On the

sleep mode, the proposed cell reduces the leakage current by 60% for 70nm technology. [C1495]

"SPRTs in sensor networks with mobile agents"

We assume a detection network engaged in the task of sequentially testing simple Gaussian hypotheses. The network architecture follows the SENMA paradigm but, as opposed to the usual assumptions, the mobile agent (rover) implements continuous-time polling. This, along with a Poisson random field model for the sensor locations (which are completely unknown to the rover), allows us to avoid channel collision concerns. The remote sensors employ Wald sequential tests (SPRTs) so that, when any is eventually polled, it may have reached a (local) decision. The rover also implements an SPRT using as observables the local decisions (amounting to some counting processes). The idea behind is that of reducing the time needed to end up with a final decision by the rover, with respect to similar, but nonsequential, schemes. The local SPRTs, moreover, ensure energy savings in terms of communication needs. [C1496]

"A low-power H.264/AVC decoder"

In this paper, memory access could be saved in inter and intra prediction by adopting the proposed memory-efficient decoding ordering. In the proposed hierarchical syntax parser, gated clock technique could be effectively applied to reduce power. Simulation shows the proposed design consumes 88mW in real time decoding 1080HD video sequence. [C1497]

"Low power adiabatic multiplier with complementary pass-transistor logic"

This paper presents a low-power multiplier based on adiabatic logic. Complementary pass-transistor adiabatic logic (CPAL) circuits are described, and the minimization of energy consumption is investigated by choosing the optimal size of the CPAL circuits. An 8Ч8-bit adiabatic multiplier is designed. The organization of the multiplier is identical to the conventional CMOS carry-save multiplier. All the circuits use CPAL to recover the charge of node capacitances. The power consumption of the proposed multiplier, based on CPAL, is significantly reduced, because the non-adiabatic energy loss of output loads has been eliminated using complementary pass-transistor logic for evaluation and transmission gates for energy-recovery. SPICE simulation results indicate energy savings of 70% as compared to the conventional CMOS implementation at 200 MHz. [C1498]

"Systematic power reduction and performance analysis of mismatch limited ADC designs"

This paper focuses on several methods to save power consumption in mismatch limited ADC designs, like flash and folding architectures. Migrating existing designs to a next submicron technology helps to reduce the power consumption significantly. It is shown that decreasing bandwidth and sample rate creates a more than linear reduction of the power consumption. Both of these methods are addressed in this paper. Also the balance between power consumption of the analog and digital circuitry is examined. An existing 6-bit 1.6GS/s ADC in 0.18µm CMOS is transferred to a 0.12µm technology. The sampling rate is reduced to 260MS/s, the measured ERBW to 124MHz while running at only 32mW. As the bandwidth is downscaled 5Ч, the power consumption is reduced by 10Ч, which results in an improved conversion efficiency. As the design topology is unaltered, the implemented design sets a reference for evaluation of any low-power technique. [C1499]

"Region-level approximate computation reuse for power reduction in multimedia applications"

Motivated by data value locality and quality tolerance present in multimedia applications, we propose a new micro-architecture, region-level approximate computation buffer (RACB), to reduce power consumption in such applications. The proposed RACB relaxes the exact matching into partial and approximate tag matching and applies it to regions of code in a program, thereby allowing for aggressive computation/execution reduction, in addition to reductions in memory accesses and pipeline activities. Our experiments demonstrate that a 64-entry RACB can yield up to 70% of region-level execution reduction without noticeable quality degradation in MPEG-2 video decoding, corresponding to 55.9% of system power savings with respect to the regions. [C1500]

"Power-optimal repeater insertion considering Vdd and Vth as design freedoms"

This work first presents an analytical repeater insertion method which optimizes power under delay constraint for a single net. This method finds the optimal repeater insertion lengths, repeater sizes, and Vddand Vthlevels for a net with a delay target, and it reduces more than 50% power over a previous work which does not consider Vddand Vthoptimization. This work further presents the power saving when multiple Vddand Vthlevels are used in repeater insertion at the full-chip level. Compared to the case with single Vddand Vthsuggested by ITRS, optimized dual Vddand dual Vthreduce overall global interconnect power by 47%, 28% and 13% for 130nm, 90nm and 65nm technology nodes, respectively, but extra Vddor Vthlevels only give marginal improvement. We

also show that an optimized single Vthreduce interconnect power almost as effective as dual-Vthdoes, in contrast to the need of dual Vthfor logic circuits. [C1501]

"Inter-program optimizations for conserving disk energy"

Previous work has shown that intra-program optimizations, i.e., optimizations performed on individual programs in isolation, can be very effective in reducing disk energy in streaming applications. This paper investigates the potential additional benefits of inter-program optimizations where sets of programs are optimized together. Experimental results on different subsets of three streaming applications show that 7-49% additional energy savings (27.3% on average) can be obtained with negligible performance penalties using two novel inter-program optimizations, namely execution context sensitive buffer size selection and inverse barrier synchronization. These figures were obtained via physical measurements on two laptop disks. [C1502]

"Near-memory caching for improved energy consumption"

Main memory has become one of the largest contributors to overall energy consumption and offers many opportunities for power/energy reduction. In this paper, we propose a power-aware cached-DRAM (PA-CDRAM) organization that integrates a moderately sized cache directly into a memory module. We use this near-memory cache to turn a memory bank off immediately after it is accessed to reduce power consumption. We modify the structure of cached DRAM (CDRAM) with the goal of reducing energy consumption while retaining the performance advantage for which CDRAM was originally proposed. We evaluate the approach using a cycle accurate processor and memory simulator. Our results show that PACDRAM achieves up to 84% (28% on average) improvement in the energy-delay product and up to 76% (19% on average) savings in energy when compared to a time-out power management technique. [C1503]

"Architectural Design of a Sensory-Node-Controller for Sensor Network"

Increasing complexity of manufacturing systems has led to a wick-spread application of large-scale sensor networks. Effective and efficient operation of the sensor network requires the introduction of a new platform that enables adaptive, event-driven information gathering based on the condition of machines. To realize such a platform, this paper presents several fundamental aspects regarding the architectural design of a Sensory-Node Controller (SNOC), which is the key element in a large-scale sensor network that controls the operation of individual physical sensors and coordinates the communication among various sensing clusters. The focus of the study is on an energy-efficient SNOC design that enables a dynamically adjustable power supply and data acquisition procedure to reduce the overall energy requirement of the sensor network, for sustainable, long-term operations. Both hardware and software considerations for the parametric SNOC design are described, and analytical formulations presented. Simulation of energy consumption based on a sensor cluster consisting of 40 SNOCs shows 57% of energy saving in comparison with the conventional sensing technique. The study has provided input to the design optimization and experimental realization of a SNOC-based sensor network for machine system monitoring [C1504]

"An evaluation of code and data optimizations in the context of disk power reduction"

Disk power management is becoming increasingly important in high-end server and cluster type of environments that execute data-intensive applications. While hardware-only approaches (e.g., low-power modes supported by current disks) are successful to a certain extent, one also needs to consider the software side to achieve further energy savings. This paper first demonstrates that conventional data locality oriented code transformations are not sufficient for minimizing disk power consumption. The reason is that these optimizations do not take into account how disk-resident array data are laid out on the disk system, and consequently, fail to increase idle periods of disks, which is the primary metric using which disk power can be reduced. Instead, we propose a disk layout aware application optimization strategy that uses both code restructuring and data layout optimization. Our experimental evaluation with several benchmark codes reveal that the proposed strategy is very successful in reducing disk energy consumption without performing much worse than a pure data locality oriented scheme, as far as execution cycles are concerned. The experiments also show that the benefits coming from our approach increase with the increased number of disks; i.e., it scales very well. [C1505]

"A tunable bus encoder for off-chip data buses"

Off-chip buses constitute a significant portion of the total system power in embedded systems. Past research has focused on encoding contiguous bit positions in data values to reduce the transition activity in the off-chip data buses. In this paper, the authors proposed tunable bus encoding (TUBE) scheme to reduce the power consumption in the data buses, which exploits repetition in contiguous as well as non-contiguous bit positions in order to encode data values. Problems of keeping just one control signal for the codec design were also solved.

The results were compared with some of the already existing best schemes such as frequent value encoding (FVE) and FV-MSB-LSB encoding schemes. It is found that the scheme achieves an improvement of 21 % on average and up to 28% on some benchmarks over the FVE scheme and up to 84% over unencoded data. In comparison to FV-MSB-LSB encoding scheme, the presented scheme improves the energy savings by 10% on average and up to 21% for some media applications at the expense of minimal 0.45% performance overhead. A hardware design of the codec was presented and a detailed analysis of the hardware overhead in terms of area, delay and energy consumption were provided. It is again found that the codec can be easily implemented in an on-chip memory controller with small area requirement of 0.0521 mm2. [C1506]

"Fast configurable-cache tuning with a unified second-level cache"

Tuning a configurable cache subsystem to an application can greatly reduce memory hierarchy energy consumption. Previous tuning methods use a level one configurable cache only, or a second level with separate instruction and data configurable caches. The authors instead used a commercially-common unified second level, a seemingly minor difference that actually expands the configuration space from 500 to about 20,000. Additive way tuning for tuning a cache subsystem was developed with this large space, yielding 62% energy savings and 35% performance improvements over a non-configurable cache, greatly outperforming an extension of a previous method. [C1507]

"Low-power multimedia scheduling using output pre-buffering"

This paper describes BE-OS, a buffer-based energy-efficient CPU scheduler for mobile devices that primarily run real-time multimedia applications. BE-OS is an operating system algorithm on low-power hardware technique such as dynamic voltage scaling (DVS), which has been a key technique in taking advantage of hardware characteristics of processor (CPU) to reduce energy consumption. DVS provides operating system with the ability to dynamically change processor's clock frequency and thus optimize energy consumption. The pre-buffering technique for multimedia output is a key motivation for our algorithm that keeps output data (frames) of real-time multimedia applications in the buffers temporarily. We aimed the fact that the buffer absorbs the variation of CPU workload. Our control algorithm observes how much the buffer is occupied, and adjusts CPU frequency accordingly. This frequency adjustment operates as a feedback control system for the buffer. Mathematical analysis shows that this control model is stable and well-behaved. This buffer-based algorithm eliminates CPU idle time fully, minimizing energy consumption compared with previously proposed algorithms. And our scheduling algorithm enables BE-OS to support multiple task case, which includes not only buffer-enabled multimedia tasks, but also interactive tasks. Our simulation results show that overall operation of BE-OS is successful in guaranteeing both quick response of interactive tasks and QoS of multimedia tasks. And the results indicates that compared to previously proposed algorithms, BE-OS saves energy by 20% to 70% while delivering almost perfect QoS guarantees for multimedia playbacks. [C1508]

"Limits for switching power consumption in encoded interconnects"

Power consumption emerged as a key performance and cost limiting factor in CMOS integrated circuit design. As technology shrinks, the required interconnection structures increasingly affect the overall power consumption, performance and area requirements. Therefore, signal encoding has been proposed as an efficient way to reduce the switching power consumption in buses. The goal of this work is to determine the realizable lower bound of encoding-based schemes that reduce switching power consumption. These limits can be employed at higher levels of abstraction to give information about the maximum achievable encoding-based power savings without any knowledge on the optimal encoding scheme. Moreover, the algorithm developed in this work can also be used to construct those optimal encoding schemes in a more efficient way than previously proposed techniques. [C1509]

"Dynamic slack reclamation with procrastination scheduling in real-time embedded systems"

Leakage energy consumption is an increasing concern in current and future CMOS technology generations. Procrastination scheduling, where task execution can be delayed to maximize the duration of idle intervals, has been proposed to minimize leakage energy drain. The authors addressed dynamic slack reclamation techniques under procrastination scheduling to minimize the static and dynamic energy consumption. In addition to dynamic task slowdown, a dynamic procrastination was proposed, which seeks to extend idle intervals through slack reclamation. While using the entire slack for either slowdown or procrastination need not be the most energy efficient approach, the slack was distributed between slowdown and procrastination to exploit maximum energy savings. The simulation experiments showed that dynamic slowdown result on an average 10% energy gains over static slowdown. Dynamic procrastination extends the average sleep interval by 25%, which reduces the idle energy consumption by 15%, while meeting all timing requirements. [C1510]

"Fault and energy-aware communication mapping with guaranteed latency for applications implemented on NoC"

As feature sizes shrink, transient failures of on-chip network links become a critical problem. At the same time, many applications require guarantees on both message arrival probability and response time. We address the problem of transient link failures by means of temporally and spatially redundant transmission of messages, such that designer-imposed message arrival probabilities are guaranteed. Response time minimisation is achieved by a heuristic that statically assigns multiple copies of each message to network links, intelligently combining temporal and spatial redundancy. Concerns regarding energy consumption are addressed in two ways. Firstly, we reduce the total amount of transmitted messages, and, secondly, we minimise the application response time such that the resulted time slack can be exploited for energy savings through voltage reduction. The advantages of the proposed approach are guaranteed message arrival probability and guaranteed worst case application response time. [C1511]

"Custom instruction filter cache synthesis for low-power embedded systems"

Filter cache has been shown to substantially reduce the power consumption in instruction memory hierarchy. Filter cache achieves energy savings due to the locality found in the frequent tiny loops, which are application dependent. In this paper we show that tuning filter cache to the needs of a particular application can save power and energy. Beside, a simple loop profiler directed methodology to deduce the optimal or near-optimal filter cache is proposed, without having to simulating all possible combinations of cache parameters from the specified space. Our experiments with MediaBench benchmark suite shows that the proposed methodology results in up to 49% energy reduction by tuning the filter cache. Moreover, the proposed filter cache tuning is done with the loop characteristics of the application, which in most cases are readily made available. [C1512]

"Energy Aware Routing Protocol for Heterogeneous Wireless Sensor Networks"

In this paper we present Energy Aware Random Asynchronous Wakeup (RAW-E), a novel crosslayer power management and routing protocol for heterogeneous wireless sensor and actor networks. RAW-E is an extension of our previously presented Random Asynchronous Wakeup (RAW), a power saving technique for sensor networks that has been shown to reduce energy consumption without significantly affecting the latency or connectivity of the network. RAW-E is a distributed, randomized algorithm where nodes make local decisions on whether to sleep, or to be active based on the energy level of its neighbors. The primary result of RAW-E is the reduction of energy disparity among sensor nodes. Therefore, while the energy reduction is spread uniformly among nodes, the life of network connectivity is prolonged. RAW-E is scalable to the change in network size, node type, node density and topology. RAW-E accommodates seamlessly such network changes, including the presence of actors in heterogeneous sensor networks. RAW-E takes advantage of actor nodes, and uses their resources when possible, thus reducing the energy consumption of sensor nodes. The performance of our protocol remains very good even in large networks, and it scales with density. Previously we have shown by analysis and simulations that RAW improves communication latency and system lifetime compared to current schemes. Through simulation evaluations, we show that RAW-E adds to those features the improvement on energy consumption and extension of connectivity life for heterogeneous sensor and actor networks [C1513]

"An opportunistic scheduler to balance performance measures and energy consumption in wireless networks: design and implementation"

Energy management is critical for emerging tiny wireless mobile devices such as sensors and PDAs, which are power limited by the capacity of their batteries. The energy cost of wireless transmission is high, being superlinear in the communication distance. Even an idle node that is turned on but otherwise not engaged in any activity may consume a significant amount of energy. Based on the observation that reduced communication distance between two communicating parties can significantly reduce the energy cost of the communication, we propose a motion prediction algorithm that exploits the movement history of a sender node to predict the likelihood that the node may move closer to the receiver by a given deadline. If the likelihood is high, then the transmission is postponed until the mobile node moves closer to the receiver at a future time. To reduce unproductive energy use by an idle node, we propose a sleep/wakeup algorithm that adoptively puts the node into sleep mode. However, while a mobile node is sleeping, it may miss critical opportunities for position update and motion prediction. The objective of this paper is then to realize an opportunistic scheduler that can balance the energy consumption by an idle system and the performance of motion prediction in saving energy for network transmission. The proposed system has been prototyped on an actual sensor network platform. Experimental results show that our opportunistic scheduler can achieve significant energy savings in terms of both network communication and keeping the system awake as necessary. [C1514]

"Transaction-centric split synchronization mechanism for mobile e-business applications"

A mobile e-business client application may intentionally operate in disconnected mode to reduce the communication cost and the power consumption of mobile devices. We use "data hoarding" to allow business transactions to be processed on the mobile client despite of disconnection, which is implemented by the materialized view. We split the synchronization of a mobile transaction with the server database into 2 steps: intermediate and final synchronization. The intermediate synchronization uses the high cost wireless medium while the final synchronization generally uses the low cost communication medium such as a wired LAN. User can customize the synchronization details including the synchronization type for each data object through the materialized view definition expressed in extended SQL. We present the Transaction-Centric Split Synchronization (TCSS) algorithm and evaluate its performance. It supports the customized synchronization for each object that a transaction accesses. Appropriately selected synchronization details considering the data object's semantics can make it possible to save the power consumption of the mobile device and wireless communication cost. [C1515]

"Frame buffer compression using a limited-size code book for low-power display systems"

Modern hand-held multimedia terminals consume significant power for their quality display devices. Due to 60Hz or higher LCD refresh operations, frame buffer memory and related buses become dominant power consumers. In this paper, we introduce an efficient frame buffer compression scheme that uses differential Huffman coding and its hardware implementation. The compression and decompression must be simple and not incur distinct power overhead involving no CPU operations. We have achieved both on-the-fly compression and high compression efficiency devising a limited-size code book, color-difference reduction techniques and an adaptive code book update scheme. On the MobileMark 2002 benchmark, our techniques reduce the frame buffer activity by 52% to 90%, saving up to 86mW including the overhead. [C1516]

"Energy saving for fluorescent lighting in commercial buildings"

Lighting represents a significant component of commercial buildings, particularly in office buildings. This paper reviews the potential of energy savings of fluorescent lighting used in office buildings. It is proposed to obtain energy saving by reducing the supply voltage without much degradation in lighting performance. Experimental results confirm that as much as 20% of electrical energy can be saved by reducing about 9% of the supply voltage, without noticeably affecting light output. [C1517]

"Keeping hot chips cool"

With 90nm CMOS in production and 65nm testing in progress, power has been pushed to the forefront of design metrics. This paper outline practical techniques that are used to reduce both leakage as well as active power in a standard-cell library based high-performance design flow. We discuss the design and cost issues for using different power saving techniques such as: power gating to reduce leakage, multiple and hybrid threshold libraries for leakage reduction and multiple supply voltage based design. In addition techniques to reduce clock tree power are presented as power consumed in clocks accounts for a significant portion of total chip power. Practical aspects of implementing these techniques is also discussed. [C1518]

"System-level energy-efficient dynamic task scheduling"

Dynamic voltage scaling (DVS) is a well-known low power design technique that reduces the processor energy by slowing down the DVS processor and stretching the task execution time. But in a DVS system consisting of a DVS processor and multiple devices, slowing down the processor increases the device energy consumption and thereby the system-level energy consumption. In this paper, we present dynamic task scheduling algorithms for periodic tasks that minimize the system-level energy (CPU energy + device standby energy). The algorithms use a combination of (i) optimal speed setting, which is the speed that minimizes the system energy for a specific task, and (ii) limited preemption which reduces the numbers of possible preemptions. For the case when the CPU power and device power are comparable, these algorithms achieve up to 43% energy savings, but only up to 12% over the non-DVS scheduling. If the device power is large compared to the CPU power, we show that DVS should not be employed. [C1519]

"Reducing power consumption in IEEE 802.11 networks"

In this paper, we show a performance evaluation of the frame aggregation mechanism. This mechanism is introduced as a replacement for the power save polling (PSP) mode integrated in the IEEE 802.11 standard (1999). Since it uses bigger frame to achieve lower traffic and overhead, we investigate the consequences of packet loss on power consumption. Using this study, we are able to propose an adaptive mechanism to trigger

frame aggregation based on the medium conditions as they can be observed from the station (STA) standpoint in an infrastructure environment. [C1520]

"Load-store queue management: an energy-efficient design based on a state-filtering mechanism"

Modern microprocessors incorporate sophisticated techniques to allow early execution of loads without compromising program correctness. To do so, the structures that hold the memory instructions (load and store queues) implement several complex mechanisms to dynamically resolve the memory-based dependences. Our main objective in this paper is to design an efficient LQ-SQ structure, which saves energy without sacrificing much performance. We propose a new design that divides the load queue into two structures, a conventional associative queue and a simpler FIFO queue that does not allow associative searching. A dependence predictor predicts whether a load instruction has a memory dependence on any inflight store instruction. If so, the load is sent to the conventional associative queue. Otherwise, it is sent to the non-associative queue which can only detect dependence in an inexact and conservative way. In addition, the load will not check the store queue at execution time. These measures combined save energy consumption. We explore different predictor designs and runtime policies. Our experiments indicate that such a design can reduce the energy consumption in the load-store queue by 35-50% with an insignificant performance penalty of about 1%. When the energy cost of the increased execution time is factored in, the processor still makes net energy savings of about 3-4%. [C1521]

"Cross-layer flooding for sensor networks without location information"

Flooding algorithm is one of the most significant algorithms used in sensor networks. Although simple, this algorithm causes a large amount of energy and bandwidth to be wasted. The most important application of flooding is RREQ flooding in initial step of most routing algorithms. Although simple, this algorithm causes a large amount of energy and bandwidth to be wasted. Most previous efficient flooding algorithms use location information, which is impossible for simple node in sensor network. Some others are not suitable for RREQ flooding due to eliminating redundant retransmissions. We present a modified flooding that simultaneously decreases energy consumption as well as network delay. This flooding algorithm is a form of cross layer algorithm which uses physical layer information to be more efficient in time and energy. It is shown that the proposed algorithm can save a significant amount of energy while reducing the settling time delay [C1522]

"Conserving energy with on-demand topology management"

To reduce idle-time energy consumption, nodes in ad hoc networks can switch to a power-save mode. However, since operating all nodes in power-save mode limits network capacity, some nodes may need to stay in active mode to support forwarding. The main challenge of selecting nodes to stay in active mode stems from the need to conserve energy while maintaining communication. Although topology management protocols build a forwarding backbone of active nodes by powering down redundant nodes, such protocols incur proactive backbone maintenance overhead. The reactive approach, on-demand power management, manages node transitions from active to power-save mode based on routing information. However, node transitions are only traffic-driven and may result in keeping redundant nodes awake. To this end, we propose TITAN, which builds a backbone reactively using information about both ongoing communication and the current power-management mode of nodes. The design of TITAN is based on the trade-offs between waking up power-saving nodes on shorter routes and using longer routes that contain active nodes. Simulation results show that TITAN conserves energy while maintaining efficient communication without additional control overhead for topology management [C1523]

"Improving power save protocols using carrier sensing for dynamic advertisement windows"

Energy efficient protocols are important in ad hoc networks since battery life for wireless devices is limited. The IEEE 802.11 protocol specifies a simple power save mechanism (PSM) to conserve energy. Packets are advertised for a fixed length of time, known as an advertisement window, at epochs known as beacon intervals. However, the protocol needlessly wastes energy when traffic is relatively light in a network. In this paper, we address this problem by proposing the use of carrier sensing to dynamically adjust the size of the advertisement windows. The adjustment is based on the amount of traffic that needs to be advertised in the current window as opposed to the static window size used by 802.11 PSM. Carrier sensing is used for two different aspects of our protocol. First, carrier sensing is used as an energy efficient method to provide a binary signal which lets neighbors know if a node intends to advertise any packets in the upcoming window. Second, carrier sensing is used as a mechanism for nodes to keep track of whether their neighbors have already stopped listening for advertisements and possibly returned to sleep. Using the ns-2 simulator we show that our techniques can significantly reduce the energy consumption of 802.11 PSM while only slightly increasing latency [C1524]

"EasiPC: a packet compression mechanism for embedded WSN"

Wireless sensor network (WSN) has many promising applications. One of the most challenging technical issues for sensor network design is to enable ultra low power consumption communication. In this paper we propose a packet compression mechanism, namely EasiPC, as a new power management technique for WSN with this mechanism, the lengths of data packets are shortened significantly due to the effective reduction of redundant information. As a consequence the energy required for transporting packets is saved too. Experiments carried out on WSN platform developed in-house show that this packet compression mechanism is both feasible and effective. Additional benefits introduced by this packet compression mechanism include reduced transmission delays, reduced channel accessing collisions, as well as enhanced channel utilization. [C1525]

"Exploration of memory-aware dynamic voltage scheduling for soft real-time applications"

Dynamic voltage scaling (DVS) and dynamic power management (DPM) are widely-used techniques to reduce energy consumption in modern computing systems. Although combining these techniques can save more energy, there has not been much work focused on energy-optimal combination of these techniques under variable memory clock frequencies. In this paper, we explore system-wide energy-optimal frequency space for a memory-aware DVS technique based on a stochastic memory access model for systems with frequency-variable memory devices. In addition, we propose a simple but practical DVS method, which can be applied to an actual platform. [C1526]

"Adaptive energy-aware design of a multi-bank flash-memory storage system"

An architectural solution to reducing energy consumption of flash-memory storage system is to take advantage of a multi-bank architecture instead of a single-bank one. Thus, allowing unused banks to be placed into low-power operating modes can help reduce energy. In this paper, an adaptive energy-aware bank assignment policy is proposed to cluster data with temporal affinity into the same bank, increasing the number of banks put into low-power modes. Then we propose an energy-aware garbage collection policy, which could keep banks in idle conditions for long durations of time to compensate for resynchronization penalties. Experiments over the prototype show the effectiveness of these policies and indicate that large energy savings can be achieved with low overhead. [C1527]

"Designing a high performance and low energy-consuming embedded system with considering code compressed environments"

In this paper, we present an embedded system design which is cost-efficient and which considers performance improvement and power consumption based on the frequency with which instructions are executed. We use the locality of running programs to optimize the use of memory space, system performance, and power consumption; that is, we compress infrequently executed codes to save the use of memory space but compress (encode) frequently executed codes to power consumption and maximize performance. To save the number of memory access times, the frequently executed instructions are encoded as shorter code words and then the continuous code words are packed into a pseudo instruction. Once the decompression engine fetches one pseudo instruction, it can extract multiple instructions to reduce the number of memory access times. In addition, we also propose a design with multiple look-ahead tables that solves the problem which arises due to the reduction in instructions from one-time memory access which occurs because the great amount of frequently executed instructions. From our simulation results, our method with one 256-instruction look-ahead table does not increase the compression ratio, and the ratio of the power consumption can be reduced by about 47.23% than compressing all instructions. With regard to multiple look-ahead table methods, when one 512-instruction look-ahead table is used, the ratio of the power consumption is reduced by 37.25% only, however, when two look-ahead tables that contain 256 instructions in each table are used, the power consumption can be improved by 49.36%. According to the simulation results, our proposed methods based on the frequencies of executed instructions result in low power consumption, performance improvement and reduced memory space. [C1528]

"An energy efficient routing algorithm for wireless sensor networks"

Wireless sensor networks (WSN) is different from the traditional ad-hoc networks with its limited size, memory, energy and computation ability, as well as its cheap and densely deployment characteristic. Some special designs must meet these demands. In this paper, we analyze the problems of traditional routing protocols for WSN, and suggest an energy efficient directional routing protocol. In our algorithm, we use election strategy to select the next hop to the sink, and force other candidates to enter sleep state to save energy. These candidates are weakened up after certain duration to attend the next election. The simulation shows that the new algorithm reduces the average dissipated energy by about 50% percent compared with directional flooding when network size is big enough, and the end-to-end delay is also improved significantly. [C1529]

"A Energy Conservation Scheme to Maintain Data Aggregation Tree in Sensor Networks"

The lifetime of sensor nodes increases mainly in proportion to limited battery capacity in wireless sensor networks. All sensor nodes must reduce energy consumption for maximizing network lifetime. The part of the most energy consumption in the wireless sensor networks is wireless transmission part. Many researches that minimize energy consumption of wireless transmission part are progressing to maximize lifetime of sensors. Especially, the aggregation tree method accomplishes the undertaken job to use that a few representative sensor nodes cover all area. If one of representative sensor nodes occurs break down by battery exhaustion, fault tolerance is achieved by the algorithm that new one replaces old one. Although multiform algorithms have proposed for it, those have the problem that all sensor nodes take unnecessary battery consumption for periodical message transmission due to fault tolerance. This paper proposes an epochal saving mechanism for reducing battery consumption in fault tolerant process [C1530]

"An IR drop-driven placer for standard cells in a SOC design"

A partition-based IR drop-driven algorithm is proposed for standard cell placement. Different cost functions for reducing IR drop are used in the horizontal cut and vertical cut partitioning processes. In addition to minimizing the total wire length, we balance the power consumption of the two partitions during the horizontal cut partitioning process. During the vertical cut partitioning process, we move the cells with higher power consumption closer to the power sources to reduce the maximum IR drop of the row. After placement is finished, we apply a greedy placement refinement process to further reduce the value of the maximum IR drop. Each standard cell row is modeled with an equivalent conductance model. Then the IR drop of each row is calculated and analyzed. We compare the placement generated by the proposed approach with the wire length-driven placement. On average, the proposed approach improves the value of maximum IR drop by 51%. Therefore, it reduces the need to add power straps on the chip and more routing resources are saved [C1531]

"CF-MAC and H-MAC protocols for energy saving in wireless ad hoc networks"

Wireless ad-hoc networks are widely adopted in contexts where a temporary network connectivity is required. The distributed and flexible architecture of these networks is a key strength but, due to the scarce energy resources available at each station, innovative energy efficient MAC algorithms are required in order to extend as much as possible network lifetime, while providing acceptable throughput and delays. Starting from the theory of balanced incomplete block design (BIBD), this paper proposes two power efficient MAC algorithms, which will be referred to as hybrid MAC (H-MAC) and collision free MAC (CF-MAC). The H-MAC algorithm combines standard IEEE 802.11 power saving features with a BIBD-based schedule. CF-MAC, instead, is a fully BIBD-based protocol, which allows a collision free transmission over a shared wireless medium. The performance of the proposed MAC schemes have been compared with the standard 802.11 power saving algorithm using computer simulations, showing that: (1) CF-MAC improves the overall network throughput and reduces the energy consumption with respect to the 802.11 power saving while guaranteeing acceptable delays; (2) H-MAC reduces the energy consumption with respect to 802.11 power saving while guaranteeing the same throughput, at the expense of higher delays. [C1532]

"Improving connectivity and power efficiency in wireless ad hoc networks through agent nodes"

In this paper, we present a framework that improves the reliability and reduce the power consumption of a wireless ad hoc network through the deployment of supplementary nodes called agents. Agents are stationary nodes that have less stringent power constraints than the battery-operated mobile nodes. Placed in a mesh-like formation, agents enhance the connectivity of an ad hoc network by reducing the probability of having a partitioned system. We also show that the power consumption of user nodes is significantly decreased with a clever choice of the routing strategy, one that picks the routes that go through the agent nodes as often as possible, hence preventing the mobiles from relaying packets. In addition, the impact of a power control mode is analyzed. Even though such a mode already promises power efficiency, we demonstrate that the amount of power savings is further increased when the power control is used within the agent scheme. Finally, we present the traffic simulation results to assess the maximum throughput of no-agent and agent-supported networks under various routing strategies like bandwidth-conserving, power-conserving, etc. Some degradation in maximum throughput can be observed as a result of forcing routes to go through agent nodes [C1533]

"Power saving efficiency of a novel packet aggregation scheme for high-throughput WLAN stations at different data rates"

Multiple MCS and receiver aggregation (MMRA) is a method to aggregate several MAC protocol data units (MPDUs) that are intended for different receivers and can be transmitted at different modulation and coding

schemes (MCS) in the next generation of WLAN, the IEEE 802.11n protocol. Traditional aggregation schemes only link MPDUs between the same source and destination device pair together. The main purpose of aggregation is to reduce the number of access attempts to the medium and thereby significantly increase the protocol efficiency and data throughput. Analytical computations show that MMRA performs better not only in time efficiency compared to other single-rate aggregation schemes, where MPDUs aggregates belonging to different receivers are limited to the lowest MCS, but above all MMRA outperforms single-rate aggregation schemes in terms of power efficiency. MMRA provides a power saving frame format structure, which will allow receiving stations to reduce power consumption and save battery life, crucial for small handled devices. [C1534]

"Directed diffusion light: low overhead data dissemination in wireless sensor networks"

In this paper we introduce directed diffusion light, a variant of the well-known protocol directed diffusion (DD), which results in significant savings in terms of exchanged control messages and energy consumption, and improvements in network lifetime. Directed diffusion light defines local rules to generate a sparse logical topology over which DD can be run. This decreases the costs associated to the required DD periodic flooding. Ns-2 based simulation results show that, when 300 sensor nodes are deployed over a squared area of side 200 m directed diffusion light is able to increase the network lifetime four times, to halve the average energy consumption, and to reduce the control overhead to one third the one of DD. [C1535]

"Reducing the energy of speculative instruction schedulers"

Energy dissipation from the issue queue and register file constitutes a large portion of the overall energy budget of an aggressive dynamically scheduled microprocessor. We propose techniques to save energy in these structures by reducing issue queue occupancy and by reducing unnecessary register file accesses that can result from speculative scheduling. Our results show a 44% reduction in issue queue occupancies and an 87% reduction in register file accesses for scheduling replays. Our data show that these savings can translate into a 52% saving in issue queue energy, a 13% savings in register file energy, and a 22% overall energy savings. [C1536]

"Routing through Backbone Structures in Sensor Networks"

Virtual infrastructures or backbones in wireless sensor networks reduce the communication overhead and energy consumption. In this paper, we present backbone routing (BBR), a novel fully distributed protocol for construction and rotation of backbone networks. BBR reduces energy consumption without significantly diminishing the capacity or connectivity of the network. Another key feature of BBR is its energy balancing nature by distributing the role of being backbone node among all the nodes. BBR builds on the observation that when a region of a shared-channel wireless network has a sufficient density of nodes, only a small number of them need be on at any time to forward traffic for active connections. Improvement in system lifetime due to BBR increases as the ratio of idle-to-sleep energy consumption increases, and increases as the density of the network increases. Our experiments show that BBR is more efficient in saving energy and extending network life without deteriorating network performance when compared with 802.11 [C1537]

"Energy- Aware Signals Classification in Ad- hocWireless Sensor Networks"

With the advancement of wireless and electronic technologies, wireless networks consist of tiny sensor devices hold the promise of revolutionizing sensing in a wide range of application domains because of their flexibility, low costs and ease of deployment. In this paper, the employment of ad-hoc wireless sensor networks to perform signals classification is proposed. For such application, the use of low-performance, low-power wireless sensor nodes requires the development of ad-hoc solutions of detection, features extraction and classification of the signals considered. In particular, these solutions allow to reduce the amount of data transmitted from the nodes, thus saving the consumption of energy, and the implementation costs of the classification process. Among other pattern recognition techniques based on theorems from statistical learning theory (SLT), the support vector machine is chosen for its flexibility in classifying patterns. In particular, the properties of the u-SVM allow implementing the SVM classifier on tiny sensor nodes, without significantly to make worse classification performances. As a case of study, acoustic signals are considered for implementation of the proposed algorithms on the Mical sensor node, by Crossbow Technology Inc [C1538]

"A power reduction technique based on the microscopic dynamic voltage scaling (DVS) of multimedia processors in wireless communication terminal"

The paper proposes a DVS method, which effectively reduces the power consumption of multimedia signal processor. Analytical expressions for effective range of power saving efficiency obtained with the assumption of a Gaussian distribution for the frame-based computational burden of the multimedia processor are derived. A

closed form solution for the power saving factor is obtained in terms of the mean and standard deviation of the distribution. An MPEG-2 audio/video decoder algorithm is tested on Xscale processor for experimental verification of the power saving due to the proposed DVS approach. The experimental results with diverse MPEG-2 audio/video files show about 35% power saving efficiency [C1539]

"A Dynamic Node Degree Management Scheme for Energy-efficient Routing Protocols in Wireless Ad Hoc Networks"

In mobile devices, the battery-based power is a precious resource. To maximize the network lifetime becomes a challenge issue in MANETs. We found that transmission collision is a problem which affects the energy saving much. If we can reduce the numbers of the transmission collision, we save more power. In this paper, we propose a new mechanism to address this problem and hence prolong network lifetime. Our approach, based on relative neighborhood graph (RNG), adjusts the transmission range according to the degree of the node which is only based on local information. We also suggest appropriate transmission power ranges to some routing protocols such as AODV, DSR and BELLMAN-FORD. Simulation results show that a great improvement of the energy saving for those routing protocols when comparing with the performance of those protocols without applying our mechanism [C1540]

"Modified distributed mediation device for low power consumption in large scale sensor networks"

This paper proposes a new medium-access control (MAC) protocol designed for wireless sensor networks. A wireless sensor network is an array of large number of sensors interconnected by a multi-hop ad-hoc network. The fundamental objective for sensor network is low-power consumption while latency is usually less important. This characteristic of sensor network motivates different MAC layer design from the conventional wireless network to reduce power consumption. In this paper novel algorithm based on distributed mediation device (DMD) protocol has been introduced that utilized distributed node scheduling strategy to dramatically increase energy saving principally in intermediate devices within a multi-hop communication. The simulation results have shown noticeable power consumption improvement compared with Sensor MAC (S-MAC) and 802.11-like protocols especially in the large scales achieved in trade of more latency in the network. [C1541]

"Energy efficiency analysis of an RLS-based adaptive signal processing algorithm for energy aware sensor networks"

A joint source coding and RLS-based adaptive signal processing approach that exploits the inherent correlations among the sensor data, in order to improve energy efficiency of low-power wireless sensor networks is proposed. The energy efficiency is achieved by reducing the transmission requirements from sensors. A semi-analytical technique is presented in order to determine the energy-efficiency of the proposed scheme taking into account both communications and circuit power consumptions. The numerical results obtained with real sensor data show that the proposed scheme offers significant energy savings compared to previously proposed schemes. [C1542]

"Tracking irregularly moving objects based on alert-enabling sensor model in sensor networks"

Tracking moving objects is one of the important applications in sensor networks. A key issue in designing such sensor applications is to reduce energy consumption as the available power of a sensor is supplied by a battery and is limited. Many methods have been proposed to track moving objects, however, the improvement in energy consumption is still insignificant, particularly for those moving objects with irregularly moving behavior. In this paper, we tackle the object tracking problem under the theme of minimizing energy consumption for sensor networks. We first design an alert-enabling sensor model so that distributed sensors are able to participate in the decision making for tracking objects. We then propose a novel alert-based object tracking (AbOT) scheme, to minimize the consumed energy for the object tracking applications. Our performance results reveal that AbOT can significantly save energy and still have high accuracy under various conditions. [C1543]

"APSM: bounding the downlink delay for 802.11 power save mode"

The popularity of wireless LANs, due to their low cost provision of high speed wireless Internet access, has resulted in a strong trend toward the integration of this technology in the upcoming all-in-one mobile devices that could include, for instance, cellular, wireless LAN and personal digital assistant (PDA) capabilities. Such devices, though, require power saving mechanisms in order to guarantee a reasonable battery duration. The 802.11 standard provides a power save mode that reduces the wireless LAN technology power consumption, however, this mode can result in downlink delays (AP to station) unacceptable for the QoS of some applications, e.g., VoIP. To overcome this problem, we propose an adaptive power save mode algorithm (APSM) that adapts

the data frames MAC downlink delay of a certain station according to the downlink frame interarrival time observed at the AP MAC layer. We conducted an evaluation of our proposal with respect to downlink delay, power efficiency and signaling load using the OPNET simulator and compared its performance with the 802.11 standard power save mode and two different static alternatives. The results show the effectiveness of our algorithm in providing a soft upper bound to the MAC downlink delay while significantly decreasing the power consumption and requiring a signaling load similar to that of the standard power save mode. [C1544]

"Sensor Network Design and Implementation for Health Telecare and Diagnosis Assistance Applications"

The attempts to develop a ubiquitous health care monitoring system arisen from the need of automatic real-time medical services for emergent diseases. Besides, the physiological statuses gathered and maintained by this system are very helpful for diagnosis and early warning. To improve the medical services and diagnosis accuracy, a Wireless Health Advanced Mobile Bio-diagnostic System (abbreviated as WHAM-BioS) is proposed. This study focuses on network/communication technology in the WHAM-BioS and proposes a novel clustered sensor network (CSN) architecture for long-term periodical telecare applications. In the proposed CSN architecture, most network functions are concentrated in a special purpose device called the human body gateway (HBG). The sensor nodes focus on detecting and reporting their detection results to their HBG. To reduce the design complexity and the implementation cost for the sensor nodes, the proposed architecture proposed several protocols to help each HBG to provide a contention free environment for their sensor nodes. The contention free environment significantly reduces the power consumption in data retransmission. Besides, to further reduce the power consumption of the sensor nodes, this study also proposes a power saving mechanism, which reduces the power consumption in idle listening. Based on the proposed network architecture and protocols, a prototype system is implemented [C1545]

"Feasibility study of low-swing clocking"

This paper evaluates the feasibility of low-swing clocking under no performance degradation constraint. We consider flip-flops, logic and clock distribution network in our analysis. The preferred flip-flop topologies for low-swing clocking (low-VClk) are different from those normally used in a full-swing (high-VClk) design. Clock buffers are redesigned to accommodate reduced drive current under low-VClk. In order to maintain performance, logic and flip-flops must absorb increase in clock skew due to low-VClk. In a 64-bit ALU design, the optimal low-VClkdesign point is at the minimum energy-delay product (EDP) point of the high-VClkdesign, with no delay or energy penalty in the ALU itself. A 43% energy reduction achieved in the clock distribution network results in a 13% overall energy savings due to low-VClk, assuming that the clocking energy is 40% of the total energy tinder high-VClk. For performance targets of at least one FO4 inverter delay better than the min-EDP point, low-swing clocking becomes ineffective because of a high energy cost in logic that is spent to absorb increase in flip-flop delay and clock skew. Finally, low-VClkcannot achieve the peak performance of the high-VClkdesign due to slower flip-flops and higher clock uncertainty at low-VClk. [C1546]

"Data aggregation in wireless sensor networks-exact and approximate algorithms"

A fundamental challenge in the design of wireless sensor networks (WSNs) is to maximize their lifetimes. Data aggregation has emerged as a basic approach in WSNs in order to reduce the number of transmissions of sensor nodes, and hence minimizing the overall power consumption in the network. We study optimal data aggregation in WSNs. Data aggregation is affected by several factors, such as the placement of aggregation points, the aggregation function, and the density of sensors in the network. The determination of an optimal selection of aggregation points is thus extremely important. We present exact and approximate algorithms to find the minimum number of aggregation points in order to maximize the network lifetime. Our algorithms use a fixed virtual wireless backbone that is built on top of the physical topology. We also study the tradeoffs between energy savings and the potential delay involved in the data aggregation process. Numerical results show that our approach provides substantial energy savings. [C1547]

"Synchroscalar: a multiple clock domain, power-aware, tile-based embedded processor"

We present Synchroscalar, a tile-based architecture for embedded processing that is designed to provide the flexibility of DSPs while approaching the power efficiency of ASICs. We achieve this goal by providing high parallelism and voltage scaling while minimizing control and communication costs. Specifically, Synchroscalar uses columns of processor tiles organized into statically-assigned frequency-voltage domains to minimize power consumption. Furthermore, while columns use SIMD control to minimize overhead, data-dependent computations can be supported by extremely flexible statically-scheduled communication between columns. We provide a detailed evaluation of Synchroscalar including SPICE simulation, wire and device models, synthesis of key

components, cycle-level simulation, and compiler- and hand-optimized signal processing applications. We find that the goal of meeting, not exceeding, performance targets with data-parallel applications leads to designs that depart significantly from our intuitions derived from general-purpose microprocessor design. In particular, synchronous design and substantial global interconnect are desirable in the low-frequency, low-power domain. This global interconnect supports parallelization and reduces processor idle time, which are critical to energy efficient implementations of high bandwidth signal processing. Overall, Synchroscalar provides programmability while achieving power efficiencies within 8-30Ч of known ASIC implementations, which is 10-60Ч better than conventional DSPs. In addition, frequency-voltage scaling in Synchroscalar provides between 3-32% power savings in our application suite. [C1548]

"Flexible power scheduling for sensor networks"

We propose a distributed on-demand power-management protocol for collecting data in sensor networks. The protocol aims to reduce power consumption while supporting fluctuating demand in the network and provide local routing information and synchronicity without global control. Energy savings are achieved by powering down nodes during idle times identified through dynamic scheduling. We present a real implementation on wireless sensor nodes based on a novel, two-level architecture. We evaluate our approach through measurements and simulation, and show how the protocol allows adaptive scheduling and enables a smooth trade-off between energy savings and latency. An example current measurement shows an energy savings of 83% on an intermediate node. [C1549]

"Backcasting: adaptive sampling for sensor networks"

Wireless sensor networks provide an attractive approach to spatially monitoring environments. Wireless technology makes these systems relatively flexible, but also places heavy demands on energy consumption for communications. This raises a fundamental trade-off: using higher densities of sensors provides more measurements, higher resolution and better accuracy, but requires more communications and processing. This paper proposes a new approach, called "back-casting," which can significantly reduce communications and energy consumption while maintaining high accuracy. Back-casting operates by first having a small subset of the wireless sensors communicate their information to a fusion center. This provides an initial estimate of the environment being sensed, and guides the allocation of additional network resources. Specifically, the fusion center backcasts information based on the initial estimate to the network at large, selectively activating additional sensor nodes in order to achieve a target error level. The key idea is that the initial estimate can detect correlations in the environment, indicating that many sensors may not need to be activated by the fusion center. Thus, adaptive sampling can save energy compared to dense, non-adaptive sampling. This method is theoretically analyzed in the context of field estimation and it is shown that the energy savings can be quite significant compared to conventional approaches. For example, when sensing a piecewise smooth field with an array of 100 Ч 100 sensors, adaptive sampling can reduce the energy consumption by roughly a factor of 10 while providing the same accuracy achievable if all sensors were activated. [C1550]

"A content aware integer register file organization"

A register file is a critical component of a modern superscalar processor. It has a large number of entries and read/write ports in order to enable high levels of instruction parallelism. As a result, the register file's area, access time, and energy consumption increase dramatically, significantly affecting the overall superscalar processor's performance and energy consumption. This is especially true in 64-bit processors. This paper presents a new integer register file organization, which reduces energy consumption, area, and access time of the register file with a minimal effect on overall IPC. This is accomplished by exploiting a new concept, partial value locality, which is defined as occurrence of multiple live value instances identical in a subset of their bits. A possible implementation of the new register file is described and shown to obtain proposed optimized register file designs. Overall, an energy reduction of over 50%, a 18% decrease in area, and a 15% reduction in the access time are achieved in the new register file. The energy and area savings are achieved with a 1.7% reduction in IPC for integer applications and a negligible 0.3% in numerical applications, assuming the same clock frequency. A performance increase of up to 13% is possible if the clock frequency can be increases due to a reduction in the register file access time. This approach enables other, very promising optimizations, three of which are outlined in the paper. [C1551]

"A low-power group-based VLD design"

In this paper, a low power variable length code decoder with group-based scheme is proposed. It can save at most 70% power dissipation while maintaining the same throughput rate as the conventional one. This proposal mainly consists of look-up table (LUT) partitioning and group-based memory storing, where the former is used to

reduce the power wasted on looking-up unnecessary code-words due to a large LUT, especially those code-words with low probability; the latter is used to reduce the storage space of VLC tables and maintain the flexibility of our hardware decoder. [C1552]

"Direct digital frequency synthesizer with multi-stage linear interpolation"

Direct digital frequency synthesizers (DDFS's) are playing an important role in modern communication systems. One of the problems of the DDFS is a phase-to-amplitude converter (PAC) based on ROM. The large size ROM yields not only better frequency resolution and better spurious performance, but also higher power consumption and lower speed. This papers proposes a new type of DDFS with a multi-stage interpolation scheme to convert the phase data into sinusoid amplitude. The multi-stage interpolation provides better approximation while the increase of the ROM size is held minimum. Better approximation ability of the proposed DDFS reduces the spurious performance. The simulation and experimental results show that it can achieve a considerable savings in the required ROM capacity while respectable spurious performance is provided. [C1553]

"A 0.8μm CMOS programmable IIR SC filter"

The design of a 0.8μm standard CMOS digitally programmable switched-capacitor recursive (IIR) filter is presented. A digital-to-analog conversion technique, instead conventional capacitor banks, is adopted so that power consumption and silicon area savings are achieved. Using transfer functions with only two poles and positioning zeros structurally on the unit circle, the described design technique ensures low sensitivity in both passband and stopband frequencies. Moreover, non-ideal effects, such as charge injection and opamp offset voltages, are greatly reduced by using a fully differential filter structure. Experimental results verifying the feasibility of the proposed approach are included. [C1554]

"Crosstalk energy reduction by temporal shielding"

This work proposes a novel approach to reduce coupling energy in a data bus, while guaranteeing complete elimination of crosstalk. The proposed solution is based on exploiting the redundancy introduced for implementing the shielding of bus lines, to realize a time-multiplexed scheme in which two data words are sent on the bus simultaneously. Results on a set of typical data sequences show energy savings of over 18% (on average) with respect to the original bus structure, and of over 17% (on average) with respect to a conventional shielding solution. [C1555]

"Dual-edge triggered level converting flip-flops"

Level converting flip-flops are critical elements in dual-VDDdesign for level conversion at the interface from low supply to high supply regions. Level converting flip-flops also provide energy savings on the clock distribution network by using low-swing clock signals. We propose dual-edge triggered level converting flip-flops that provide data sampling and level converting functions at both rising and falling edges of a low-swing clock. Adding the dual-edge triggering feature to level converting flip-flops, the clock frequency can be reduced by half, resulting in 50% power savings on the clock tree in addition to the savings due to low voltage swing clock. Moreover, the proposed flip-flops outperform the existing level converting flip-flops in terms of performance. The dual-edge triggering capability is achieved by using a dual pulse clock generator that generates short pulses at both rising and falling edges of the clock. Based on simulation results in a 0.25 μm CMOS technology, the proposed flip-flops exhibit up to 68% delay reduction as compared to existing level converting flip-flops. [C1556]

"Energy efficient dual threshold voltage dynamic circuits employing sleep switches to minimize subthreshold leakage"

A sleep switch dual threshold voltage domino logic circuit technique for placing idle domino circuits into a low leakage state is proposed in this paper. The circuit technique reduces the leakage energy by up to 830 times as compared to a standard low threshold voltage domino logic circuit in a 0.18 μm CMOS technology. The sleep switch circuit technique significantly enhances the effectiveness of a dual threshold voltage CMOS technology to reduce subthreshold leakage current by strongly turning off all of the high threshold voltage transistors. The circuit technique reduces leakage energy by up to 714 times as compared to a standard dual threshold voltage domino logic circuit. A domino adder enters and leaves the low leakage sleep mode within a single clock cycle. The energy overhead of the circuit technique is low, justifying the activation of the proposed sleep scheme by producing a net savings in total power consumption during idle periods as short as 57 clock cycles. [C1557]

"A pseudo-class-AB telescopic-cascode operational amplifier"

A class-AB architecture for single-stage operational amplifiers is presented. The structure employs a switched-

capacitor level shifter to apply the signal to both sink and source output transistors to create the class-AB behavior. Using this structure, the current mirror circuit of traditional class-AB structures can be eliminated. Thus some power can be saved and the operation frequency can be increased. Simulation results of a fast-settling telescopic-cascode op-amp employing this pseudo-class-AB technique confirm the effectiveness of the approach to reduce the power consumption. This approach can be applied to the first stage of a two-stage op-amp as well, to increase the slew rate. The simulated 12-bit 100-Ms/s sample-and-hold amplifier employing the proposed pseudo-class-AB telescopic-cascode op-amp consumes only 16 mW from 3.3 V power supply. [C1558]

"Design of digital control systems with dynamic voltage scaling"

For real-time computer-controlled systems, control performances of tasks as well as energy consumption of overall system must be optimized. A control task does not have a fixed period but a range of periods in which control performance varies. Hence when more than one control tasks are scheduled on a single processor, an optimization problem appears. Furthermore, when an energy saving technique such as dynamic voltage scaling is used, its properties affect the control performance. Using a performance index that involves control performance and energy consumption, a static solution is proposed to obtain optimal processor speed and a set of periods for given control tasks in O(k). Also, a dynamic solution is proposed to utilize system services of real-time operating systems to overcome unavoidable deficiencies of the static solution and to further reduce the energy consumption of the overall system. The performances of proposed solutions are revealed via simulation studies. [C1559]

"Energy-aware traffic shaping for wireless real-time applications"

Sleep modes of wireless network cards are used to switch these cards into low-power state when idle, but large timeout periods and frequent wake-ups can reduce the utility of this approach. Modern processors offer the ability to switch CPU voltages or clock frequencies and therefore reduce CPU energy consumption, however, that can reduce the sleep durations of a network device, adversely affecting the achievable energy savings. This paper describes an approach in which multiple resource managers cooperate to reduce a mobile device's energy consumption. This system-level approach is based on the integrated management of a real-time CPU scheduler, the frequency scaling capabilities of a modern processor, a QoS packet scheduler, and the low-power sleep mode of a wireless network card. [C1560]

"Development of Ka/Q-band 100 W peak power MMPM"

We are currently developing a Ka/Q-band 100 W peak power MMPM which is suited to millimeter-wave FWA base stations or satellite terminals. The innovative power-saved MMPM has the feature of a peak RF output power of more than 100 W (100 W peak) with power consumption of approximately 100 W at an actual operating output power level of 10 W cw. The TWT is designed so as to reduce power consumption by adopting a four-stage-depressed collector and setting the collector voltages matched to the actual operating condition (output power of 10 W cw). In addition, we have researched several kinds of basic technology, for example, for RF loss reduction and secondary emission suppression. [C1561]

"Power-conscious design methodology for class-A switched-current wave filters"

This paper addresses power consumption in switched-current filters, designed using the wave filter technique and class-A memory cells. It has been demonstrated that power consumption can de reduced through the proposed two stage bias and signal current scaling method, whilst ensuring no degradation in filter total harmonic distortion. Two full transistor-level filter case studies using 0.6μm 3.3V BSim3v3 CMOS foundry models are given to demonstrate the method, with additional simulation results for filters of different types and orders showing power savings as high as 16.6%. One case study has been fabricated, with measured silicon results confirming simulated savings. [C1562]

"Dynamic, power-aware scheduling for mobile clients using a transparent proxy"

Mobile computers consume significant amounts of energy when receiving large files. The wireless network interface card (WNIC) is the primary source of this energy consumption. One way to reduce the energy consumed is to transmit the packets to clients in a predictable fashion. Specifically, the packets can be sent in bursts to clients, who can then switch to a lower power sleep state between bursts. This technique is especially effective when the bandwidth of a stream is small. This work investigates techniques for saving energy in a multiple-client scenario, where clients may be receiving either UDP or TCP data. Energy is saved by using a transparent proxy that is invisible to both clients and servers. The proxy implementation maintains separate connections to the client and server so that a large increase in transmission time is avoided. The proxy also

buffers data and dynamically generates a global transmission schedule that includes all active clients. Results show that energy savings within 10-15% of optimal are common, with little packet loss. [C1563]

"Traceback-enhanced MAP decoding algorithm"

Soft-input soft-output algorithms are the principal component of the iterative decoding used in turbo codes and other 'turbo' feedback schemes. To enable efficient implementation, especially on energy constrained platforms such as portable devices, it is crucial to reduce the computational complexity to a minimum. We propose an enhancement to the MAX-LOG-MAP algorithm by adding a traceback operation similar to that used in the Viterbi algorithm, and devise a new efficient way to initialize the start state of the traceback. This enhancement is effective for each decoding iteration, and provides saving on top of existing techniques such as early termination and memory optimizations. It reduces the computational complexity by an additional 15%, without incurring any performance penalty. [C1564]

"A distributed optimization algorithm for power control in wireless ad hoc networks"

Summary form only given. Power control is an important issue in wireless networks, which still has no satisfactory solution. Due to the limited amount of power available to wireless units, there is a need for systems that operate with reduced power consumption levels. We propose a new model for the problem, that exploits the relationship among necessary power and reach of broadcast. The resulting model is called the power control problem in ad hoc networks (PCADHOC). We derive a linear integer programming model, which is used to find lower bounds on the amount of required power. The constraints of the problem guarantee that all required transmissions can be successfully performed. A distributed algorithm based on variable neighborhood search is proposed to solve the PCADHOC. The results of experiments with the algorithm show that the power savings are considerable. [C1565]

"Dynamic power management using data buffers"

This paper presents a method to reduce energy consumption by inserting data buffers. The method determines whether power can be reduced by inserting a buffer between two components and periodically turning off one of them. This method calculates the length of the period and the required buffer size to achieve the optimal energy savings. Our approach can be applied to any applications whose data arrival and departure rates are different and known in advance. [C1566]

"Why transition coding for power minimization of on-chip buses does not work"

Encoding techniques which minimize the self- or coupling activity of buses are often proposed to reduce power dissipation on system buses. In this paper, we investigate the efficiency of several coding schemes for on-chip buses with respect to overall power dissipation. The power of the codec systems was estimated by power simulations with the lay-outs and related to the savings on the bus. We derived an expression for the energy efficiency of the codecs as a function of bus length (capacitive load). Despite the fact that adaptive schemes could obtain up to 40% savings, the bus lengths required to reduce the overall power consumption are not realistic for on-chip buses. [C1567]

"A low power strategy for future mobile terminals"

In this paper, we have investigated the efficiency of two power-saving strategies that reduces both static and dynamic power consumption when applied to a chip-multiprocessor (CMP). They are evaluated under two workload scenarios and compared against a conventional uni-processor architecture and a CMP without any power-aware scheduling. The results show that energy due to static and dynamic power consumption can be reduced by up to 78% and that further 8% energy can be saved at the expense of response-time of non-critical applications. Furthermore, a small study on the potential impact of system-level events showed that system calls can contribute significantly to the total energy consumed. [C1568]

"Cache-aware scratchpad allocation algorithm"

In the context of portable embedded systems, reducing energy is one of the prime objectives. Most high-end embedded microprocessors include onchip instruction and data caches, along with a small energy efficient scratchpad. Previous approaches for utilizing scratchpad did not consider caches and hence fail for the au courant architecture. In the presented work, we use the scratchpad for storing instructions and propose a generic cache aware scratchpad allocation (CASA) algorithm. We report an average reduction of 8-29% in instruction memory energy consumption compared to a previously published technique for benchmarks from the mediabench suite. The scratchpad in the presented architecture is similar to a preloaded loop cache. Comparing

the energy consumption of our approach against preloaded loop caches, we report average energy savings of 20-44%. [C1569]

"Tuning in-sensor data filtering to reduce energy consumption in wireless sensor networks"

In recent years, research on wireless sensor networks has been undergoing a revolution, promising to have significant impact on a broad range of applications from military to health care to food safety. An important problem in many sensor network applications is to decide the amount of computation (or filtering) that needs to be done in the sensor nodes before the data are shifted to a central base station. Right amount of data filtering in the sensor nodes can lead to large savings in network-wide energy consumption. The main goal of this paper is to develop an automated strategy for data filtering in wireless sensor nodes. Assuming that one needs to reduce the overall energy consumption (as opposed to reducing just computation energy or communication energy), the proposed strategy attempts to strike a balance between computation energy consumption and communication energy consumption. Our experimental results clearly indicate that the proposed data filtering strategy generates substantial energy savings in practice. [C1570]

"Impact of data transformations on memory bank locality"

High-energy consumption presents a problem for sustainable clock frequency and deliverable performance. In particular, memory energy consumption of array-intensive applications can be overwhelming due to poor cache locality. One option for reducing memory energy is to adopt a banked memory architecture, where memory space is divided into banks and each bank can be powered down if it is not in active use. An important issue here is the bank access pattern, which determines opportunities for saving energy. In this paper, we present a compiler-based data layout transformation strategy for increasing the effectiveness of a banked memory architecture. The idea is to transform the array layouts in memory in such a way that two loop iterations executed one after another access the data in the same bank as much as possible; the remaining banks can be placed into a low-power mode. Our simulation-based experiments with nine array-intensive applications show significant savings in memory energy consumption. [C1571]

"Prediction-based strategies for energy saving in object tracking sensor networks"

In order to fully realize the potential of sensor networks, energy awareness should be incorporated into every stage of the network design and operation. In this paper, we address the energy management issue in a sensor network killer application-object tracking sensor networks (OTSNs). Based on the fact that the movements of the tracked objects are sometimes predictable, we propose a prediction-based energy saving scheme, called PES, to reduce the energy consumption for object tracking under acceptable conditions. We compare PES against the basic schemes we proposed in the paper to explore the conditions under which PES is most desired. We also test the effect of some parameters related to the system workload, object moving behavior and sensing operations on PES through extensive simulation. Our results show that PES can save significant energy under various conditions. [C1572]

"Partial tag comparison: a new technology for power-efficient set-associative cache designs"

We call comparing a small part of two tags a Partial Comparison. In this paper, we show that the partial comparison method can filter out most of the unmatched tag comparisons for different cache configurations. The delay of the partial comparison operation is only 60% of that of the full comparison. This paper proposes to use the partial comparison technique to reduce energy dissipation on major cache components of set-associative caches. We show that when adaptive schemes based on partial comparison are applied to amplifiers and bit-lines, the power consumption of set-associative caches is similar to that of direct-mapped caches. We used the CACTI cache model to evaluate the proposed cache architecture and the Simplescalar CPU simulator to produce final results. The power simulation results suggest that the proposed set-associative cache architecture is very power-efficient. In the simulated cache configurations, 25%-60% of cache accessing energy was saved. [C1573]

"Automatic tuning of two-level caches to embedded applications"

The power consumed by the memory hierarchy of a microprocessor can contribute to as much as 50% of the total microprocessor system power, and is thus a good candidate for optimizations. We present an automated method for tuning two-level caches to embedded applications for reduced energy consumption. The method is applicable to both a simulation-based exploration environment and a hardware-based system prototyping environment. We introduce the two-level cache tuner, or TCaT-a heuristic for searching the huge solution space of possible configurations. The heuristic interlaces the exploration of the two cache levels and searches the various cache parameters in a specific order based on their impact on energy. We show the integrity of our heuristic across multiple memory configurations and even in the presence of hardware/software partitioning-a

common optimization capable of achieving significant speedups and/or reduced energy consumption. We apply our exploration heuristic to a large set of embedded applications. Our experiments demonstrate the efficacy of our heuristic: on average the heuristic examines only 7% of the possible cache configurations, but results in cache sub-system energy savings of 53%, only 1% more than the optimal cache configuration. In addition, the configured cache achieves an average speedup of 30% over the base cache configuration due to tuning of cache line size to the application's needs. [C1574]

"Power minimization in a backlit TFT-LCD display by concurrent brightness and contrast scaling"

This paper presents a concurrent brightness and contrast scaling (CBCS) technique for a cold cathode fluorescent lamp (CCFL) backlit TFT-LCD display. The proposed technique aims at conserving power by reducing the backlight illumination while retaining the image fidelity through preservation of the image contrast. First, we explain how CCFL works and show how to model the non-linearity between its backlight illumination and power consumption. Next, we propose the contrast distortion metric to quantify the image quality loss after backlight scaling. Finally, we formulate and optimally solve the CBCS optimization problem with the objective of minimizing the fidelity and power metrics. Experimental results show that an average of 3.7X power saving can be achieved with only 10% of contrast distortion. [C1575]

"Low static-power frequent-value data caches"

Static energy dissipation in cache memories will constitute an increasingly larger portion of total microprocessor energy dissipation due to nanoscale technology characteristics and the large size of on-chip caches. We propose to reduce the static energy dissipation of an on-chip data cache by taking advantage of the frequent values (FV) that widely exist in a data cache memory. The original FV-based low-power cache design aimed at only reducing dynamic power, at the cost of a 5% slowdown. We propose a better design that reduces both static and dynamic cache power, and that uses a circuit design that eliminates performance overhead. A designer can utilize our architecture by simulating an application and then synthesizing the FVs into an application-specific cache design when values will not change, or by simulating and then writing to an FV-cache with configuration registers when values could change. Furthermore, we describe hardware that can dynamically determine FVs and write to the configuration registers completely transparently. Experiments on 11 Spec 2000 benchmarks show that, in addition to the dynamic power savings, 33% static energy savings for data caches can be achieved. [C1576]

"Cool-Fetch: a compiler-enabled IPC estimation based framework for energy reduction"

With power consumption becoming an increasingly important factor, it is necessary to reevaluate traditional, power-intensive, architectural techniques and their relative performance benefits. We believe that combined architecture-compiler efforts open up new and efficient ways to retain the performance benefits of modern architectures while addressing their power impact. In this paper, we present Cool-Fetch, an architecture compiler based approach to reduce energy consumption in the processor. While we mainly target the fetch unit, an important side-effect of our approach is that we obtain energy savings in many other parts of the processor. The explanation is that the fetch unit often runs substantially ahead of execution, bringing in instructions to different stages in the processor that may never be executed. We have found that although the degree of instruction level parallelism (ILP) of a program tends to vary over time, it can be statically estimated by the compiler. Our instructions per clock (IPC) estimation scheme uses monotonic dataflow analysis and simple heuristics, to guide a fetch-throttling mechanism. We develop the necessary architecture support and include its power overhead. Using Mediabench and SPEC2000 applications, we obtain up to 15% total energy savings in the processor with generally little performance degradation. We also provide a comparison of Cool-Fetch with previously proposed hardware-only dynamic fetch-throttling schemes. [C1577]

"Compiler-directed physical address generation for reducing dTLB power"

Address translation using the Translation Lookaside Buffer (TLB) consumes as much as 16% of the chip power on some processors because of its high associativity and access frequency. While prior work has looked into optimizing this structure at the circuit and architectural levels, this paper takes a different approach of optimizing its power by reducing the number of data TLB (dTLB) lookups for data references. The main idea is to keep translations in a set of translation registers, and intelligently use them in software to directly generate the physical addresses without going through the dTLB. The software has to work within the confines of the translation registers provided by the hardware, and has to maximize the reuse of such translations to be effective. We propose strategies and code transformations for achieving this in array-based and pointer-based codes, looking to optimize data accesses. Results with a suite of Spec95 array-based and pointer-based codes show dTLB energy savings of up to 73% and 88%, respectively, compared to directly using the dTLB for all references. Despite the small increase in instructions executed with our mechanisms, the approach can in fact

provide performance benefits in certain cases. [C1578]

"Peak shaving-a method to reduce utility costs"

By thinking out of the box, Baldor Electric Company has been able to save about $1 million a year in energy savings corporate-wide for each of the last three years. Over $100,000 a year of this savings comes from our Westville, OK plant. This paper will discuss Baldor's success reducing utility costs at a motor plant in Westville, Oklahoma by working with the local electricity supplier (Ozarks Electric Cooperative Corp) and practicing peak shaving during summer months. After the plant had adopted all current energy saving methods such as use of NEMA Premium™ electric motors, adjustable speed drives and high-efficiency lighting systems, additional savings were desired. Ozarks Electric Cooperative was also interested in a reduction in the plant's electrical demand during the peak season to unload their system. The co-author is Keith Kaderly from the utility to give a win-win perspective on the project from the utility's viewpoint. [C1579]

"Distributed embedded systems for low power: a case study"

Summary form only given. A multiple-processor system can potentially achieve higher energy savings than a single processor, because the reduced workload on each processor creates new opportunities for dynamic voltage scaling (DVS). However, as the cost of communication starts to match or surpass that of computation, many new challenges arise in making DVS effective in a distributed system under communication-intensive workload. We discuss implementation issues for supporting DVS on distributed embedded processors. We implemented and evaluated four distributed schemes: (1) DVS during I/O, (2) partitioning, (3) power-failure recovery, and (4) node rotation. We validated the results on a distributed embedded system with the Itsy pocket computers connected by serial links. Our experiments confirmed that a distributed system can create new DVS opportunities and achieve further energy savings. However, a surprising result was that aggregate energy savings do not translate directly into a longer battery life. In fact, the best partitioning scheme, which distributed the workload onto two nodes and enabled the most power-efficient CPU speeds at 30-50%, resulted in only 15% improvement in battery lifetime. Of the four techniques evaluated, node rotation showed the most measurable improvement to battery lifetime at 45% by balancing the discharge rates among the nodes. [C1580]

"The Hi-Lo Bi-Track System"

The Hi-Lo Bi-Track System is an innovative technology that provides appropriate superelevations on curves to suit both high-speed passenger trains and low-speed freight trains. Adoption of the Hi-Lo Bi-Track System would provide the following benefits: (a) permit creation of high-speed lines for passenger trains over existing freight train rights-of-way without compromising performance of either train technology; (b) provide improvement in typical train trip times due to reduced need for speed reduction at curves; (c) provide savings in energy consumption due to less braking for curves and subsequent acceleration back to line speed; (d) provide better performance then "tilting trains" in reducing typical train trip times; (e) avoid high vertical and lateral track forces resulting from operation of "tilting trains"; and (f) applicable to high-speed mail and express freight trains in addition to high-speed passenger trains. [C1581]

"Joint content authentication and error control for wireless multimedia communications"

Today, multimedia delivery through wireless networks is rapidly gaining popularity. Many cellular phones are already equipped with an extra large full-color display and various multimedia applications and devices. It is challenging to transmit and access multimedia data through wireless communications channels due to device mobility, power constraints, bandwidth limitations, and an error prone environment. We investigate multimedia services in wireless networks. We propose an integrated service approach for authentication and error control (including error detection, recovery and concealment) that potentially reduces bandwidth requirement and power consumption. Authentication is used in secure wireless communications to ensure the integrity of a message, i.e., that it has not been tampered with and that it originated with the presumed transmitter. To combat transmission errors with the least additional bandwidth requirement, error concealment can be used to obtain a close approximation of the original signal at the receiver end. The efficiency and effectiveness of an error recovery technique rely on the system error detection capabilities. Traditionally, those problems are treated separately using different schemes. We investigate the problem at the application layer, and design a joint media authentication and error control scheme to reduce cost and save resources. Simulation results show that the proposed scheme is efficient and effective. [C1582]

"Integrated rate control and entropy coding for JPEG 2000"

In this paper, we present an integrated rate control and entropy coding (IREC) scheme for JPEG 2000. Based on an efficient heap-based rate allocation algorithm, the characteristics of image content, the subband coefficient

and bitplane weighting models, and the user-specified optimization criteria, the proposed IREC scheme can selectively perform entropy coding only on those parts of image data that are likely to be included in the final bitstream. Since entropy coding is the most time and power consuming part, the IREC scheme can then reduce the overall computation and power consumption of JPEG 2000 encoding procedure. Both theoretical analysis and empirical results validate the advantages of the IREC scheme. For example, when encoding the Lenna color image with a targeted compression ratio of 128:1, compared with the separate rate control and entropy coding schemes, about 93% savings in computation and power consumption can be achieved on the entropy coding procedure. [C1583]

"Optimizing bus energy consumption of on-chip multiprocessors using frequent values"

Chip multiprocessors (CMP) are a convenient way of leveraging from the technological trends to build high-end and embedded systems that are performance and power efficient, while exhibiting attractive properties such as scalability, reliability and ease of design. However, the onchip interconnect for moving the data between the processors, and between the processors and memory subsystem, plays a crucial role in CMP design. We present a novel approach to optimizing its power by exploiting the value locality in data transfers between processors. A communicating value cache (CVC) is proposed to reduce the number of bits transferred on the interconnect, and simulation results with several parallel applications show significant energy savings with this mechanism. Results show that the importance of our proposal will become even more significant in the future. [C1584]

"ZBP: a zone-based broadcasting protocol for wireless sensor networks"

Wireless sensor networks (WSNs) have been widely used in monitoring and collecting information. Packet flooding or broadcasting is an essential function for establishing a communication path from the sink node to a region of sensor nodes. However, flooding operation consumes power and bandwidth resources and raises the packet collision and contention problems, which reduce the success rate of packet transmissions and consume energy. This article proposes an efficient broadcasting protocol to reduce the number of sensor nodes that forward the query request, hence improving the packet delivery rate and saving bandwidth and power consumptions. The sensor node that received the query request dynamically transfers the coordinate system according to the zone-ID of the source node and determines whether it would forward the request or not in a distributed manner. Compared with a traditional flooding operation, experimental results show that the proposed zone-based broadcasting protocol decreases the bandwidth and power consumptions, reduces the packet collisions, and achieves a high success rate of packet broadcasting. [C1585]

"Hybrid greedy/multicasting power-aware routing protocol in ad hoc networks"

Traditional routing algorithms tend to use shortest path algorithms with minimum hop count to reduce transmission latency and error rates, resulting in a quick exhaustion of a small subset of nodes where the traffic load is heavy and risking a disconnection of the entire network. We define a new power-aware cost metric with the aim of reflecting both power-saving perspectives: maximizing network lifetime and minimizing the power consumption of a routing task. We also propose a new location-aided, power-aware routing protocol that is based on a combination of greedy and multicasting strategies. The decision on applying greedy or multicasting within its routing zone depends on the link cost and the node's neighborhood distribution. Simulation results show that performances on network lifetime and average power consumption for routing tasks are greatly improved without sacrifices in the delivery rate of the ad hoc network. [C1586]

"Construction of power efficient routing tree for ad hoc wireless networks using directional antenna"

In ad hoc wireless networks, nodes are typically powered by batteries. Therefore saving energy has become a very important objective, and different algorithms were proposed to achieve power efficiency during the routing process. Directional antenna was suggested to further decrease transmission energy as well as to reduce interference. We discuss three algorithms for routing tree construction that take advantage of directional antenna, i.e, Simple-Linear (SL), Linear-Insertion (LI), and Reverse-Cone-Pairwise (RCP). Their performances are compared through a simulation study. [C1587]

"A cross-layer energy-saving mechanism for an enhancement of 802.11 WLAN systems"

Most multiple access collision avoidance-based (MAC) protocols for WLAN systems have been using fixed transmission power and have not considered energy-saving techniques targeted on channel estimation models. In order to prolong battery life and to improve the overall throughput performance of such systems, a novel PHY-MAC cross-layer energy-saving mechanism based on a distributed queuing MAC protocol and fuzzy logic theory is introduced for WLAN systems. Computer simulations have been performed and values for the throughput

maximum performance and energy consumption have been obtained as a function of different scenario parameters. These values show that the throughput outperforms the one obtained with the IEEE 802.11 standard while reducing the energy consumption. [C1588]

"A power-efficient MAC protocol for integrated voice and data services over 802.11e HCF"

A novel power-efficient MAC protocol, named on-demand polling (ODP) scheme, is presented for supporting integrated voice and data services over WLAN. The ODP scheme combines the polling-based and the contention-based mechanisms over HCF (hybrid coordination function). In the ODP scheme, a voice station is in the polling list when it is in the active mode. During the idle mode, it is configured to operate in the sleep mode for saving power. Also, it adopts the contention-based mechanism to join the list again when returning from the idle mode. In this paper, we investigate the RR-Brady, the RR-CBR and the proposed ODP schemes and derive the power consumption and the aggregate throughput for voice and data stations, respectively. Simulation results show that the ODP scheme can reduce the power consumption for voice stations and enhance the throughput for data stations. [C1589]

"Memory-Aware Energy-Optimal Frequency Assignment for Dynamic Supply Voltage Scaling"

Dynamic supply voltage scaling (DVS) is one of the best ways to reduce the energy consumption of a device when there is a super-linear relationship between energy and supply voltage, and a pseudo-linear relationship between delay and supply voltage. However, most DVS schemes scale the clock frequency of the supply-voltage-clock-scalable (SVCS) CPU only and do not address the energy consumption of the memory. The memory is generally non-supply-voltage-scalable (NSVS), but its energy consumption is variable to its clock frequency and the total execution time. Thus, DVS for an SVCS CPU cannot achieve an optimal system-wide energy saving without consideration of the memory, as far as it is controlled by an SVCS CPU. We introduce an energy-optimal frequency assignment, for both an SVCS CPU and a synchronous NSVS memory, which optimizes the system-wide energy consumption. We derive the energy-optimal clock frequencies for an SVCS CPU and a synchronous NSVS memory, as a function of the number of processor clock cycles, the number of memory accesses and the hardware energy model. Our technique modifies the frequency assignment of the CPU and the memory used in previous DVS schemes, which ignore the memory energy. It enables the system-wide energy-optimal settings and achieves additional 50% energy reduction over previous DVS schemes. This technique can also be applicable to synchronous NSVS peripheral devices. [C1590]

"Novel optimum reduced search MLSE decoding algorithm enabling system-aware power savings"

The amount of control signaling required by a wide range of wireless services to reconfigure system and architecture parameters at runtime is expected to increase significantly. Low-power design constraints force the decoding complexity to be kept to a minimum in such "continuous monitoring" scenarios. We propose a novel reduced search concept which can be adapted to MLSE-based algorithms to reduce the processing complexity without altering the communication performance. Power consumption reductions of up to 45% have been observed for TFCI and up to 50% for HS-SCCH (both 3GPP specific) decoding implemented on the ST122 DSP-MCU in a 0.13 μm CMOS technology. [C1591]

"Reducing overhearing energy in 802.11 networks by low-power interface idling"

In this paper we propose and analyze a new interface idling mechanism for improving energy efficiency of IEEE 802.11 based MAC hardware. A novel protocol state analysis technique is developed for detecting time windows during which a wireless interface consumes energy due to 802.11 overhearing. During this window, energy savings at the MAC layer is accomplished by forcing the wireless interface to a relatively lower-energy idling state. At the end of this window, the interface is transitioned back to its regular receiving mode. Energy savings are realized by exploiting the difference in power consumption between the overhearing state and the idling state. We evaluate the proposed protocol using ns-2 simulator. Simulation experiments validate that the proposed mechanism is capable of significantly reducing overhearing expenditure for newer 802.11 cards that support low-energy idling mode as described above. Our experimentation with Socket Communications Inc. low power 802.11 card demonstrate that the reduction in overhearing expenditure can be up to 23% and the subsequent network life extension can be up to 86% Results also show that the proposed MAC layer idling is fairly insensitive to network loading. [C1592]

"Energy aware data gathering based on adaptive modulation scaling in wireless sensor networks"

Energy consumption has been a key concern of data gathering in wireless sensor networks. Previous research works show that modulation scaling is an efficient technique to reduce energy consumption. However, such a technique also impacts on both packet delivery latency and packet loss, therefore, may result in adverse effects

on the quality of applications. In this paper, we study the problem of modulation scaling and energy optimization. A mathematical model is proposed to analyze the impact of modulation scaling on the overall energy consumption, end-to-end mean delivery latency and mean packet loss rate. A centralized optimal management mechanism is developed, based on the model, which adaptively adjusts the modulation levels to minimize energy consumption while ensuring the QoS for data gathering. Experimental results show that the management mechanism saves significant energy in all the investigated scenarios. Some valuable results are also observed in the experiments. [C1593]

"Query aggregation for providing efficient data services in sensor networks"

Providing efficient data services is one of the fundamental requirements for wireless sensor networks. The data service paradigm requires that the application submit its requests as queries and the sensor network transmits the requested data to the application. While most existing work in this area focuses on data aggregation, not much attention has been paid to query aggregation. For many applications, especially ones with high query rates, query aggregation is very important. We study a query aggregation-based approach for providing efficient data services. In particular: (1) we propose a multi-layered overlay-based framework consisting of a query manager and access points (nodes), where the former provides the query aggregation plan and the latter executes the plan; (2) we design an effective query aggregation algorithm to reduce the number of duplicate/overlapping queries and save overall energy consumption in the sensor network Our performance evaluations show that by applying our query aggregation algorithm, the overall energy consumption can be significantly reduced and the sensor network lifetime can be prolonged correspondingly. [C1594]

"Resource-aware video processing techniques for ambient multimedia systems"

Ambient intelligence (AmI) is the inconspicuous presence of computing into every facet of our lives. AmI systems of the future will contain devices with highly limited resources in terms of processing power, memory, and battery lifetime. Contrary to this are the memory, power, and cycle-hungry video processing applications which are required to provide the level of utility demanded by users. The paper introduces the idea of processing a portion of a video frame with the intent of achieving high levels of video processing performance while reducing considerably the hardware requirements for that processing. The techniques we propose operate only on a portion of the video frame and optionally adjust that portion's size dynamically to match the video content reasonably well. Our results show that this technique can save roughly 75% in both memory and processing cycle requirements and up to 87% in energy consumption, while inducing less than 10% error in XY processing of the video frame [C1595]

"Coding tradeoffs for reduced energy consumption in sensor networks"

We consider the design of error control schemes in wireless sensor networks. Unlike in traditional communications systems, in which coding is almost always beneficial, in sensor networks, the relatively short communications range and the lack of energy resources may lead to different conclusions. In particular, the energy spent for decoding may actually exceed that saved due to the coding gain. In this environment, interesting tradeoffs can be identified and non-traditional ways to perform error control may be proposed. [C1596]

"Alternative run-length coding through scan chain reconfiguration for joint minimization of test data volume and power consumption in scan test"

Test data volume and scan power are two major concerns in SoC test. In this paper we present an alternative run-length coding method through scan chain reconfiguration to reduce both test data volume and scan-in power consumption. The proposed method analyzes the compatibility of the internal scan cells for a given test set and then divides the scan cells into compatible classes. To extract the compatible scan cells we apply a heuristic algorithm by solving the graph coloring problem; and then a simple greedy algorithm is used to configure the scan chain for the minimization of scan power. Experimental results for the larger ISCAS'89 benchmarks show that the proposed approach leads to highly reduced test data volume with significant power savings during scan test. [C1597]

"Search of guidelines for the optimal design of TFR processors"

The paper faces the problem of designing a compact processor devoted to the evaluation of a time-frequency transformation for space applications. The guidelines to save circuitry and power consumption are searched. Starting from the simple Gabor transformation, the effects of the Weyl-Heisenberg indetermination principle are examined in connection with the effects induced by the use of a short wordlength. A simple criterion to choose the optimal wavelet is given and applied to improve the transformations performed using a reduced wordlength. [C1598]

"CHASER: content and channel aware object scheduling and error control for wireless Web access in 3G networks"

A major bottleneck in satisfying the increasing demand for wireless multimedia access is the dynamic error conditions requiring a very high error protection overhead in terms of energy consumption and access delay. In this paper, we explore ways to use application-level data properties to reduce the error protection cost. We observe that the objects constituting a wireless Web-based access differ in terms of the inherent resiliency to residual error, and the object's importance to the overall content quality. Additionally, since the cost of achieving a target residual error level depends on the experienced channel conditions, the access cost can be affected by changing the transmission schedule of objects according to the channel conditions. Based on the above observations, in this paper, we present a framework that exploits the application properties, namely content importance and error resiliency, to reduce the cost of error protection by scheduling objects for transmission and adapting the lower-layer error control mechanisms based on the data properties as well as wireless channel conditions. The approach is evaluated under diverse channel conditions using a MATLAB-based simulation environment. Our results show that the proposed approach leads to significant savings in access cost (average 37.4%) with minimal degradation in application quality. [C1599]

"The effects of energy management on reliability in real-time embedded systems"

The slack time in real-time systems can be used by recovery schemes to increase system reliability as well as by frequency and voltage scaling techniques to save energy. Moreover, the rate of transient faults (i.e., soft errors caused, for example, by cosmic ray radiations) also depends on system operating frequency and supply voltage. Thus, there is an interesting trade-off between system reliability and energy consumption. This work first investigates the effects of frequency and voltage scaling on the fault rate and proposes two fault rate models based on previously published data. Then, the effects of energy management on reliability are studied. Our analysis results show that, energy management through frequency and voltage scaling could dramatically reduce system reliability, and ignoring the effects of energy management on the fault rate is too optimistic and may lead to unsatisfied system reliability. [C1600]

"A Way-Halting Cache for Low-Energy High-Performance Systems"

Caches contribute to much of a microprocessor system's power and energy consumption. We have developed a new cache architecture, called a way-halting cache, that reduces energy while imposing no performance overhead. Our way-halting cache is a four-way set-associative cache that stores the four lowest-order bits of all ways' tags into a fully associative memory, which we call the halt tag array. The lookup in the halt tag array is done in parallel with, and is no slower than, the set-index decoding. The halt tag array pre-determines which tags cannot match due to their low-order four bits mismatching. Further accesses to ways with known mismatching tags are then halted, thus saving power. Our halt tag array has an additional feature of using static logic only, rather than dynamic logic used in highly associative caches. We provide data from experiments on 17 benchmarks drawn from MediaBench and Spec 2000, based on our layouts in 0.18 micron CMOS technology. On average, 55% savings of memory-access related energy were obtained over a conventional four-way set-associative cache. We show that energy savings are greater than previous methods, and nearly twice that of highly-associative caches, while imposing no performance overhead and only 2% cache area overhead. [C1601]

"A power-saving implementation of generalized selection combining by output thresholding"

Generalized selection combining (GSC) delivers the largest possible diversity benefit for a given hardware-complexity constraint. However, it also increases the power consumption of the receiver with the path selection and the maximum ratio combining (MRC) operations. In this paper, we investigate a variant of GSC, termed output thresholded GSC (OT-GSC). More specifically, to reduce the power consumption of the GSC scheme, we introduce a threshold check at the GSC combiner output. The resulting OT-GSC combiner tries to raise the signal to noise ratio of the combined signal above a threshold by using the least combiner resources (in terms of path estimations and active MRC branches) possible. The tradeoff between power consumption and performance is illustrated with selected numerical examples. [C1602]

"Optimizing mode transition sequences in idle intervals for component-level and system-level energy minimization"

New embedded systems offer rich power management features in the form of multiple operational and nonoperational power modes. While they offer mechanisms for better energy efficiency, they also complicate power management decisions in the presence of realtime constraints. A traditional dynamic power management

techniques based on localized break-even-time analysis with simple on/off power controls often yield suboptimal if not incorrect results globally. To address these problems, This work presents two core algorithms for reducing idle energy consumption at the component level and system level. The first algorithm discovers the optimal sequence for mode transition over multiple power modes under timing constraints. It assists the second algorithm that performs a sophisticated global search strategy to aggressively explore system-wide energy savings by correctly interpreting the constraints across all subsystems. Experimental results show that in an embedded radio system where idle energy cost matches or exceeds the active energy consumption, our technique can further reduce the idle energy by 50-70%, which translates into 30-50% of overall system energy compared to existing techniques. [C1603]

"Asynchronous power management scheme for wireless ad-hoc networks"

In wireless ad-hoc networks, power-saving by the terminals is a very important issue since their operation depends on limited battery-power. To reduce their power consumption the terminals are allowed to enter a low-power mode (LPM) in many wireless networks. However, as there is no clock synchronization of information transmission in ad-hoc networks, the problem occurs that terminals do not know when a neighboring terminal in LPM awakes. We propose a novel power management scheme using SLEEP _TABLE to solve this problem. Simulation results show that the proposed scheme outperforms 802.11 LPM and the conventional scheme in terms of power saving, and the power consumption of each terminal is distributed. [C1604]

"A multiplexer based decoder for flash analog-to-digital converters"

A decoder for flash analog-to-digital converters with short critical path, regular structure, and small area is presented. The decoder is based on 2:1 multiplexers connected as a tree. Each level of the tree divides the input thermometer scale in two and calculates one of the bits in the binary output. In comparison with the Wallace tree decoder and the folded decoder the length of the critical path is approximately reduced to one third and one half, respectively. The amount of hardware is also reduced, which is likely to translate to a power saving, compared with the Wallace tree decoder and the folded decoder. [C1605]

"Traffic aware dynamic node scheduling for power efficient sensor networks"

The paper proposes a new medium-access control (MAC) protocol designed for wireless sensor networks. A wireless sensor network is an array of a large number of sensors interconnected by a multi-hop ad-hoc network. The primary objective for the sensor network is achieving low-power consumption while latency is usually less important compared to traditional wireless networks. This characteristic of a sensor network motivates the design of a new MAC layer so that power consumption is reduced. A novel traffic-aware algorithm based on distributed node schedule management (DMD) protocol is introduced that utilizes a distributed dynamic node scheduling strategy to increase energy saving dramatically, especially in intermediate devices inside a multi-hop network. Simulation results show noticeable power consumption improvements compared to 802.11-like, sensor MAC and dynamic SMAC protocols, especially on the large scale; this has been achieved at the expense of higher latency. [C1606]

"Reducing Energy Consumption of Disk Storage Using Power-Aware Cache Management"

Reducing energy consumption is an important issue for data centers. Among the various components of a data center, storage is one of the biggest consumers of energy. Previous studies have shown that the average idle period for a server disk in a data center is very small compared to the time taken to spin down and spin up. This significantly limits the effectiveness of disk power management schemes. This paper proposes several power-aware storage cache management algorithms that provide more opportunities for the underlying disk power management schemes to save energy. More specifically, we present an off-line power-aware greedy algorithm that is more energy-efficient than Belady's off-line algorithm (which minimizes cache misses only). We also propose an online power-aware cache replacement algorithm. Our trace-driven simulations show that, compared to LRU, our algorithm saves 16% more disk energy and provides 50% better average response time for OLTP I/O workloads. We have also investigated the effects of four storage cache write policies on disk energy consumption. [C1607]

"On the effectiveness of dynamically allocating resources across program execution phases for media workloads"

Processing embedded applications is essentially a trade-off between power and performance. Increasing level of complexity in present day microprocessor at the expense of more power call for different optimization methodologies at architecture level. The study of general characteristics of program execution phases gives insight to dynamically reconfigure or enable/disable additional resources on-demand basis. This leads to

significant amount of power saving with negligible or tolerable performance degradation. We characterize execution of such programs into execution phases based on their dynamic IPC profile. We show that program execution of selected phases (based on IPC profile) can be dynamically boosted by activating additional standby functional units which are otherwise powered down for saving energy. Through simulation we show that speedup ranging from 1.1 to 1.25 can be achieved while reducing the energy-delay product (EDP) for most of the media benchmarks evaluated. [C1608]

"A new dual transmission gate adiabatic logic and design of an 8Ч8-bit multiplier for low-power DSP"

This paper presents an adiabatic multiplier for low-power DSP. A dual transmission gate adiabatic logic (DTGAL) suitable for pipelined structures is described. It can recover the charge of load nodes by using feedback control from next-stage buffer outputs to realize power-efficient design. An 8Ч8-bit adiabatic multiplier based on our DTGAL is designed. The power consumption of the proposed multiplier is significantly reduced because the energy transferred to the load capacitance is mostly recovered. Functional and energy simulations are performed for the multiplier using the net-list extracted from its layout. HSPICE simulations indicate energy savings of 65% to 85% as compared to the conventional CMOS implementation for clock rates ranging from 25 to 200 MHz. [C1609]

"The pulse protocol: sensor network routing and power saving"

We present a performance evaluation of the pulse protocol operating in a sensor network. In this work, a number of modifications are made to the original pulse protocol to provide efficient operation in a sensor network environment. The pulse protocol utilizes a periodic flood (the pulse) initiated by a single node (the pulse source) to provide both routing and synchronization to the network. This periodic pulse forms a pro-actively updated spanning tree rooted at the pulse source. Nodes communicate by forwarding packets through this tree. In addition, nodes are able to synchronize with the periodic pulse, allowing idle nodes to power off their radios a large percentage of the time when they are not required for packet forwarding. This results in substantial energy savings. A new mechanism called intermediate wake-up periods is introduced in this work in order to reduce the energy costs of low delay applications. Through simulation we explore the performance of both the protocol and the modifications with respect to energy efficiency and delay. [C1610]

"Clustering sensor networks using growing self-organising map"

Sensor networks consist of wireless enabled sensor nodes with limited energy. As sensors could be deployed in a large area, data transmitting and receiving are energy consuming operations. One of the methods to save energy is to reduce the transmission distance of each node by grouping nodes into clusters. Each cluster has a cluster-head (CH), which communicates with all the other nodes of that cluster and transmits the data to the remote base station. We describe the adaptation of a growing self-organising map (GSOM) to cluster the wireless sensor nodes and to identify the cluster-heads. We compare the results with a well-known clustering algorithm. We also describe the energy minimization criterion for clustering. [C1611]

"Micro-architecture optimization of THUMP105 SOC implementation"

At microarchitectural level this paper presents our research on performance-constraint problems for VLSI system design with IP and VC cores. With 32bit embedded and low-power processor THUMP105 as an example, delay complexity measure of control module, and signal noise ratio (SNR) of special managing request (SMR) signals were discussed to evaluate final performance and power consumption. Optimized results of THUMP105 indicated that the critical path delay was reduced by 46.8% at same supply voltage, which means that the lower supply voltage can be employed resulting in significant power saving with same performance constraints. [C1612]

"SRDA: secure reference-based data aggregation protocol for wireless sensor networks"

Data aggregation in wireless sensor networks eliminates data redundancy, thereby improving bandwidth usage and energy utilization. The paper presents a secure data aggregation protocol, called SRDA (secure reference-based data aggregation), for wireless sensor networks. In order to reduce the number of bits transmitted, sensor nodes compare their raw sensed data value with their reference data value and then transfer only the difference data. In addition to reducing the number of transmitted bits, SRDA also establishes secure connectivity among sensor nodes without any online key distribution. The security level of the communication links is gradually increased as packets are transmitted at higher level cluster-heads, since intercepting a packet at higher levels of the clustering hierarchy provides a summary of a large number of transmissions at lower levels. Simulation results show that the proposed protocol yields significant savings in energy consumption while preserving data

security. [C1613]

"A case study of an integrated conveyor belt model for the mining industry"

The energy cost is one of the largest components of operating costs on a belt conveyor system. The majority of papers on energy savings on conveyor systems focus on the mechanical improvement of the conveyor system in order to save energy. In This work the model that was developed to simulate the energy consumption patterns of the conveyor belts will be introduced and explained by means of a case study from industry. The model focuses on load scheduling as a means of energy management rather reducing the amount of energy consumption. [C1614]

"Power-efficient scheduling method in sensor networks"

Advances in micro-sensor and radio technology would enable the deployment of small but smart sensors for various environmental monitoring applications. Generally, the sensor node cannot recharge and the battery life is not expected to increase significantly in the future. Reducing power consumption and providing efficient power savings are crucial points in sensor networks. From the related research, this study generalizes four cases of power waste and consumption, as follows: collision, sparse node, overhead and listen. The proposed method can avoid those four case of power consumption and waste case. Numerous studies demonstrate that sleeping mode is merely a method for power saving. Thus This work utilized those previous related works results about power saving, every node according to schedule working, the other node enters the sleeping mode until it needs to work again. Simulation results demonstrated that the proposed approach performs between 150% and 250% better than PEGASIS when 10%, 20%, 50%, and 100% of nodes die in different sensor network sizes and topologies. [C1615]

"Power consumption reduction by multi-hop transmission in cellular networks"

Multi-hop transmission breaks the single-hop path from a mobile station to the base station into two or more hops. In this case, distances between transmitters and receivers are smaller than that in the direct transmission case, hence it is expected that transmit power will be greatly reduced. In this paper, we analyze the probability that a mobile station can find its relay, and the average power consumption of mobile stations and their relays compared to the power consumption in case of direct transmission. As the number of relaying stations increases, it is highly probable that mobile stations can find their relay and save power. The gain of power saving through a two-hop relay is much greater when the path loss becomes greater. [C1616]

"Exploiting prediction to reduce power on buses"

We investigate coding techniques to reduce the energy consumed by on-chip buses in a microprocessor. We explore several simple coding schemes and simulate them using a modified SimpleScalar simulator and SPEC benchmarks. We show an average of 35% savings in transitions on internal buses. To quantify actual power savings, we design a dictionary based encoder/decoder circuit in a 0.13 μm process, extract it as a netlist, and simulate its behavior under SPICE. Utilizing a realistic wire model with repeaters, we show that we can break even at median wire length scales of less than 11.5 mm at 0.13 μ and project a break-even point of 2.7 mm for a larger design at 0.07 μ. [C1617]

"Program counter based techniques for dynamic power management"

Reducing energy consumption has become one of the major challenges in designing future computing systems. We propose a novel idea of using program counters to predict I/O activities in the operating system. We present a complete design of program-counter access predictor (PCAP) that dynamically learns the access patterns of applications and predicts when an I/O device can be shut down to save energy. PCAP uses path-based correlation to observe a particular sequence of program counters leading to each idle period, and predicts future occurrences of that idle period. PCAP differs from previously proposed shutdown predictors in its ability to: (1) correlate I/O operations to particular behavior of the applications and users, (2) carry prediction information across multiple executions of the applications, and (3) attain better energy savings while incurring low mispredictions. [C1618]

"A load shedding controller for management of residential loads during peak demand periods"

South Africa is experiencing an unprecedented increase in electricity consumption. A direct consequence of this increased demand is the enormous load burden that has been imposed on the nation's national electricity grid, especially during peak demand periods. One solution to this problem would be the construction of additional power generating facilities, at a great cost to the economy and more importantly the environment. A more viable

solution would be to shift loads off the electricity grid's peak consumption demand periods. To this end we will propose a controller that will reduce the residential load demand burden on the electricity supply grid, plus improve the load factor. The proposed controller allows the user to adjust the threshold setpoint at which the controller must operate. The controller performs the necessary load shedding operations when the setpoint is exceeded. The efficacy of the proposed controller was assessed by managing the load demands of residential consumers. A comparison was made between residential peak period consumption, under controlled and uncontrolled conditions. These comparisons were based on the following aspects: total consumption, maximum demand and load factor. The cost of consumption for each customer was calculated by using a flat rate tariff. The tests demonstrated the following: increases in consumer savings, a significant reduction in maximum demand on the electricity grid during peak consumption periods and improvements in load factor. [C1619]

"On the use of high bit rate transceivers for low duty cycle wireless sensor networks"

In most wireless sensor network applications reducing the energy consumption of each node has highest optimisation priority to allow sensor nodes to operate for an extended period of time. The radio transceiver plays an especially important role in this regard, because it typically consumes most of the nodes energy. Up to now only low bit rate radio transceivers (up to 115 kbps) were proposed for the use in sensor applications which leads to a sub optimal node efficiency. In This work the use of commercially available high bit rate (≥ 1 Mbps) transceivers for low duty cycle, ultra low power wireless sensor networks is proposed. Using state of the art high bit rate transceivers with an efficient MAC protocol such as the recently proposed CSMA-MPS can save considerable energy at the physical layer. [C1620]

"An energy efficient select optimal neighbor protocol for wireless ad hoc networks"

We propose two location-aware select optimal neighbor (SON) algorithms that are suitable for CSMA/CA based MAC protocols for wireless ad hoc networks. Both algorithms optimize the energy efficiency by reducing the effective number of neighbors and thus reduce the transmission power as well as the overhearing power consumption at irrelevant receivers. NS-2 simulations show that our algorithms can achieve about 28% and 38% average energy savings per node compared to CSMA/CA based MAC protocols such as IEEE 802.11. [C1621]

"Design of circuits for a robust clocking scheme"

The design of a clock distribution network in a digital integrated circuit is challenging in terms of obtaining low power consumption, low waveform degradation, low clock skew and low simultaneous switching noise. In this work we aim at alleviating these design restrictions by using a clock buffer with reduced size and a D flip-flop circuit with relaxed constraints on the rise and fall times of the clock. According to simulations the energy dissipation of a D flip-flop, implemented in a 0.35 μm process, increases with only 21% when the fall time of the clock is increased from 0.05 ns to 7.0 ns. Considering that smaller clock buffers can be used there is a potential of power savings by using the suggested clocking scheme. [C1622]

"Toggle-masking for test-per-scan VLSI circuits"

This paper presents a novel toggle-masking technique that eliminates the switching activity in a circuit under test (CUT) during the scan-shifting in a test-per-scan test. Conventional scannable D flip-flops (DFFs) are modified to ensure that CUT inputs remain unchanged until an entire test vector is loaded, significantly reducing the power dissipation in the CUT. Our experiments on ISCAS85/89 benchmark circuits show that the proposed technique offers an average of 47% savings in average power compared to previous work (S. Gerstendorfer and H. Wunderlich, Proc. Int. Test Conf., pp. 77-84, 1999), and an average of 99% savings in average power and 8% savings in peak power with respect to test-per-scan circuits with conventional DFFs. [C1623]

"Including Kyoto in electrical engineering curriculum"

The paper describes the response to the changing aspirations of first degree electrical engineering students to learn more about energy questions. It begins by reviewing energy use and carbon emissions, with particular emphasis to electricity consumption. Next, the Kyoto Protocol, which imposes to reduce Canadian greenhouse gas (GHG) emissions to 6% below 1990 levels by 2008-2012 is described. In the year 2000, Canada's GHG emissions were 20% above the 1990 reference level. So, the gap between Canada's Kyoto commitment and our total projected emissions is becoming alarmingly large. It is indicated that Canada can reach its target by using classical energy saving mechanisms, as well as Kyoto implementation mechanisms. It is concluded that the implementation of the new teaching material in electrical engineering education can make students able to obtain further insight in energy questions and induce the promotion of technological options for long term sustained emissions reduction. [C1624]

"A novel low-power adiabatic SRAM with an energy-efficient line driver"

A novel 64Ч64 bit adiabatic SRAM is designed using 0.25 μm CMOS technology. An adiabatic line driver, which does not have non-adiabatic loss on output loads through using feedback control from the next-stage buffer, is used to recover the charge of the large switching capacitance on the bit-lines and word-lines in a fully adiabatic manner. The power consumption of the proposed SRAM is significantly reduced because the energy transferred to the large capacitance buses is mostly recovered. The energy and functional simulations are performed using the net-list extracted from the layout. HSPICE simulation results indicate energy savings of 75% to 85%, as compared to the conventional CMOS implementation, for clock rates ranging from 25 to 200 MHz. [C1625]

"Dynamic voltage and frequency scaling based on workload decomposition"

This paper presents a technique called "workload decomposition" in which the CPU workload is decomposed in two parts: on-chip and off-chip. The on-chip workload signifies the CPU clock cycles that are required to execute instructions in the CPU whereas the off-chip workload captures the number of external memory access clock cycles that are required to perform external memory transactions. When combined with a dynamic voltage and frequency scaling (DVFS) technique to minimize the energy consumption, this workload decomposition method results in higher energy savings. The workload decomposition itself is performed at run time based on statistics reported by a performance monitoring unit (PMU) without a need for application profiling or compiler support. We have implemented the proposed DVFS with workload decomposition technique on the BitsyX platform, an Intel PXA255-based platform manufactured by ADS Inc., and performed detailed energy measurements. These measurements show that, for a number of widely used software applications, a CPU energy saving of 80% can be achieved for memory-bound programs while satisfying the user-specified timing constraints. [C1626]

"Power-optimal pipelining in deep submicron technology"

This paper explores the effectiveness of pipelining as a power saving tool, where the reduction in logic depth per stage is used to reduce supply voltage at a fixed clock frequency. We examine power-optimal pipelining in deep submicron technology, both analytically and by simulation. Simulation uses a 70 nm predictive process with a fanout-of-four inverter chain model including input/output flipflops, and results are shown to match theory well. The simulation results show that power-optimal logic depth is 6 to 8 FO4 and optimal power saving varies from 55 to 80% compared to a 24 FO4 logic depth, depending on threshold voltage, activity factor, and presence of clock-gating. We decompose the power consumption of a circuit into three components, switching power, leakage power, and idle power, and present the following insights into power-optimal pipelining. First, power-optimal logic depth decreases and optimal power savings increase for larger activity factors, where switching power dominates over leakage and idle power. Second, pipelining is more effective with lower threshold voltages at high activity factors, but higher threshold voltages give better results at lower activity factors where leakage current dominates. Lastly, clock-gating enables deeper pipelining and more power saving because it reduces timing element overhead when the activity factor is low. [C1627]

"Design and implementation of scalable low-power Montgomery multiplier"

In this paper, an efficient Montgomery multiplier is introduced for the modular exponentiation operation, which is fundamental to numerous public-key cryptosystems. Four aspects are considered: performance, power, reliability, and scalability. To increase performance, the architecture is based on the radix-4 carry-save adder (CSA). To lower power consumption, we devised several effective techniques for reducing the spurious transitions and the expected switching activity (ESA) of high fan-out signals. To achieve scalability, we implement a 4-fold nested loop for the whole data processing flow. It is compatible with the multiple-precision digit-serial arithmetic as well as the data transfer to/from an external memory. Finally, to make sure that the arithmetic operation runs correctly without inducing data overflow error, we find out the optimum numbers of bits for all vectors appearing in the operation through a mathematical analysis and a logic simulation. In the evaluation of hardware implemented using 0.18 μm CMOS standard library and 4 metal layers, area and current consumption are 59 K gates and 0.4 mA/MHz at 1.8 V supply voltage, respectively. The presented low power techniques save more than 20% of power consumed. [C1628]

"A way-halting cache for low-energy high-performance systems"

Caches contribute to much of a microprocessor system's power and energy consumption. We have developed a new cache architecture, called a way-halting cache, that reduces energy while imposing no performance overhead. Our way-halting cache is a four-way set-associative cache that stores the four lowest-order bits of all ways' tags into a fully associative memory, which we call the halt tag array. The look-up in the hall tag array is done in parallel with, and is no slower than, the set-index decoding. The hall tag array pre-determines which

tags cannot match due to their low-order four bits mismatching. Further accesses to ways with known mismatching tags are then halted, thus saving power. Our halt tag array has an additional feature of using static logic only, rather than dynamic logic used in highly associative caches. We provide data from experiments on 17 benchmarks drawn from MediaBench and Spec 2000, based on our layouts in 0.18 micron CMOS technology, On average, 55% savings of memory-access related energy were obtained over a conventional four-way set-associative cache. We show that energy savings are greater than previous methods, and nearly twice that of highly-associative caches, while imposing no performance overhead and only 2% cache area overhead. [C1629]

"A framework for energy-saving data gathering using two-phase clustering in wireless sensor networks"

A high-density wireless sensor network can be deployed for specific information-gathering. In such a network, sensors need to route their sensed data to a base station, consuming highly-limited and unreplenishable energy resource. Hence, one of the most critical issues in designing sensor data gathering algorithms is to minimize the energy consumption for network longevity while meeting certain requirements given, such as delay constraints, which may vary depending on specific applications or environmental situations. We propose a novel two-phase clustering (TPC) scheme for energy-saving and delay-adaptive data gathering in wireless sensor networks. The proposed scheme partitions the network into clusters in phase I, each with a cluster head, forming a direct link between cluster member and cluster head. In phase II, each cluster member searches for a neighbor closer than the cluster head within the cluster to set up an energy-saving data relay link. The sensors use either the direct link or the data relay link for their sensed data forwarding depending on the requirements specified by the users or applications. Simulation results show that the TPC reduces average transmission distance by up to 75% with the help of data relay links when there is no delay constraint, implying that there is a significant amount of energy-savings in collecting sensed data. [C1630]

"Dynamic filter cache for low power instruction memory hierarchy"

Filter cache (FC) is effective in achieving energy saving at the expense of some performance degradation. The energy savings, here, comes from repeated execution of tiny loops from energy efficient FC. The absence of cacheable loops leads to performance degradation in such FC structures. Therefore, we propose a simple dynamic FC scheme, which detects the opportunity for use of the FC and enables (or disables) it dynamically. Thus providing (slightly reduced) energy savings at minimal performance degradation. A combination of the predictive filter cache with the above schemes reduces the performance and energy penalty. For the benchmarks simulated with 256 byte FC, the average performance degradation is 1.13% with the proposed scheme compared to 2.47% with just the predictive filter cache. With the same configuration, the resulting energy reduction is 42.77%. Finally, the proposed dynamic filter cache scheme is inherently simple and hence it lends well for VLSI efficient implementation. [C1631]

"Frequency driven repeater insertion for deep submicron"

Repeaters now widely used to decrease delay and increase the performance of long interconnects. The maximum operating frequency is limited by the longest wire between two repeaters. The main goal of repeater insertion is to reduce the delay of the interconnects in a circuit. Increasing the number of repeaters on an interconnect increases the slew rate and the operating frequency but decreases the design performance in terms of area and power. This paper presents a new methodology of repeater insertion considering the circuit operating frequency to improve the slew rate and reduce the area overhead of the repeaters. We propose a mathematical treatment for finding the number and position of repeaters while keeping the same size of the optimal repeater size. Experimental results are shown for different frequencies and repeater sizes to indicate the improvements of slew rate and saving area overheard. [C1632]

"Event-driven dynamic power management based on wavelet forecasting theory"

The goal of dynamic power management is to reduce power dissipation in system level by putting system components into different states. This paper proposes a wavelet based approach that models the device behavior precisely. In spite of conventional stochastic models, this method eliminates some impractical assumptions which were shortcoming for previous methods. The stationary behavior of devices and the use of a memoryless distribution for device modelling are some of the aforementioned assumptions that have been relaxed in our model. Additionally, wavelet model can capture the local information accurately. Furthermore this algorithm is adaptive. This method has two additional benefits; firstly according to the device application a suitable wavelet basis can be used. Secondly, it has a sparse time-scale representation indicating that only a few coefficients in their wavelet representation have to be estimated. The simulation results show 95% accuracy in desktop hard disk drive (HDD) states prediction and power saving by a factor of 2. [C1633]

"The energy impact of aggressive loop fusion"

Loop fusion combines corresponding iterations of different loops, ft is traditionally used to decrease program run time, by reducing loop overhead and increasing data locality. In this paper, however, we consider its effect on energy. By merging program phases, fusion tends to increase the uniformity, or balance of demand for system resources. On a conventional superscalar processor, increased balance tends to increase IPC, and thus dynamic power, so that fusion-induced improvements in program energy are slightly smaller than improvements in program run time. If IPC is held constant, however, by reducing frequency and voltage-particularly on a processor with multiple clock domains-then energy improvements may significantly exceed run time improvements. We demonstrate the benefits of increased program balance under a theoretical model of processor energy consumption. We then evaluate the benefits of fusion empirically on synthetic and real-world benchmarks, using our existing loop-fusing compiler and a heavily modified version of the SimpleScalar/Wattch simulator. For the real-world benchmarks, we demonstrate energy savings ranging from 7-40%, with run times ranging from 1% slowdown to 17% speedup. In addition to validating our theoretical model, the simulation results allow us to "tease apart" the factors that contribute to fusion-induced time and energy savings. [C1634]

"Power savings in channel equalizers using run-time reconfiguration"

A channel equalizer is a major component in every communication system. Adaptive channel equalizers, which are used to compensate varying channels, are one of the most computationally intensive and power consuming components of a receiver. Power consumption is a major issue in portable communication systems and methods that provide power savings for channel equalizers are essential in mobile communications. Run-time reconfiguration (RTR) is a promising approach for reducing power consumption of many applications. We use run-time reconfiguration to reduce the power consumption of adaptive channel equalizers. Moreover, a simpler method (bypassing) is presented to take advantage of run-time reconfiguration benefits while avoiding the complexity and overhead of designing a run-time reconfigurable system. Simulation results show that the proposed run-time reconfigurable architecture reduces the power consumption by 15%. [C1635]

"Decode filter cache for energy efficient instruction cache hierarchy in super scalar architectures"

The power consumption of microprocessors has been increasing in step with the complexity of each progressive generation. In general purpose processors, this is primarily attributed to the high energy consumption of fetch and decode circuitry, pursuant to the high instruction issue rate required of these high performance processors. Predictive decode filter cache (DFC) has been shown to be effective in reducing the fetch and decode energy consumed by the instruction cache hierarchy of inorder single issue processors. We propose the architectural level enhancements to facilitate the incorporation of the DFC in wide issue superscalar processors for an energy efficient memory hierarchy. Extensive simulations on the modified superscalar architecture shows that the use of the (predictor based) DFC results in an average reduction of 17.33% and 25.09% fetch energy reduction in LI cache along with 37.2% and 46.6% reduction in number of decodes for 64 and 128 instruction DFC respectively. This fetch and decode energy savings are achieved with minimal reduction in the average instruction per cycle (IPC) of 0.54% and 0.73% for 64 and 128 instruction DFC for the selected set of spec2000 benchmarks. [C1636]

"Energy efficient code generation exploiting reduced bit-width instruction set architectures (rISA)"

Energy consumption is emerging as a critical design concern for programmable embedded systems. Many reduced bit-width instruction set architectures (rISA) (e.g., ARM Thumb) are being increasingly used to decrease code size. Previous work has explored energy savings in noncached rISA architectures as a byproduct of code size reduction. We present an energy efficient code generation technique for rISA architectures, and furthermore explore energy savings for both cached and noncached architectures. Our code generation technique uses profile information to find the most frequently executed parts of the program. By aggressively reducing code size on frequently executed parts, fewer fetches to instruction memory are incurred, thus reducing the power consumption of the instruction memory. We achieve an average 30% reduction in instruction memory energy consumption in cached systems, on a variety of benchmarks, as compared to non-rISA architectures. [C1637]

"Memory-aware energy-optimal frequency assignment for dynamic supply voltage scaling"

Dynamic supply voltage scaling (DVS) is one of the best ways to reduce the energy consumption of a device when there is a super-linear relationship between energy and supply voltage, and a pseudo-linear relationship between delay and supply voltage. However, most DVS schemes scale the clock frequency of the supply-voltage-clock-scalable (SVCS) CPU only and do not address the energy consumption of the memory. The memory is generally non-supply-voltage-scalable (NSVS), but its energy consumption is variable to its clock frequency and the total execution time. Thus, DVS for an SVCS CPU cannot achieve an optimal system-wide

energy saving without consideration of the memory, as far as it is controlled by an SVCS CPU. We introduce an energy-optimal frequency assignment, for both an SVCS CPU and a synchronous NSVS memory, which optimizes the system-wide energy consumption. We derive the energy-optimal clock frequencies for an SVCS CPU and a synchronous NSVS memory, as a function of the number of processor clock cycles, the number of memory accesses and the hardware energy model. Our technique modifies the frequency assignment of the CPU and the memory used in previous DVS schemes, which ignore the memory energy. It enables the system-wide energy-optimal settings and achieves additional 50% energy reduction over previous DVS schemes. This technique can also be applicable to synchronous NSVS peripheral devices. [C1638]

"Application specific instruction memory transformations for power efficient, fault resilient embedded processors"

In this paper we present a coding framework for a low energy instruction bus for embedded processors. The encoder exploits application-specific knowledge regarding program hot-spots to generate codewords that deliver savings in power and to furthermore provide concurrent detection of errors. Power savings can be obtained through the use of codewords that reduce the switching activity on the bus. The analysis shows that generating codewords that prohibit the occurrence of three consecutive transitions in three adjacent lines is fundamental to capturing the worst-case crosstalk faults in the bus lines at run time, thus improving the overall reliability of the bus. The desired codewords can be generated through a set of simple prespecified transformations. The detailed analysis we outline shows that the presented transformations are optimal. The proposed encoding scheme is dynamically reprogrammable, thus targeting code particularities effectively. The restriction to a simple yet efficient set of transformations reduces the required storage capacity and eases reprogrammability while achieving these objectives. Extensive experimental analysis on numerical and DSP codes indicates significant improvements in power savings. [C1639]

"CoolPression-a hybrid significance compression technique for reducing energy in caches"

This paper describes CoolPression, a hybrid hardware-based significance compression technique for reducing energy in caches. The scheme exploits data compression opportunities at bit granularity by employing two compression schemes: a significance compression scheme that counts leading ones and zeros, and a dynamic zero compression technique. Based on actual data, the more energy-efficient scheme is selected dynamically to minimize bitline drives needed for each cache access. Using SPECint2000 benchmark, our experiments show that the CoolPression improves dynamic energy consumption by more than 35% against a baseline cache, while having a saving ranged from 5 to 15% compared to each scheme applied alone. [C1640]

"Energy-efficient flash-memory storage systems with an interrupt-emulation mechanism"

One of the emerging critical issues for flash-memory storage systems, especially on the implementations of many embedded systems, is on its programmed I/O nature for data transfers. Programmed-I/O-based data transfers might not only result in the wasting of valuable CPU cycles of microprocessors but also unnecessarily consume much more energy from batteries. This work presents an interrupt-emulation mechanism for flash-memory storage systems with an energy-efficient management strategy. We propose to revise the waiting function in the memory-technology-device (MTD) layer to relieve the microprocessor from busy waiting and to reduce the energy consumption of the system. We show that energy consumption could be significantly reduced with good saving on CPU cycles and minor delay on the average response time in the experiments. [C1641]

"Power analysis of system-level on-chip communication architectures"

For complex system-on-chips (SoCs) fabricated in nanometer technologies, the system-level on-chip communication architecture is emerging as a significant source of power consumption. Managing and optimizing this important component of SoC power requires a detailed understanding of the characteristics of its power consumption. Various power estimation and low-power design techniques have been proposed for the global interconnects that form part of SoC communication architectures (e.g., low-swing buses, bus encoding, etc). While effective, they only address a limited part of communication architecture power consumption. A state-of-the-art communication architecture, viewed in its entirety, is quite complex, comprising several components, such as bus interfaces, arbiters, bridges, decoders, and multiplexers, in addition to the global bus lines. Relatively little research has focused on analyzing and comparing the power consumed by different components of the communication architecture. In this work, we present a systematic evaluation and analysis of the power consumed by a state-of-the-art communication architecture (the AMBA on-chip bus), using a commercial design flow. We focus on developing a quantitative understanding of the relative contributions of different communication architecture components to its power consumption, and the factors on which they depend. We decompose the communication architecture power into power consumed by logic components (such as arbiters, decoders, bus

bridges), global bus lines (that carry address, data, and control information), and bus interfaces. We also perform studies that analyze the impact of varying application traffic characteristics, and varying SoC complexity, on communication architecture power. Based on our analyses, we evaluate different techniques for reducing the power consumed by the on-chip communication architecture, and compare their effectiveness in achieving power savings at the system level. In addition to quantitatively reinforcing the view that on-chip communication is an important target for system-level power optimization, our work demonstrates (i) the importance of considering the communication architecture in its entirety, and (ii) the opportunities that exist for power reduction through careful comm- unication architecture design. [C1642]

"A dynamically-reconfigurable, power-efficient turbo decoder"

The development of turbo codes has allowed for near-Shannon limit information transfer in modern communication systems. Although turbo decoding is viewed as superior to alternate decoding techniques, the circuit complexity and power consumption of turbo decoder implementations can often be prohibitive for power-constrained systems. To address these issues, we have developed a reduced-complexity turbo decoder specifically optimized for contemporary FPGA devices. Our key power-saving technique is the use of decoder run-time dynamic reconfiguration in response to variations in the channel conditions. If less favorable channel conditions are detected, a more powerful, less power-efficient decoder is swapped into the FPGA hardware to maintain a fixed bit error rate. More favorable channel conditions result in the opposite effect. Through experimentation on a stratix-based NIOS development board, we show that dynamic reconfiguration can result in a 52% power reduction versus a static decoder implementation. Comparisons with contemporary microprocessors illustrate a 100Ч performance improvement. [C1643]

"Adaptive sampling for wireless sensor networks"

This paper proposes an adaptive three-stage approach for accurate field estimation using a wireless sensor network that can significantly reduce energy consumption. Under a piecewise smooth field assumption, this method nearly achieves the minimax error rate n-12/, where n is the number of available sensors, while activating only n34/ of the sensors in the network. This approach can save significant energy compared to dense, nonadaptive sampling. [C1644]

"Random asynchronous wakeup protocol for sensor networks"

This paper presents a random asynchronous wakeup (RAW), a power saving technique for sensor networks that reduces energy consumption without significantly affecting the latency or connectivity of the network. RAW builds on the observation that when a region of a shared-channel wireless network has a sufficient density of nodes, only a small number of them need be active at any time to forward the traffic for active connections. RAW is a distributed, randomized algorithm where nodes make local decisions on whether to sleep, or to be active. Each node is awake for a randomly chosen fixed interval per time frame. High node density results in existence of several paths between two given nodes whose path length and delay characteristics are similar to the shortest path. Thus, a packet can be forwarded to any of several nodes in order to be delivered to the destination without affecting much the path length and delay experienced by the packet as compared to forwarding the packet through the shortest path. The improvement in system lifetime, due to RAW, increases as the ratio of idle-to-sleep energy consumption increases, and as the density of the network increases. Through analytical and experimental evaluations, we show that RAW improves communication latency and system lifetime compared to current schemes. [C1645]

"Improving energy savings in power adaptive broadcasting in MANETs"

Network wide broadcast is a frequently used operation in mobile ad hoc networks (MANETs). Many unicast protocols including dynamic source routing (DSR) and ad hoc on-demand distance vector (AODV) protocol use broadcast to discover the unicast routes toward destinations. In addition, depending on the application, broadcast can be used to deliver actual data packets to all the nodes in the network. Nodes in MANETs work with limited battery power and the efficient utilization of this power is important for increasing the lifetime of the individual nodes as well as the overall network. As a result, it is important to utilize energy efficient algorithms in achieving network wide broadcast in MANETs. In this poster paper, the authors improve the energy efficiency in power adaptive broadcast using local information. In this proposal, the authors introduce an improved algorithm for deciding the transmission power level. The paper also attempts to further increase the energy savings by reducing the redundant transmission by including an efficient forward node set at the selection algorithm. [C1646]

"Exploiting the behavior of ready instructions for power benefits in a dynamically scheduled embedded processor"

Many instructions in a dynamically scheduled superscalar processor spend a significant time in the instruction window (IW) waiting to be selected even though their dependencies are satisfied. These "delays" are due to resource constraints and the oldest first selection policy used in many processors that gives a higher priority to older ready instructions than younger ones. In this paper, we study the "delay" and criticality characteristics of instructions based on their readiness during dispatch. We observe that most ready-on-dispatch (ROD) instructions are non critical and show that 57% of these instructions spend more than 1 cycle in the IW. We analyze the impact of: (i) steering ROD instructions to slow low power functional units; and (ii) early issue of ROD instructions, on power and performance. We find that the "early issue and slow execution" of ROD instructions reduces power consumption by 4-12% while degrading performance by about 5%. On the other hand, "early issue normal execution" of ROD instructions results in 3.5% power savings with less than 1% performance loss. Further, we find that the above policies reduce the energy expended in executing wrong path instructions by about 2%. [C1647]

"New power saving design method for CMOS flash ADC"

A new power saving design method for CMOS flash ADC is presented. With an inverter as a comparator along with an NMOS and a PMOS as switches, we use bisection method to let only half of comparators in flash ADC working in every clock cycle. An example of 6-bit flash ADC operates at 200 MHz sampling rate and 3.3 V supply voltage is demonstrated. The power consumption of proposed circuit is only 40.75 mW with HSPICE simulation. Compared with the traditional flash ADC, our bisection method can reduce up to 43.18% in power consumption. [C1648]

"Low power dual transmission gate adiabatic logic circuits and design of SRAM"

A dual transmission gate adiabatic logic (DTGAL) suitable for driving large capacitance is presented. DTGAL, has no non-adiabatic energy loss on output loads by using feedback control from next-stage buffer outputs. The minimization of energy consumption was investigated by choosing the optimal size of DTGAL circuits. A 64Ч64-b adiabatic SRAM is designed. The proposed DTGAL circuits are used to recover the charge of large switching capacitance on bit-lines, word-lines, and address decoders in fully adiabatic manner. The power consumption of the proposed SRAM is significantly reduced as the energy transferred to large capacitance buses is mostly recovered. Energy and functional simulations were performed using the net-list extracted from the layout. HSPICE simulation results indicate that the proposed SRAM attains energy savings of 65% to 90% as compared with the conventional CMOS implementation for clock rates ranging from 25 to 200 MHz. [C1649]

"Array hybrid multiplier versus modified booth multiplier: comparing area and power consumption of layout implementations of signed radix-4 architectures"

In this paper, we describe the fully automated custom layout implementations of two architectures for signed multiplication. Performance comparisons between the two, namely in terms of their power consumption and area estimation are provided for 8 and 16-bit operands. The first architecture consists of a signed array multiplier that uses a radix-4 hybrid encoding to reduce the partial product lines and switching activity in the data buses. This new arithmetic operand encoding was recently proposed in (Costa et al., 2004), however only results at the logic level were presented. The second architecture implemented was the widely used modified Booth multiplier (Khater et al., 1996). The layout of both multipliers was generated by an automatic layout synthesis tool called TROPIC (MOraes, 1999). We compare the layout implementations in terms of area and power, as well as provide comparisons to first-order area estimates done in the logic design phase. The results show that the new hybrid array multiplier can be significantly more efficient, with close to 30% power savings. [C1650]

"A power-aware and QoS-aware service model on wireless networks"

Many studies show that the wireless network interface (WNI) accounts for a significant part of the power consumed by mobile terminals. Thus, putting the WNI into sleep when it is idle is an effective technique to save power. To support streaming applications, existing techniques cannot put the WNI into sleep due to strict delay requirements. We present a novel power-aware and QoS-aware service model over wireless networks. In the proposed model, mobile terminals use proxies to buffer data so that the WNIs can sleep for a long time period. To achieve power-aware communication while satisfying the delay requirement of each flow, a scheduling scheme, called priority-based bulk scheduling (PBS), is designed to decide which flow should be served at which time. Through analysis, we prove that the PBS service model can provide delay assurance and achieve power efficiency. We use audio-on-demand and Web access as case studies to evaluate the performance of the PBS service model. Experimental results show that PBS achieves excellent QoS provision for each flow and significantly reduces the power consumption. [C1651]

"On the correlated data gathering problem in wireless sensor networks"

A fundamental challenge in the design of wireless sensor networks (WSNs) is to maximize their lifetimes. Since many sensors have correlated readings, data aggregation has emerged as an efficient approach to reduce the number of transmissions, and hence minimize overall power consumption in the network. An important aspect of data aggregation is the placement of aggregation points and how aggregated data is routed to the gathering points. In this paper, we consider the problem of correlated data gathering in WSNs with the objective of minimizing the total transmission cost in terms of power consumption. We particularly focus on the problem of finding the set of aggregation points that satisfy our objective. Two solution strategies are presented: an exact solution using an integer linear program (ILP) formulation and a near optimal, but simple and efficient heuristic, called load balancing with aggregation (LISA). Our solutions use a fixed virtual wireless backbone that is built on top of the physical topology. Numerical results show that our proposed scheme provides substantial energy savings when compared to other schemes. [C1652]

"Modeling the performance of wireless sensor networks"

A critical issue in wireless sensor networks is represented by the limited availability of energy within network nodes; therefore making good use of energy is a must. A widely employed energy-saving technique is to place nodes in sleep mode, corresponding to a low-power consumption as well as to reduced operational capabilities. In this work, we develop a Markov model of a sensor network whose nodes may enter a sleep mode, and we use this model to investigate the system performance in terms of energy consumption, network capacity, and data deliver delay. Furthermore, the proposed model enables us to investigate the trade-offs existing between these performance metrics and the sensor dynamics in sleep/active mode. Analytical results present an excellent matching with simulation results for a large variety of system scenarios showing the accuracy of our approach. [C1653]

"Energy storage on board of DC fed railway vehicles PESC 2004 conference in Aachen, Germany"

The proposed energy storage on board of a DC-railway vehicle leads to a big step in the reduction of consumed energy. Up to 30% energy saving are expected in a light rail vehicle, at the same time reducing the peak power demand drastically. In addition, with the energy storage an operation without catenary could become reality, which was successfully demonstrated with the prototype light rail vehicle driving with switched off pantograph. This prototype vehicle is in passenger operation since September 2003, the implemented software is optimised on energy savings and first experience is very promising. [C1654]

"Architecture-aware low-density parity-check codes"

A high-throughput memory-efficient decoder architecture for architecture-aware low-density parity-check (LDPC) codes is proposed based on a novel turbo-decoding algorithm. The architecture benefits from various optimizations at the code-design, decoding algorithm, and decoder architecture levels. The interconnect complexity and memory overhead problems of current decoder implementations are reduced by designing structured or architecture-aware LDPC codes and employing a new turbo-decoding algorithm. An efficient memory architecture coupled with a scalable and dynamic transport network for storing and routing messages are proposed. Simulations demonstrate that the proposed architecture attains a throughput of 1.92 Gbits/s for a frame length of 2304 bits, and achieves savings of 89.13 % and 62.80 % in power consumption and silicon area over state-of-the-art, with a reduction of 60.5 % in interconnect wires. [C1655]

"Minimum selection GSC and adaptive low-power rake combining scheme"

In this paper, we investigate a new generalized selection combining (GSC) technique and an adaptive low-power rake combining scheme to save the power consumption of mobile rake receivers for wideband CDMA systems. The new GSC technique called minimum selection GSC (MS-GSC) selects a minimum number of rake fingers as long as the combined SNR is larger than a given threshold. The proposed rake combining scheme adaptively adjusts the threshold value to maintain the desired BER, in which a GSC dynamically selects rake fingers to meet the given threshold condition. The proposed MS-GSC shows a low standard deviation in bit error statistics and advantages practical implementation. The proposed adaptive scheme works well with existing GSC schemes as well as the proposed MS-GSC. The proposed scheme reduced the power consumption of a mobile rake receiver up to 67.8% by turning off unselected rake fingers. [C1656]

"A multi-phase charge-sharing technique without external capacitor for low-power TFT-LCD column drivers"

With up to 75% power saving efficiency, theoretically, with infinite phases, a novel multi-phase charge-recycling

technique that does not require any external capacitor for charge conservation is proposed for the dot inversion method, to reduce AC power consumption of a TFT-LCD column driver. It is easy to implement with simple circuitry. Compared with the original circuit (without any low-power scheme) and previous low-power charge-recycling work, the proposed method, with each group of 8 data lines, decreases the power consumption about 23%-68% and 10%-18%, respectively. [C1657]

"A 3.3 V 1 GHz low-latency pipelined Booth multiplier with new Manchester carry-pass adder"

In this paper, a high speed, low latency pipelined Booth multiplier with new Manchester carry-bypass adder (MCBA) is proposed. By using new partial product generation scheme and new MCBA, the latency is reduced to 6. By using new MCBA, the speed bottleneck is overcome with 40.16% improvement and the energy can be saved with 30.59% improvement. The 13-bit new MCBA pipelined into 2 stages can operate above 1 GHz with worst-case delay of 0.833 ns and consumed only 16.81 mW. Finally, the proposed pipelined Booth multiplier is presented at 3.3 V, 1 GHz in TSMC 0.35 μm process with a power consumption of only 60.18 mW. [C1658]

"Wireless LANs: an adaptive algorithm to reduce power consumption"

A novel radio modem architecture is proposed for a single-hop ad hoc networks (WLAN) providing wireless access to Internet. The system works at 17 GHz, employs OFDM modulation and provides very high bit rate (up to 160 Mbit/s at physical layer) using TDMA access scheme. Network control is centralized and handled by a device (master), which is run-time selected among all the active devices (slaves). The main focus of the paper is to address the power consumption issue, which is a crucial requirement for portable devices. In particular, the paper described the developed MAC procedures and algorithms concerning the interface with physical layer. Simulation trials show that a considerable power saving can be attained without decreasing system performance. [C1659]

"Paging-aided connection setup for real-time communication in mobile Internet"

Mobile IP is a solution mobility on the global Internet. However, the basic mobile IP does not support paging. The main benefit of providing paging services is to save the battery power consumption at mobile terminals. Next generation Internet is expected to support multimedia communications. For real-time data traffic, quality of service (QoS) provision must be guaranteed. The resource reservation protocol (RSVP) was proposed to support the signaling of end-to-end IP QoS. When both IP paging and RSVP are supported in the network, the signaling delay for connection setup is the sum of the paging delay and the time for RSVP path setup. This paper introduces a new scheme for fast connection setup with the help of mobile IP location registration and paging. Performance analysis shows that the proposed scheme reduces the overall signaling delay and the total number of signaling messages. [C1660]

"Reduce the complexity of frequency-response masking filter using multiplication free filter"

A modified frequency-response masking (FRM) approach is presented for the design of arbitrary bandwidth sharp FIR filters. The new filter achieves significant savings in the number of arithmetic operations by replacing the band-edge shaping filter in the FRM technique with a modified interpolated finite impulse response (IFIR) filter. Our example shows that the proposed one-stage FRM filter outperforms an original two-stage FRM filter in terms of the number of multipliers and group delay. [C1661]

"A power-efficient architecture for high-speed D/A converters"

A novel power-efficient architecture for high-speed D/A converters is proposed. A data look ahead technique is used to pre-switch the current sources so that the DAC current is reduced when generating small voltage levels. Interestingly, this technique also eliminates the need for a pre-driver block for each current-cell, which also saves power. Based on this architecture, a 6-bit DAC is designed in 0.18μm standard digital CMOS technology. The update rate for this DAC is 1GS/s and it consumes only 24mW at 1GS/s. [C1662]

"Reducing dynamic power consumption in next generation DS-CDMA mobile communication receivers"

Reduction of the power consumption in portable wireless receivers is an important consideration for next-generation cellular systems specified by standards such as the UMTS, IMT2000. We explore the architectural design-space and methodologies for reducing the dynamic power dissipation in the direct sequence code division multiple access (DS-CDMA) downlink RAKE receiver. Starting with a reference implementation of the DS-CDMA RAKE receiver, we demonstrate design methodologies for achieving significant power reduction, while highlighting the corresponding performance trade-offs. At the algorithm level, we investigate the tradeoffs of

reduced precision and arithmetic complexity on the receiver performance. We then present two architectures for implementing the reference and reduced complexity receivers, and analyze these architectures with respect to their dynamic power dissipation. Our findings report that reduction in precision from a 16 bit to a 10 bit data-path is found to yield significant power savings of 25.6% in the reference RAKE receiver architecture, with a performance loss of less than 1 dB. Further, a power reduction of up to 24.65% is achieved in a 16 bit data-path for the reduced complexity RAKE receiver compared to the reference architecture, with a performance loss of less than 2 dB. Although there is a tradeoff in performance, adaptive power saving is very important for mobile wireless terminals. The combined effect of reduced precision and complexity reduction leads to a 37.44% savings in baseband processing power. [C1663]

"A distributed and adaptive signal processing approach to reducing energy consumption in sensor networks"

We propose a novel approach to reducing energy consumption in sensor networks using a distributed adaptive signal processing framework and efficient algorithm. While the topic of energy-aware routing to alleviate energy consumption in sensor networks has received attention recently (C. Toh, 2001; R. Shah et al., 2002), in this paper, we propose an orthogonal approach to previous methods. Specifically, we propose a distributed way of continuously exploiting existing correlations in sensor data based on adaptive signal processing and distributed source coding principles. Our approach enables sensor nodes to blindly compress their readings with respect to one another without the need for explicit and energy-expensive intersensor communication to effect this compression. Furthermore, the distributed algorithm used by each sensor node is extremely low in complexity and easy to implement (i.e., one modulo operation), while an adaptive filtering framework is used at the data gathering unit to continuously learn the relevant correlation structures in the sensor data. Our simulations show the power of our proposed algorithms, revealing their potential to effect significant energy savings (from 10%-65%) for typical sensor data corresponding to a multitude of sensor modalities. [C1664]

"An energy reduction technique for multimedia application with tolerance to deadline misses"

Many embedded systems such as PDAs require processing of the given applications with rigid power budget. However, they are able to tolerate occasional failures due to the imperfect human visual/auditory systems. The problem we address in this paper is how to utilize such tolerance to reduce multimedia system's energy consumption for providing guaranteed quality of service at the user level in terms of completion ratio. We explore a range of offline and on-line strategies that take this tolerance into account in conjunction with the modest non-determinism in application's execution time. First, we give a simple best-effort approach that achieves the maximum completion ratio; then we propose an enhanced on-line best-effort energy minimization (BEEM) approach and a hybrid offline/on-line minimum effort (O2ME) approach. We prove that BEEM maintains the maximum completion ratio while consuming the probably least amount of energy and O2ME guarantees the required completion ratio statistically. We apply both approaches to a variety of benchmark task graphs, most from popular DSP applications. Simulation results show that significant energy savings (38% for BEEM and 54% for O2ME, both over the simple best-effort approach) can be achieved while meeting the required completion ratio requirements. [C1665]

"An efficient power saving mechanism for wireless LAN"

In this paper, a novel radio modem architecture for a wireless local area network is proposed. The main focus is to reduce the power consumption, which is a crucial requirement for portable devices. In particular, the paper describes a new control architecture which is in charge of properly adapting the transmission power to the link's condition by controlling the transmission bit rate and the capacity request scheme. By using fuzzy logic and internal model control, the scheme manages to adapt the bit rate, granting at the same time the reduction of the power consumption and the satisfaction of the quality of service requirements. [C1666]

"A highly configurable cache architecture for embedded systems"

Energy consumption is a major concern in many embedded computing systems. Several studies have shown that cache memories account for about 50% of the total energy consumed in these systems. The performance of a given cache architecture is largely determined by the behavior of the application using that cache. Desktop systems have to accommodate a very wide range of applications and therefore the manufacturer usually sets the cache architecture as a compromise given current applications, technology and cost. Unlike desktop systems, embedded systems are designed to run a small range of well-defined applications. In this context, a cache architecture that is tuned for that narrow range of applications can have both increased performance as well as lower energy consumption. We introduce a novel cache architecture intended for embedded microprocessor platforms. The cache can be configured by software to be direct-mapped, two-way, or four-way set associative,

using a technique we call way concatenation, having very little size or performance overhead. We show that the proposed cache architecture reduces energy caused by dynamic power compared to a way-shutdown cache. Furthermore, we extend the cache architecture to also support a way shutdown method designed to reduce the energy from static power that is increasing in importance in newer CMOS technologies. Our study of 23 programs drawn from Powerstone, MediaBench and Spec2000 show that tuning the cache's configuration saves energy for every program compared to conventional four-way set-associative as well as direct mapped caches, with average savings of 40% compared to a four-way conventional cache. [C1667]

"Profile-based dynamic voltage and frequency scaling for a multiple clock domain microprocessor"

A Multiple Clock Domain (MCD) processor addresses the challenges of clock distribution and power dissipation by dividing a chip into several (coarse-grained) clock domains, allowing frequency and voltage to be reduced in domains that are not currently on the application's critical path. Given a reconfiguration mechanism capable of choosing appropriate times and values for voltage/frequency scaling, an MCD processor has the potential to achieve significant energy savings with low performance degradation. Early work on MCD processors evaluated the potential for energy savings by manually inserting reconfiguration instructions into applications, or by employing an oracle driven by offline analysis of (identical) prior program runs. Subsequent work developed a hardware-based online mechanism that averages 75-85% of the energy-delay improvement achieved via offline analysis. We consider the automatic insertion of reconfiguration instructions into applications, using profile-driven binary rewriting. Profile-based reconfiguration introduces the need for "training runs" prior to production use of a given application, but avoids the hardware complexity of online reconfiguration. It also has the potential to yield significantly greater energy savings. Experimental results (training on small data sets and then running on larger, alternative data sets) indicate that the profile-driven approach is more stable than hardware-based reconfiguration, and yields virtually all of the energy-delay improvement achieved via offline analysis. [C1668]

"Energy analysis of end-of-life options for personal computers: resell, upgrade, recycle"

Governments, firms, and civil society are increasingly taking action to manage the end-of-life of computers. While appropriate treatment of the waste stream via recycling and other technologies is required, it is also important to address the flow upstream through reduction of final demand via improved utilization. This article evaluates end-of-life options for computers via quantitative assessment of life cycle energy use in three cases: reselling to secondary markets, upgrading of key components, and recycling to recover materials. Results indicate that reselling or upgrading 10% of end-of-life computers reduces life cycle energy use by 8.6% and 5.2% respectively. In contrast, recycling 10% of computers only saves 43% of life cycle energy, suggesting that reselling and upgrading are far more effective from an environmental standpoint. The origin of this dramatic difference between reuse and recycling lies in the fact that much of the energy investment in the life cycle of a computer is in producing its complex form rather than its physical substance. Thus, the environmental payback of recycling materials is poor compared to many goods. This strongly suggests that management strategies for waste electronics should emphasize extension of lifespan. [C1669]

"Assessing the potential of telecommuting as an energy savings technology in Japan"

A simple macro-model is developed to assess the potential of telework as an energy saving technology for Japan. Results are that adoption of 4-day per week telecommuting of the mobile sales and specialist/technical work force could reduce national energy consumption by 1.0%. If clerical workers also telecommute an additional 1.1% of savings become possible. While these results have a fair margin of uncertainty, they do indicate that telecommuting should be considered as a serious candidate for reduction of energy-related environmental burdens. The adoption of telecommuting, especially for clerical workers, is hampered by the limitation on modes of communication available via current networking technologies. In particular, inexpensive, high quality video-calling on demand would be key in making telecommuting practicable and enjoyable on a large scale. However, current trends in the progress in Internet bandwidth are not promising. While last mile bandwidth (from provider to home) is nearing the critical level needed for video-calls, the scale and fluctuations in first miles bandwidth (from server to provider) is the real bottleneck. Future efforts to upgrade the Internet should focus on this factor, or alternatively, developing a broadband switched network. While transport savings is the dominant factor in the energy balance of telecommuting, changes in energy use in buildings, both commercial and residential, is significant and deserves attention. In particular, firm-level management of telecommuting programs should strive to insure that consumption in office buildings falls sufficiently to at least balance out increases in residential consumption. [C1670]

"Design of asynchronous function unit and software development tools for a low-power DSP"

The requirement for extended battery life, reduced size and low electromagnetic interference (EMI) for mobile

communication equipment has led to the development of a novel low-power asynchronous digital signal processor (DSP) device known as CADRE (configurable asynchronous DSP for reduced energy). The architecture of CADRE is based on an asynchronous 'function unit' (FU) which has been designed to reduce power consumption as far as possible without sacrificing speed. This paper describes current work in redesigning the FU hardware to achieve improvements in power efficiency with the use of pass-transistor logic, voltage scaling and modifications to the hardware multiplication and addition circuitry. Software support for the new DSP is needed to avoid manual assembly-level programming and a 'C' compiler is being developed to make the best use of the power saving features of CADRE when implementing speech coding algorithms as required by 3G mobile telephony. A cost database and 'pattern' program for guiding the energy aware compilation is used and three optimisation strategies are described. Results are presented which demonstrate the effectiveness of the optimisations. [C1671]

"Control techniques to eliminate voltage emergencies in high performance processors"

Increasing focus on power dissipation issues in current microprocessors has led to a host of proposals for clock gating and other power-saving techniques. While generally effective at reducing average power, many of these techniques have the undesired side-effect of increasing both the variability of power dissipation and the variability of current drawn by the processor This increase in current variability, often referred to as the dI/dt problem, can cause supply voltage fluctuations. Such voltage fluctuations lead to unreliable circuits if not addressed, and increasingly expensive chip packaging techniques are needed to mitigate them. This paper proposes and evaluates a methodology for augmenting packaging techniques for dI/dt with microarchitectural control mechanisms. We discuss the resonant frequencies most relevant to current microprocessor packages, produce and evaluate a "dI/dt stressmark" that exercises the system at its resonant frequency, and characterize the behavior of more mainstream applications. Based on these results plus evaluations of the impact of controller error and delay, our microarchitectural control proposals offer bounds on supply voltage fluctuations, with nearly negligible impact on performance and energy. With the ITRS roadmap predicting aggressive drops in supply voltage and power supply impedances in coming chip generations, novel voltage control techniques will be required to stay on track. Our microarchitectural dI/dt controllers represent a step in this direction. [C1672]

"Combining software and hardware monitoring for improved power and performance tuning"

By anticipating when resources will be idle, it is possible to reconfigure the hardware to reduce power consumption without significantly reducing performance. This requires predicting what the resource requirements will be for an application. In the past, researchers have taken one of two approaches: design hardware monitors that can measure recent performance, or profile the application to determine the most likely behavior for each block of code. This paper explores a third option which is to combine hardware monitoring with software profiling to achieve lower power utilization than either method alone. We demonstrate the potential for this approach in two ways. First, we compare hardware monitoring and software profiling of IPC for code blocks and show that they capture different information. By combining them, we can control issue width and ALU usage more effectively to save more power. Second, we show that anticipating stalls due to critical load misses in the L2 cache can enable fetch halting. Again, hardware monitoring and software profiling must be used together to effectively predict misses and criticality of loads. [C1673]

"Reconfigurable ADC for 3-G UTRA-TDD mobile receiver"

A novel reconfigurable architecture has been proposed for a mobile terminal receiver that can reduce power dissipation dependant on adjacent channel interference. Quantisation error analysis was carried out in order to find the minimum number of bits required. The proposed design can automatically scale the number of bits by monitoring the in-band and out-of-band powers. The new architecture performance was evaluated in a simulation UTRA-TDD environment because of the large near far problem caused by adjacent channel interference from adjacent mobiles and base stations. The UTRA-TDD downlink mode was examined statistically and results show that the reconfigurable architecture can save an average of up to 75% power dissipation when compared to a fixed word length of 16 bits. This will prolong talk and standby time in a mobile terminal. The average number of bits were calculated to be 10, for an outage of 97%. [C1674]

"Energy efficient scheduling for datapath synthesis"

In this paper, we describe two new algorithms for datapath scheduling which aim at energy reduction while maintaining performance. The proposed algorithms, time constrained and resource constrained, utilize the concepts of multiple supply voltage and dynamic clocking for energy minimization. In dynamic clocking, the functional units can be operated at different frequencies depending on the computations occurring within the datapath during a given clock cycle. The strategy is to schedule high energy units, such as the multipliers at

lower frequencies such that they can be operated at lower voltages to reduce energy consumption and the low energy units, such as adders at higher frequencies, to compensate for speed. The algorithms have been applied to various high level synthesis benchmark circuits under different time and resource constraints. The experimental results show that for the time constrained algorithm, energy savings in the range of 33-75% are obtained. Similarly, for the resource constrained algorithm, under various resource constraints using two supply voltage levels (5.0 V, 3.3 V), energy savings in the range of 24-53% can be obtained. [C1675]

"ASP: an adaptive energy-efficient polling algorithm for Bluetooth piconets"

Among the various wireless technologies available today, Bluetooth stands out as the most promising for use in low-power sensor networks. This is especially true for large networks of sensors with low data rates, where Bluetooth's low power Hold, Sniff, and Park modes could be utilized during periods of low activity to reduce power consumption. One way that these modes can be exploited to reduce energy consumption is by using an intelligent polling scheme to control intra-piconet traffic. We introduce a polling algorithm called adaptive share polling (ASP) that is designed to perform well when the network consists of sources sending short data packets at constant rate that may fluctuate over time. In ASP, the scheduler at the master implicitly learns the share of the bandwidth that needs to be allocated to each of the slaves in order to meet the latency and/or power requirements of the application. Our simulation results show that significant power savings can be achieved in slaves whose data rates do not approach capacity of a Bluetooth piconet, and in masters when the composite data rate of the piconet does not approach capacity. [C1676]

"Energy recovering ASIC design"

Dissipation in the clock tree and state elements of ASIC designs is often a significant fraction of total energy consumption. We propose a methodology for recovering most of this energy by using a novel energy recovering flip-flop and a novel single-phase resonant clock generator. As our state element has near-zero energy consumption when the input data is not switching, it provides the savings of clock gating approaches without the additional complexity of implementing clock gating in the design. To complement this near-zero idle energy property of the flip-flop, our resonant clock generator includes the capability to decide, on a per-cycle basis, whether or not the resonant clock needs to be replenished on the next cycle, thus automatically reducing energy consumption when most of the state elements are idling. ASICs designed with our methodology can achieve sub-C·Vdd2dissipations on the clock network at frequencies of 200-500MHz and operating voltages of 1.0-1.5V in a 0.25 µm process. To evaluate our methodology, we simulated a dual-mode (conventional and energy recovering) ASIC module to directly compare energy savings between the energy recovering and conventional clocking schemes. Our simulations demonstrate savings of over a factor of 4 for the energy-recovering mode versus the conventional mode for low switching activities. [C1677]

"Low-energy BIST design for scan-based logic circuits"

In a random testing environment, a significant amount of energy is wasted in the LFSR and in the CUT by useless patterns that do not contribute to fault dropping. Another major source of energy drainage is the loss due to random switching activity in the CUT and in the scan path between applications of two successive vectors. In this work, a new built-in self-test (GIST) scheme for scan-based circuits is proposed for reducing such energy consumption. A mapping logic is designed which modifies the state transitions of the LFSR such that only the useful vectors are generated according to a desired sequence. Further, it reduces test application time without affecting fault coverage. Experimental results on ISCAS-89 benchmark circuits reveal a significant amount of energy savings in the LFSR during random testing. [C1678]

"On localized prediction for power efficient object tracking in sensor networks"

Energy is one of the most critical constraints for sensor network applications. In this paper, we exploit the localized prediction paradigm for power-efficient object tracking sensor network. Localized prediction consists of a localized network architecture and a prediction mechanism called dual prediction, which achieve power savings by allowing most of the sensor nodes stay in sleep mode and by reducing the amount of long-range transmissions. Performance evaluation, based on mathematical analysis, shows that localized prediction can significantly reduce the power consumption in object tracking sensor networks. [C1679]

"Impact of data compression on energy consumption of wireless-networked handheld devices"

We investigate the use of data compression to reduce the battery consumed by handheld devices when downloading data from proxy servers over a wireless LAN. To make a careful trade-off between the communication energy and the overhead to perform decompression, we experiment with three universal lossless compression schemes, using a popular handheld device in a wireless LAN environment and we find interesting

facts. The results show that, from the battery-saving perspective, the gzip compression software (based on LZ77) to be far superior to bzip2 (based on BWT) and compress (based on LZW). We then present an energy model to estimate the energy consumption for the compressed downloading. With this model, we further reduce the energy cost of gzip by interleaving communication with computation and by using a block-by-block selective scheme based on the compression factor of each block. We also use a threshold file size below which the file is not to be compressed before transferring. [C1680]

"Energy optimal scheduling under average throughput constraint"

By adapting radio setting, such as the modulation or error code, in response to changes in the wireless channel, the energy consumption of a communication system can be greatly reduced. In paper, we investigate the problem of minimizing the energy for a desired average throughput. When the option of shutting down the radio completely is also considered, deciding on the optimal setting becomes a complex scheduling problem. In this case, we have to take power of both the radio electronics and the power amplifier into account, the relative importance of which has a critical impact on the nature of the adaptation strategy, as we show in this paper. We present a new algorithm that does not require any knowledge of the channel statistics, but instead quickly learns the desired adaptation strategy. It is easy to implement, yet is optimal in terms of energy savings. [C1681]

"Adaptive power control and selective radio activation for low-power infrastructure-mode 802.11 LANs"

We present an integrated dual approach to reduce power consumption in infrastructure-mode 802.11 wireless LANs. A novel distributed power control algorithm adoptively adjusts the transmit power of the 802.11 radio/NIC to achieve power savings in the presence of mobility and RF noise. An adaptive radio activation algorithm selectively sleeps the 802.11 radio/NIC, to reduce idle power consumption. We analyze the performance of these algorithms in an 802.11 testbed using Web traces of HTTP/TCP user data accesses. Our application-level architecture integrates the two approaches into an incrementally deployable and application-transparent solution for power management of the RF interface on 802.11-enabled laptops. [C1682]

"BEAM: bus encoding based on instruction-set-aware memories"

This paper introduces a new approach for minimizing power dissipation on the memory address bus. The proposed approach relies on the availability of smart memories that have certain awareness of the instruction format of one or more architectures. Based on this knowledge, the memory calculates or predicts the instruction and data addresses. Hence, not all addresses are sent from the processor to the memory. This, in turn, significantly reduces the activity on the memory bus. The proposed method can eliminate up to 97% of the transitions on the instruction address bus and 75% of the transitions on the data address bus with a small hardware overhead. The actual power savings of 85% for the instruction bus and 64% for the data bus were achieved for a per-line bus capacitance of 10 pF. [C1683]

"Energy-aware target localization in wireless sensor networks"

Wireless distributed sensor networks (DSNs) are important for a number of strategic applications such as coordinated target detection, surveillance, and localization. Energy is a critical resource in wireless sensor networks and system lifetime needs to be prolonged through the use of energy-conscious sensing strategies during system operation. We propose an energy-aware target detection and localization strategy for cluster-based wireless sensor networks based on an a posteriori algorithm with a two-step communication protocol between the cluster head and the sensors within the cluster With a very limited amount of data from the sensor nodes, the cluster head executes a localization procedure to determine the subset of sensors that must be queried for detailed target information. This approach reduces both energy consumption and communication bandwidth requirements, and prolongs the lifetime of the wireless sensor network. Simulation results show that a large amount of energy is saved during target localization using this strategy. [C1684]

"Target localization based on energy considerations in distributed sensor networks"

Wireless distributed sensor networks (DSNs) are important for a number of strategic applications such as coordinated target detection, surveillance, and localization. Energy is a critical resource in wireless sensor networks and system lifetime needs to be prolonged through the use of energy-conscious sensing strategies during system operation. We propose an energy-aware target detection and localization strategy for cluster-based wireless sensor networks. The proposed method is based on an a posteriori algorithm with a two-step communication protocol between the cluster head and the sensors within the cluster. Based on a limited amount of data received from the sensor nodes, the cluster head executes a localization procedure to determine the subset of sensors that must be queried for detailed target information. This approach reduces both energy

consumption and communication bandwidth requirements, and prolongs the lifetime of the wireless sensor network. Simulation results show that a large amount of energy is saved during target localization using this strategy. [C1685]

"Energy minimization of real-time tasks on variable voltage processors with transition energy overhead"

In this paper, we address the problem of minimizing energy consumption of real-time tasks on variable voltage processors whose transition energy overhead is not negligible. Voltage settings with minimum number of transitions are found first and sequences of lower voltage cycles are evaluated to decide voltage for each cycle of every task. Experimental results demonstrate that our approach can reduce energy consumed by transitions from 41% to 8% and save more energy. [C1686]

"Combined dynamic voltage scaling and adaptive body biasing for heterogeneous distributed real-time embedded systems"

Dynamic voltage scaling (DVS) is a powerful technique for reducing dynamic power consumption in a computing system. However, as technology feature size continues to scale, leakage power is increasing and will limit power savings obtained by DVS alone. Previous system-level real-time scheduling approaches use DVS alone to optimize power consumption without considering leakage power. To overcome this limitation, we propose a new scheduling algorithm that combines DVS and adaptive body biasing (ABB) to simultaneously optimize both dynamic power consumption and leakage power consumption for real-time distributed embedded systems. First, we derive an analytical expression to determine the optimal supply voltage and body bias voltage under a given clock frequency. Based on this expression, we compute the optimal energy consumption at a given clock frequency and analyze the tradeoff between energy consumption and execution time for a set of tasks with precedence relationships and real-time constraints. We then propose a scheduling algorithm to reduce total power consumption under given real-time constraints. This algorithm also considers variations in power consumption of different tasks and characteristics of different voltage-scalable processing elements (PEs) to maximize power reduction. Experimental results show that the average power reduction of our technique with respect to DVS alone is 34.7%, while the average saving compared to no voltage scaling is 68.3% for the 0.07 µm technology. [C1687]

"A game theoretic approach to dynamic energy minimization in wireless transceivers"

Adaptive transceivers can significantly reduce the energy consumption of a mobile, battery-powered node by capturing real-time changes in the communication channel. This paper proposes a game-theoretic solution to the optimization of the energy consumption in wireless transceivers. This is accomplished by dynamically adapting the modulation level of the transmitter modulator and the error correction aptitude of the receiver decoder with respect to channel conditions subject to specified average bit-error-rate and throughput constraints. Experimental results demonstrate energy savings of up to 15%. [C1688]

"A gate leakage reduction strategy for future CMOS circuits"

We show that a technique previously introduced for sub-threshold leakage reduction can be effectively used to reduce gate leakage dissipation in future CMOS circuits operating in stand-by mode. The technique gave one order of magnitude gate leakage savings with a certain input pattern for the evaluated two-input NAND gate. Also, we make a detailed analysis of mechanisms causing different direct oxide tunnelling currents that contributes to gate leakage power dissipation in future CMOS circuits. [C1689]

"A low power and high speed Viterbi decoder chip for WLAN applications"

This paper presents a 166Mb/s, 64-state, radix-4, 16-level soft decision Viterbi decoder for high speed WLAN applications. With the path merging and trace forward techniques, the memory read operations are reduced to save power consumption. A test chip is fabricated in 0.35µm IP4M CMOS process, and can achieve the maximum throughput rate of 166Mbit/s under 3.3V. The measured power consumption is below 55mW under 166Mb/s throughput rate at 2.2V. [C1690]

"TRANSFER: transactions routing for ad-hoc networks with efficient energy"

In future ad hoc networks, transactions are expected to become one of the primary types of flows. Transactions require only a very small number of packets to complete. Hence, providing optimal (or shortest path) routes to such transfers consumes more energy than the actual transfer. Conventional routing protocols are thus unsuitable for transactions. In this paper, we present a novel architecture for transaction routing in large-scale ad

hoc networks. In our approach we aim at reducing the total energy consumption of successful delivery as opposed to finding shortest path routes. Our architecture uses a hybrid approach, where each mobile node obtains information about nodes in its proximity, up to R hops away, using a proactive link state protocol. Beyond the proximity, we introduce the novel notion of contacts that act as short cuts to reduce the degrees of separation between the request source and the target. We propose an efficient, on-demand, contact selection protocol. No location information is assumed. Extensive simulations are used to evaluate the performance of our protocol in terms of energy consumption and request success rate. We compare our architecture to flooding and ZRP. Our results show substantial power savings for our contact-based technique, especially for large networks. [C1691]

"A topology control algorithm for constructing power efficient wireless ad hoc networks"

In this paper, we present a localized algorithm for constructing power efficient topology for wireless ad hoc networks. Each mobile node determines its own transmission power based only on local information. The proposed algorithm first constructs the constrained Gabriel graph from the given unit disk graph and then reduces the total transmission power by allowing each node individually excises some replaceable links. The constructed topology is sparse, has a constant bounded power stretch factor, and the total transmission power is lower than those obtained from other proposed algorithms. In addition, compared with others, our algorithm requires lower time complexity to generate a solution, and can thus further save the energy for each mobile node. We demonstrate the performance improvements of our algorithm through simulations. [C1692]

"LRU-SEQ: a novel replacement policy for transition energy reduction in instruction caches"

Leakage energy will be the major energy consumer in future deep sub-micron designs. Especially the memory sub-system of future SOCs will be negatively affected by this trend. In order to reduce the leakage energy, memory banks are transitioned to a low-energy state when possible. This transition itself costs some energy which is termed as the transition energy. In this paper we present, as the first approach of its kind, a novel energy saving replacement policy called LRU-SEQ for instruction caches. Evaluation of the policy on various architectures in a system-level environment has shown that up to 23% energy savings can be obtained. Considering the negligible hardware impact, LRU-SEQ offers a viable choice for an energy saving policy. [C1693]

"Energy-constrained modulation optimization for coded systems"

We consider radio applications where the nodes operate on batteries so that energy consumption must be minimized while satisfying given throughput and delay requirements. In this context, we analyze the best modulation strategy to minimize the total energy consumption required to send a given number of bits when error-control codes are used. The total energy consumption includes both the transmission energy and the circuit energy consumption. We show that for both MQAM and MFSK the total energy consumption may be reduced significantly if the transmission time Tonis optimized to reduce the sum of transmission energy and circuit energy consumption. Our optimization considers both delay and peak-power constraints. Numerical examples are given, where we exhibit up to 90% energy savings over modulation strategies that minimize the transmission energy alone. We also show that the benefit of coding varies with the transmission distance and the underlying modulation schemes. [C1694]

"Reducing power consumption for high-associativity data caches in embedded processors"

Modern embedded processors use data caches with higher and higher degrees of associativity in order to increase performance. A set-associative data cache consumes a significant fraction of the total power budget in such embedded processors. This paper describes a technique for reducing the D-cache power consumption and shows its impact on power and performance of an embedded processor. The technique utilizes cache line address locality to determine (rather than predict) the cache way prior to the cache access. It thus allows only the desired way to be accessed for both tags and data. The proposed mechanism is shown to reduce the average L1 data cache power consumption when running the MiBench embedded benchmark suite for 8, 16 and 32-way set-associate caches by, respectively, an average of 66%, 72% and 76%. The absolute power savings from this technique increase significantly with associativity. The design has no impact on performance and, given that it does not have mis-prediction penalties, it does not introduce any new non-deterministic behavior in program execution. [C1695]

"Single-ISA heterogeneous multi-core architectures: the potential for processor power reduction"

This paper proposes and evaluates single-ISA heterogeneous multi-core architectures as a mechanism to reduce processor power dissipation. Our design incorporates heterogeneous cores representing different points in the

power/performance design space; during an application's execution, system software dynamically chooses the most appropriate core to meet specific performance and power requirements. Our evaluation of this architecture shows significant energy benefits. For an objective function that optimizes for energy efficiency with a tight performance threshold, for 14 SPEC benchmarks, our results indicate a 39% average energy reduction while only sacrificing 3% in performance. An objective function that optimizes for energy-delay with looser performance bounds achieves, on average, nearly a factor of three improvements in energy-delay product while sacrificing only 22% in performance. Energy savings are substantially more than chip-wide voltage/frequency scaling. [C1696]

"Software architectural transformations: a new approach to low energy embedded software"

Previous work on software optimization for low energy has focussed on instruction-level optimizations and compiler techniques. We argue, and demonstrate, that significant energy savings could be "left on the table" if energy is not considered during the design of the software architecture. As a first step towards addressing this gap, we propose a systematic framework for software architectural transformations to reduce energy consumption. We consider software architectural transformations in the context of the multi-process software style driven by an operating system (OS), which is very commonly employed in energy-sensitive embedded systems. Our methodology for applying software architectural transformations consists of: (i) constructing a software architecture graph representation, (ii) deriving initial energy and performance statistics using a detailed energy simulation framework, (iii) constructing sequences of atomic software architectural transformations, guided by energy change estimates derived from high-level energy macro-models, that result in maximal energy reduction, and (iv) generation of program source code to reflect the optimized software architecture. We employ a wide suite of software architectural transformations whose effects span the application-OS boundary, including how the program functionality is structured into architectural components (e.g., application processes, signal handlers, and device drivers), and connectors between them (inter- component synchronization and communication mechanisms). We present experimental results on several multi-process embedded software programs, in the context of an embedded system that features the Intel StrongARM processor and the embedded Linux OS. The presented results clearly underscore the potential of the proposed methodology (up to 66.1% reduction in energy is obtained). In a broader sense, our work demonstrates the impact of considering energy during the earlier stages of the software design process. [C1697]

"Utilizing solar power in wireless sensor networks"

Sensor networks are designed especially for deployment in adverse and non-accessible areas without a fixed infrastructure. Therefore, energy conservation plays a crucial role for these networks. We propose to utilize solar power in wireless sensor networks, establishing a topology where, changing over time, some nodes can receive and transmit packets without consuming the limited battery resources. We propose and evaluate two protocols that perform solar-aware routing. The presented simulation results show that both protocols provide significant energy savings when utilizing solar power. The paper shows that incorporating the solar status of nodes in the routing decision is feasible and results in reduced overall battery consumption. [C1698]

"Control flow driven splitting of loop nests at the source code level"

This paper presents a novel source code transformation for control flow optimization called loop nest splitting which minimizes the number of executed if-statements in loop nests of embedded multimedia applications. The goal of the optimization is to reduce runtimes and energy consumption. The analysis techniques are based on precise mathematical models combined with genetic algorithms. Due to the inherent portability of source code transformations, a very detailed benchmarking using 10 different processors can be performed. The application of our implemented algorithms to three real-life multimedia benchmarks leads to average speed-ups by 23.6%-62.1% and energy savings by 19.6%-57.7%. Furthermore, our optimization also leads to advantageous pipeline and cache performance. [C1699]

"SDRAM-Energy-Aware memory allocation for dynamic multi-media applications on multi-processor platforms"

Heterogeneous multi-processors platforms are an interesting option to satisfy the computational performance of dynamic multi-media applications at a reasonable energy cost. Today, almost no support exists to energy-efficiently manage the data of a multi-threaded application on these platforms. In this paper we show that the assignment of data of dynamically created/deleted tasks to the shared memory has a large impact on the energy consumption. We present two dynamic memory allocators which solve the bank assignment problem for shared multi-banked SDRAM memories. Both allocators assign the tasks' data to the available SDRAM banks such that the number of page-misses is reduced We have measured large energy savings with these allocators compared

to existing dynamic memory allocators for several task-sets based on MediaBench. [C1700]

"On-chip stack based memory organization for low power embedded architectures"

This paper presents an on-chip stack based memory organization that effectively reduces the energy dissipation in programmable embedded system architectures. Most embedded-systems use the notion of stack for implementation of function calls. However such stack data is stored in processor address space, typically in the main memory and accessed through caches. Our analysis of several benchmarks show that the callee saved registers and return addresses for function calls constitute a significant portion of the total memory accesses. We propose a separate stack-based memory organization to store these registers and return addresses. Our experimental results show that effective use of such stack-based memories yield significant reductions in system power/energy, while simultaneously improving the system performance. Application of our approach to the SPECint95 and MediaBench benchmark suites show up to 32.5% reduction in energy in L1 data caches, with marginal improvements in system performance. [C1701]

"Power efficiency through application-specific instruction memory transformations"

The instruction memory communication path constitutes a significant amount of power consumption in embedded processors. We propose an encoding technique that exploits application information to reduce the associated power consumption. The microarchitectural support enables reprogrammability of the encoding transformations so as to track code particularities effectively. The restriction to functional transformations enables effective coding while delivering major power savings, in the process obviating furthermore the necessity to rely on dictionary lookup, one of the major shortcomings of prior approaches. The frugal functional transformation, reliant on a single bit logic gate, introduces no impact to the critical fetch stage of the processor pipeline while delivering fully all the theoretically achievable power savings. The reprogrammable hardware implementation enables flexible and inexpensive switches between the transformations. Extensive experimental results on numerical and DSP codes confirm the theoretically expected magnitude of power savings, evincing reductions that range up to half of the original transitions. [C1702]

"A new hardware efficient, low power FIR digital filter implementation approach"

This paper presents a new hardware efficient approach for low power implementation of FIR digital filters. To reduce power consumption, filter's multipliers are split to global and local multiplication units by splitting CSD representation of filter coefficients (SCSD). This idea not only reduces the number of required adders for multipliers implementation, but also decreases logic depth in multiplier logic paths. For 8-bit coefficients, it achieves a hardware average saving improvement of 49% over CSD and 42% over DM representations. It was found that an average saving improvement of 39% over CSD and 18% over DM representations is achievable in 16-bit coefficients. [C1703]

"A 12-bit high performance low cost pipeline ADC"

This paper presents the design and implementation of a 2.5V 12-bit high performance and low cost pipeline Analog-to-Digital converter (ADC) architecture using CMOS technology. A modified flash ADC was employed instead of the traditional flash ADC to implement the sub-ADC in the designed pipeline ADC scheme to reduce the device complexity and attain lower system power consumption. The designed pipeline ADC architecture is operated at 400 MHz, consumes a total power of 47.7mW. Results indicates that 40% power saving is obtained at 400MHz when the modified flash ADC is used to implement the pipeline sub-ADC instead of a full flash ADC. Such pipeline ADC is the best candidate for many applications where power and size are the major factors. [C1704]

"A modified time synchronization function in IEEE 802.11 using differentiated contention window"

Time synchronization is an important design issue of wireless communication for time critical applications, in which the order or the simultaneously launching of events is of great interest. The IEEE 802.11 standard for wireless LAN specified a distributed coordinated function (DCF) mode, which is designed for the ad-hoc communication. Time synchronization function (TSF) has been defined as an essential component to support the frequency hopping spread spectrum (FHSS) physical layer and the power saving (PS) mode. In the PS mode specified for DCF, it requires that all the participating stations switch to active state and use contention based backoff mechanism to transmit the time synchronization beacon during each target beacon transmission time (TBTT). This paper presents a modification to the existing TSF for DCF by using differentiated backoff counter ranges according to the clock accuracy of stations. Using the proposed mechanism, the probability of collision among beacons can be significantly reduced. So less time is required for the successful transmission of beacon frames, which, in term of energy efficiency, is equivalent to less energy consumption. Furthermore, the clocks

can be converged quickly and a smaller clock deviation can also be achieved compared with previous approaches. [C1705]

"An evolutionary approach for reducing the switching activity in address buses"

In this paper we present two new approaches based on genetic algorithms (GA) to reduce power consumption by communication buses in an embedded system. The first approach makes it possible to obtain the truth table of an encoder that minimizes switching activity on a bus, whereas the second outputs the netlist of the encoder using the lowest possible number of logic gates. Both approaches are static, in the sense that the encoders are generated ad hoc for specific traffic. This is not, however, a limiting hypothesis if the application scenario considered is that of embedded systems. An embedded system, in fact, executes the same application throughout its lifetime and so it is possible to have detailed knowledge of the trace of the patterns transmitted on a bus following execution of a specific application. The approach is compared with the most efficient encoding schemes proposed in the literature on both multiplexed and separate buses. The results obtained demonstrate the validity of the approach, which on average saves up to 50% of the transitions normally required, as well as their practical applicability, even in an on-chip environment. [C1706]

"Detecting black-hole attack in mobile ad hoc networks"

The paper presents a general approach for detecting black-hole attacks in mobile ad hoc networks, which, due to their mobility and being broadcast in nature, are particularly vulnerable to attacks compared to traditional wired networks. In particular, black-hole attacks can be easily deployed by an adversary. To defend against this attack, we devise a neighborhood-based method to detect whether a black hole attack exists and a routing recovery protocol to set up a correct path to the true destination. Our methods have the remarkable advantage that the number of encryption/decryption operations for authentication is much reduced compared to those methods completely relying on cryptography-based authentication, thus saving many system resources (e.g. reducing energy consumption). Through simulation, we evaluate these methods in terms of packet throughput, routing control overhead, detection probability, false positive probability and false negative probability. Simulation results show that our methods can effectively detect black hole attacks in the sense that detection probability (the probability that one attacker might be detected) in most cases is above 93%. At the same time, it does not introduce much routing control overhead. With the routing recovery mechanism, the packet throughput can be improved by at least 15% and the false positive probability of the detection approach is very low (less than 1.7%). [C1707]

"A high-level optimization scheme for low power clock design"

Power consumption due to clock signals has been a major concern in synchronous VLSI chip design. This paper proposes a high-level power optimization scheme with two techniques: operator chaining, multiple clock. Chaining the operators with shorter delay allows the use of a lower clock frequency. With multiple clocks, the operators with longer delay can be driven by another clock with lower frequency. These techniques can be combined with clock gating to further reduce clock power consumption. The experiments with benchmarks show that the clock power reduction rate and total power savings are around 46% and 15%, on average, respectively, with a little or no performance degradation. [C1708]

"Feature pruning in likelihood evaluation of HMM-based speech recognition"

In this work, we present a simple yet effective technique to reduce the likelihood computation in ASR systems that use continuous density HMM. In a variety of speech recognition tasks, likelihood evaluation accounts for a significant portion of the total computational load. Our proposed method, under certain conditions, only evaluates the component likelihoods of certain features, and approximates those of the remaining (pruned) features by prediction. We investigate two feature clustering approaches associated with our pruning technique. While a simple sequential clustering works remarkably well, a data-driven approach performs even better in its attempt to save computation while maintaining baseline recognition accuracy. With the second approach, we can speed up the likelihood evaluation by 33% and reduce its power consumption by 27% for an isolated word recognition task. For a continuous speech recognition system using either monophone or triphone models, the speedup and power reduction of the likelihood evaluation are 50% and 35% respectively. [C1709]

"Development of energy-saving fusing technology for xerographic copying machine and printer"

In copying machines and printers using a xerographic system, most electrical power is consumed in the fusing process. Since existing fusing devices require a large heat capacity with a long warm-up time, they need to be kept at a constant temperature while printing is not conducted, resulting in large power consumption. On the other hand, using a thinner fuser roll with a small diameter for smaller heat capacity causes a roll deflection.

With the deflection, it cannot form a uniform fusing nip, making it difficult to ensure fusing performance. In order to solve this problem, we have developed a Roll-in-Roll fuser for mid-to-high volume monochrome machines, and also a Free Belt Nip Fuser (FBNF) for color machines, as the fusing technology that can correct the roll deflection. Furthermore, with these two fusers, the warm-up time has been reduced substantially, reducing the energy consumption as a result. [C1710]

"Chromatic encoding: a low power encoding technique for digital visual interface"

This paper presents a low-power encoding technique, called chromatic encoding, for the Digital Visual Interface standard (DVI), a digital serial video interface. Chromatic encoding reduces power consumption by minimizing the transition counts on the DVI. This technique relies on the notion of tonal locality, i.e., the observation that the signal differences between adjacent pixels in images follow a Gaussian distribution. Based on this observation, an optimal code assignment is performed to minimize the transition counts. Furthermore, the three color channels of the DVI may be reciprocally encoded to achieve even more power saving. The idea is that given the signal values from the three color channels, one or two of these channels are encoded by reciprocal differences with a number of redundant bits used to indicate the selection. The proposed technique requires only three redundant bits for each 24-bit pixel. Experimental results show up to a 75% transition reduction. [C1711]

"On reducing the average complexity of Turbo decoding with application to W-CDMA"

A simple but effective method for reducing the average complexity (and power consumption) of turbo decoding with negligible performance degradation in a W-CDMA environment is introduced. It modifies the conventional turbo-CRC decoding scheme by performing two CRC tests per iteration to detect at the earliest a correctly converged decoding process. When applied to a W-CDMA turbo code with frame length 640 bits at a BER of 10-6, it can save about 50% of the average decoding complexity, relative to the conventional scheme. Further complexity reduction can be achieved by integrating the CRC test as an intermediate step in the component SISO decoder. In general, the proposed scheme is more attractive for short-frame and low-BER applications. [C1712]

"A real-time reconfigurable pipelined architecture with advanced power management for UTRA-FDD"

A reconfigurable-pipelined architecture with advanced power management has been proposed for a mobile terminal receiver that can reduce power dissipation. The design can automatically scale the number of filter coefficients and word length respectively by monitoring the in-band and out-of- band powers. The new architecture performance was evaluated in a simulation UTRA-FDD environment. A power consumption analysis of the implemented architecture is also presented. The UTRA-FDD downlink mode was examined statistically and results show that the reconfigurable architecture can save an average 70 percent power dissipation when compared to a fixed filter length of 41 and ADC word length of 16 bits. This will prolong talk and standby time in a mobile terminal. The average number of taps and bits were calculated to be 11 and 7 respectively. [C1713]

"Application-driven network capacity adaptation for energy efficient ad-hoc networks"

In this paper, we propose a novel technique for reducing the energy consumption in idle mode. Our proposed technique called the network capacity adaptation derives an effective network capacity required by a given application and logically slows down the network capacity when the traffic load is low. By slowing down the logical network capacity, the neighboring mobile stations can stay longer in the power-off mode, significantly saving the energy consumed in idle mode. [C1714]

"Geocasting in cellular ad hoc augmented networks"

Delivering information to every user on a pre-specified geographic area via the Internet can be accomplished by geocasting in single-hop cellular networks. Geocasting is the mechanism to multicast messages to the network nodes whose physical locations lie within a given geographic area, termed the target area. In this paper, we propose the use of cellular ad hoc augmented network (CAHAN) architecture to improve total transmitted power expended for geocast services in cellular networks. CAHAN, in which ad hoc relaying technology is applied, is an evolutionary approach to conventional single-hop cellular networks. CAHAN regulates the number of hops between the base station and the mobile terminals (MTs) given a delay constraint. Notice that when the ad hoc communication range of each MT is zero, CAHAN simplifies to a conventional cellular network. We describe the CAHAN architecture, geocast session setup, geocast routing strategy, and power consumption models. The proposed architecture also implements a simple minimum-power path search scheme that can further reduce the total geocast energy in CAHAN. The advantages of CAHAN are demonstrated by comparing the geocasting performance of CAHAN with pure cellular networks in terms of total transmitted energy. We show that by using

CAHAN for geocasting, saving in total transmitted energy can be achieved as compared to the case of pure cellular networks. When the size of geocast target area is large, CAHAN can save larger transmitted energy. Finally, we show that the dense target area in CAHAN would save more transmitted energy in general. [C1715]

"A QoS oriented topological synthesis protocol for mobile backbone networks"

We have recently introduced mobile backbone network (MBN) based architecture for ad hoc wireless networks. For such networks, we have developed a distributed stable backbone maintenance protocol identified as MBNP. In the latter protocol, we employ mechanisms that convert backbone nodes (BNs) to serve in a non-backbone role (and then identified as backbone capable nodes, i.e. BCNs) when the backbone topology can operate reliably (and at acceptable capacity level) without such BNs. This conversion serves to save power consumption. In turn, when backbone connectivity demands it (in response to nodal mobility), BCNs are converted back to act as BNs. In this paper, we extended the BN to/from BCN conversion algorithm to operate in a manner that also meets quality-of-service (QoS) objectives and network capacity limitations in best supporting network flows. We show our new integrated MBNP conversion protocol to be stable (inducing no conversion oriented oscillations). We demonstrate, through the use of simulations, the throughput efficiency of our new QoS based topology synthesis protocol, in reducing control overhead, relieving network congestion and supporting a larger number of flows. [C1716]

"Contention free data transfers in IEEE 802.11 ad-hoc wireless LAN protocol: an analysis"

Stations in IEEE 802.11 ad-hoc WLAN protocol exchange frames by contending for the channel using CSMA/CA mechanisms and follow the binary exponential backoff for retransmitting the frames on collisions. This contention and collisions lead to low throughput. The protocol facilitates power saving in stations by allowing the stations to enter sleep mode. However, once these stations wakeup they can receive the frames only after contending for the channel. This leads to long awake periods and high power consumption. We have devised improved mechanisms that facilitate transmissions with reduced contention. Our mechanisms allow the data frames to be transmitted contention-free, leading to high throughput. The stations also have to keep awake for short duration to receive these frames in a contention-free manner, leading to high power saving. The mechanisms involve only minimal software changes to the existing protocol and can be implemented on the existing 802.11 WLAN cards. The stations following these mechanisms can co-exist in a standard 802.11 based ad-hoc WLAN. The average power consumption in our mechanisms is only 1/6thof the power consumed in 802.11b protocol, with the stations consuming 84% lesser power. Our maximum throughput improved to 25% higher than throughput of 802.11b protocol. [C1717]

"Implementation of low power fast Fourier transform"

This paper provides a novel low power high-speed computation of the fast Fourier transform (FFT) of complex floating-point data. This is achieved by designing the FFT butterfly operator to have reduced switching activity and lesser hardware. Normally the calculation of a butterfly requires eight real multiply and eight real addition operations. The proposed architecture requires only four real multiply and six real additions to compute the butterfly operator. Comparing the switching activity, a Two-fold reduction of switching activity has been observed at the input of the multiplier in proposed design. Dadda tree has been used for partial product reduction for its regularity in structure and optimal number of computational elements. The final two rows of partial products are reduced using carry save adder because of its high speed. The proposed design also takes relatively lesser number of clock cycles. [C1718]

"Transport protocol optimization for energy efficient wireless embedded systems"

For wireless embedded systems, the power consumption in the network interface (radio) plays a dominant role in determining battery life. In this paper, we explore transport protocol optimizations for reducing the energy consumption of wireless LAN interfaces. Our work is based on the observation that, the transport protocol, which implements flow control to regulate the network traffic, plays a significant role in determining the workload of the network interface. Hence, by monitoring run-time parameters in the transport protocol, coarse-granularity idle periods, which present the best opportunities for network interface power reduction, can be accurately identified. We further show that, by tuning parameters in the protocol software implementation, we can shape the activity profile of the network interface, making it more energy efficient while remaining compliant to the TCP standard. We have performed extensive current measurements using an experimental testbed that consists of a Compaq iPAQ PDA with a Cisco Aironet wireless network adapter, to validate the proposed techniques. Our measurements indicate energy savings ranging from 28% to 69% compared to the use of state-of-the-art MAC layer power reduction techniques, with little or no impact on performance. [C1719]

"Exploiting program hotspots and code sequentiality for instruction cache leakage management"

Leakage energy optimization for caches has been the target of much recent effort. In this work, we focus on instruction caches and tailor two techniques that exploit the two major factors that shape the instruction access behavior, namely, hotspot execution and sequentiality. First, we adopt a hotspot detection mechanism by profiling the branch behavior at runtime and utilize this to implement a HotSpot based Leakage Management (HSLM) mechanism. Second, we exploit code sequentiality in implementing a Just-InTime Activation (JITA) that transitions cache lines to active mode just before they are accessed.,We utilize the recently proposed drowsy cache that dynamically scales voltages for leakage reduction and implement various schemes that use different combinations of HSLM and JITA. Our experimental evaluation using the SPEC2000 benchmark suite shows that instruction cache leakage energy consumption can be reduced by 63%, 49% and 29%; on the average, as compared to an unoptimized cache, a recently proposed hardware optimized cache, and a cache optimized using compiler, respectively. Further, we observe that these energy savings can be obtained without a significant impact on performance. [C1720]

"The microarchitecture of a low power register file"

The access time, energy and area of the register file are often critical to overall performance in wide-issue microprocessors, because these terms grow superlinearly with the number of read and write ports that are required to support wide-issue. This paper presents two techniques to reduce the number of ports of a register file intended for a wide-issue microprocessor with hardly any impact on IPC. Our results show that it is possible to replace a register file with 16 read and 8 write ports, intended for an eight-issue processor, with a register file with just 8 read and 8 write ports so that the impact on IPC is a few percent. This is accomplished with the addition of several small auxiliary memory structures, a 'delayed write-back queue' and an 'operand prefetch buffer.' We examine several configurations employing these structures separately and in combination. In the case of just the delayed write-back queue, we show an energy per access savings of about 40% and an area savings of 40% . This incurs a performance loss of just 4%. The area savings in turn has the potential for further savings by shortening global interconnect in the layout. We also show that the performance loss can be almost eliminated if both techniques are used in combination, although some area and power savings is lost. [C1721]

"Pipeline stage unification: a low-energy consumption technique for future mobile processors"

Recent mobile processors are required to exhibit both low-energy consumption and high performance. To satisfy these requirements, dynamic voltage scaling (DVS) is currently employed. However, its effectiveness will be limited in the future because of shrinking the variable supply voltage range. As an alternative, we previously proposed pipeline stage unification (PSU), which unifies multiple pipeline stages without reducing the supply voltage at a power-saving mode. This paper compares effectiveness of PSU to DVS in current and future process generations. Our evaluation results show PSU will reduce energy consumption by 27-34% more than DVS after about 10 years. [C1722]

"Exploiting compiler-generated schedules for energy savings in high-performance processors"

This paper develops a technique that uniquely combines the advantages of static scheduling and dynamic scheduling to reduce the energy consumed in modern superscalar processors with out-of-order issue logic. In this Hybrid-Scheduling paradigm, regions of the application containing large amounts of parallelism visible at compile-time completely bypass the dynamic scheduling logic and execute in a low power static mode. Simulation studies using the Wattch framework on several media-arid scientific benchmarks demonstrate large improvements in overall energy consumption of 43% in kernels and 25% in full applications with only a 2.8% performance degradation on average. [C1723]

"Dynamic wordlength variation for low-power 3D graphics texture mapping"

The texture mapping stage, which facilitates high quality 3D graphics applications, consumes a significant amount of power for real-time processing because of its high computation and memory access requirements. An investigation into techniques that reduce its power consumption and provide scalable power-quality trade-offs is needed for its popular use in handheld devices such as PDAs. Two techniques and an associated architecture are presented, which achieve variable power savings by exploiting the perceptual tolerance of the end-user. These techniques leverage the lower weights of certain texture pixels and the correlation present between the neighboring texture pixels for supporting dynamic wordlength variation. A methodology is developed for fast power and error estimation based on realistic 3D graphics workloads. Power savings of about 21% at a slight quality degradation have been demonstrated and scalable power-quality trade-offs of more than 50% can also be achieved. The techniques can also be used for other stages of 3D graphics and image filtering. [C1724]

"A current-saving match-line sensing scheme for content-addressable memories"

A match-line sensing scheme that reduces power consumption in content-addressable memories by dynamically allocating less power to match-lines with more mismatches is described. This scheme is implemented in a 256Ч144 bit CAM using 1.2 V 0.13 μm CMOS achieving a 2 ns search time at 1.3 fJ/bit/search. [C1725]

"Energy optimization techniques in cluster interconnects"

Designing energy-efficient clusters has recently become an important concern to make these systems economically attractive for many applications. Since the links and switch buffers consume the major portion of the power budget of the cluster, the focus of this paper is to optimize the energy consumption in these two components. To minimize power in the links, we propose a novel dynamic link shutdown (DLS) technique. The DLS technique makes use of an appropriate adaptive routing algorithm to shutdown the links intelligently. We also present an optimized buffer design for reducing leakage energy. Our analysis on different networks using a complete system simulator reveals that the proposed DLS technique can provide optimized performance-energy behavior (up to 40% energy savings with less than 5% performance degradation in the best case) for the cluster interconnects. [C1726]

"Automatical exploration of low power architecture in co-design tool"

Energy consumption is a hot topic in the design of embedded systems. As mobile computing system (video camera, cellular phone, etc.) becomes more popular, how to lengthen the battery life of these systems becomes a critical issue. Also embedded system design is one of the most challenging tasks because the increasing complexity of new and various applications and the great variety of constraints to meet (lower cost, higher performance, lower energy). In this paper, we focus on the constraint of low energy consumption in hardware/software codesign tool. Our goal is to reach the best trade-off between system performance and energy consumption. For hardware and software units (DSP, RISC processors), we have developed a model of energy consumption and the methodology to evaluate the energy consumption of the designed systems. Then to reduce this energy, we introduce optimizations in allocation and scheduling steps. Experimental results show that this approach is promising and that it provides architectures with an energy saving of 50%. [C1727]

"Memory accesses reduction for MIME algorithm"

Power consumption of digital systems has become a critical design parameter. An important class of digital systems includes applications such as video image processing and speech recognition, which are extremely memory dominant. In such systems, a significant amount of power is consumed during memory accesses. Reducing the number of memory accesses can considerably impact the power dissipation in the rest of the design. Therefore, optimizing an application for reduced memory access can greatly effect the overall power consumption in the entire system. This paper presents an architectural enhancement multi-stage interval-based motion estimation (MIME) algorithm that not only saves power by reducing the number of memory accesses but also significantly increases the speedup. [C1728]

"Clock-tree power optimization based on RTL clock-gating"

As power consumption of the clock tree in modern VLSI designs tends to dominate, measures must be taken to keep it under control. This paper introduces an approach for reducing clock power based on clock gating. We present a methodology that, starting from an RTL description, automatically generates a set of constraints for driving the construction of the clock tree by the clock synthesis tool. The methodology has been fully integrated into an industry-strength design flow, based on Synopsys DesignCompiler (front-end) and Cadence Silicon Ensemble (back-end). The power savings achieved on some industrial examples show that, when the size of the circuits is significant, savings on the power consumption of the clock tree are up to 75% larger than those achieved by applying traditional clock gating at the clock inputs of the RTL modules of the designs. [C1729]

"A semi-custom voltage-island technique and its application to high-speed serial links [CCMOS active power reduction]"

Supply-voltage reduction is a known technique for reducing CMOS active power. We propose a semi-custom voltage-island approach based on internal regulation and selective custom design. This approach enables transparent embedding, since no additional external power supply is needed. We apply the approach to high-speed serial links, and we show that high performance is retained through targeted application of custom circuit and logic design. A chip is presented that evaluates the presented approach on a 3000 gate 3.2 Gbps multi-protocol serial-link receiver logic core. When reducing the supply from 1.2 V to 0.95 V, the chip demonstrates power savings of over 25%. [C1730]

"A selective filter-bank TLB system [Cembedded processor MMU for low power]"

We present a selective filter-bank translation lookaside buffer (TLB) system with low power consumption for embedded processors. The proposed TLB is constructed as multiple banks with a small two-bank buffer, called a filter-bank buffer, located above its associated bank. Either a filter-bank buffer or a main bank TLB can be selectively accessed, based on two bits in the filter-bank buffer. Energy savings are achieved by reducing the number of entries accessed at a time, by using filtering and the bank mechanism. The overhead of the proposed TLB turns out to be negligible compared with other hierarchical structures. Simulation results show that the energyЧdelay product can be reduced by about 88% compared with a fully -associative TLB, 75% with respect to a filter-TLB, and 51% relative to a banked-filter TLB. [C1731]

"Energy efficient D-TLB and data cache using semantic-aware multilateral partitioning"

The memory subsystem, including address translations and cache accesses, consumes a major portion of the overall energy on a processor. In this paper, we address the memory energy issues by using a streamlined architectural partitioning technique that effectively reduces energy consumption in the memory subsystem without compromising performance. It is achieved by decoupling the d-TLB lookups and the data cache accesses, based on the semantic regions defined by programming languages and software convention, into discrete reference substreams-stack, global static, and heap. Their unique access behaviors and locality characteristics are analyzed and exploited for power reduction. Our results show that an average of 35% energy can be reduced in the d-TLB and the data cache. Furthermore, an average of 46% energy can be saved by selectively multi-porting the semantic-aware d-TLBs and data caches against their monolithic counterparts. [C1732]

"Reducing data cache energy consumption via cached load/store queue"

High-performance processors use a large set-associative L1 data cache with multiple ports. As clock speeds and size increase such a cache consumes a significant percentage of the total processor energy. This paper proposes a method of saving energy by reducing the number of data cache accesses. It does so by modifying the load/store queue design to allow "caching" of previously accessed data values on both loads and stores after the corresponding memory access instruction has been committed. It is shown that a 32 entry modified LSQ design allows an average of 38.5% of the loads in the SpecINT95 benchmarks and 18.9% in the SpecFP95 benchmarks to get their data from the LSQ. The reduction in the number of LI cache accesses results in up to a 40% reduction in the L1 data cache energy consumption and in an up to a 16% improvement in the energy-delay product while requiring almost no additional hardware or complex control logic. [C1733]

"Reducing multimedia decode power using feedback control"

Despite recent advances, battery life continues to be a limiting factor in mobile multimedia systems. Significant energy savings can be achieved by adapting systems at runtime to match the execution requirements of different tasks. We introduce an online dynamic voltage/frequency scaling (DVS) feedback technique that reduces voltage and frequency to match the playback rate. A PI controller adjusts the decoder's speed to keep constant the occupancy of the buffer between the decoder and the display, effectively matching the average decode rate to the display rate without the need for any off-line profiling. MPEG simulation results show that this technique reduces decoder power consumption while providing strong real-time guarantees. [C1734]

"A study of hardware techniques that dynamically exploit frequent operands to reduce power consumption in integer function units"

We analyze three different techniques, namely, memoing (caching results that can be reused), narrow-width operand exploitation (limiting computation to low order bytes), and byte encoding (computation performed over significant bytes) that dynamically exploit operands to lower power consumption in integer function units. Previously, estimates of power savings based on switching activity were reported. Our implementation of integer function units (CLA, array multiplier, comparator, etc.) at the VLSI level and analysis using standard integer benchmarks from the SPEC CPU2000 suite provide realistic power savings and area and delay overheads. [C1735]

"NC-SRAM-a low-leakage memory circuit for ultra deep submicron designs"

In this paper, we present a novel N-controlled SRAM (NC-SRAM) design for reducing the subthreshold leakage in cache and embedded memories using a dual-Vtprocess. We combine the use of high Vttransistors in the leakage path and gating the supply voltage to reduce leakage in unused SRAM cells. This circuit-level technique overcomes the potential limitations in the existing techniques for reducing leakage in memory circuits. In this

design, the data stored in the cell is retained even when the memory is put in the stand-by mode, with no additional complexity or circuit overhead. Simulation results indicate that NC-SRAM has better leakage savings as compared to other techniques. In addition, our results on 100 nm and 70 nm processes show 21% and 18% reduction in total power and 77% and55 % reduction in leakage power, respectively, with very minimal impact on performance and area, as compared to a conventional 6T-SRAM. [C1736]

"Performance evaluation of IP paging with power save mechanism"

We evaluate the performance of IP paging with power save mechanism by formulating an analytical model and carrying out simulation study of integrated IP paging protocol (HPP) that integrates both the paging and power save functionality in IP layer. The results show that, compared to the mobile IP regional registration, the UPP significantly reduces the average power consumption of a mobile node and the signaling load in the access networks, while providing link layer independent mobility and power management functions. [C1737]

"An access pattern based energy management strategy for instruction caches"

Increasing leakage energy consumption is an important problem for SOC-based platforms as such platforms rely on large on-chip SRAMs. While most of the previous techniques focus on hardware based leakage optimization, in this paper, we present an application access pattern oriented strategy for reducing instruction cache leakage energy. This strategy keeps track of the dynamic transitions between the procedures of a given application, and tries to keep the cache lines not used by the current procedure in a power-down state as much as possible. Our simulation results indicate significant savings in leakage energy. [C1738]

"Precomputation-based guarding for dynamic and leakage power reduction"

We present a precomputation-based guarding technique to reduce both dynamic and static power consumptions in CMOS VLSI circuits. More precisely, a high threshold sleep transistor is placed in series with some portions of the circuit. Based on the input values of the circuit, the sleep transistor is turned on and off, thus, saving both dynamic and static power. We show how to apply this technique to a number of common arithmetic blocks, including comparators, adders and multipliers. Finally, dynamic guarding and sleep transistor activity reduction techniques for improving the performance of the method are presented. Experimental results show 81% reduction in the power consumption of data path modules of a commercial VLIW processor can be achieved using our techniques. This is 20% higher than what has been achieved by previous methods. [C1739]

"On reducing register pressure and energy in multiple-banked register files"

The storage for speculative values in superscalar processors is one of the main sources of complexity and power dissipation. We present a novel technique to reduce register requirements as well as their dynamic and static power dissipation that is based on delaying the dispatch of instructions while minimizing its impact on performance. The proposed technique outperforms previous schemes in both performance and power savings. With only 1.77% IPC loss, the mechanism achieves more than 13% dynamic and 15% static extra power savings in the integer rename buffers and more than 9% dynamic and 10% static extra power savings in the FP rename buffers. Significant power savings are also achieved if the processor uses a physical register file for both committed and noncommitted values instead of rename buffers. Additionally the register requirements are reduced by more than 18% and 13% for integer and FP programs respectively. [C1740]

"Energy efficient asymmetrically ported register files"

Power consumption in the register file (RF) forms a considerable fraction of the total power consumption in a chip. With increasing instruction window sizes and issue widths, RF power consumption will suffer a significantly large growth. Using the fact that many of the register values are small and require only a small number of bits for representation, we propose a novel asymmetrically ported RF (to reduce RF power consumption), in which some of the ports can only read/write small-sized values. We experiment with both monolithic and partitioned versions of asymmetrically ported RFs. The power savings in the RF with partitioned asymmetrically ported RF reach as high as 60%. These reductions in RF power consumption come with about 40% improvement in RF access-time and a negligible impact on IPC (instructions per cycle). [C1741]

"Multiple-Vdd scheduling/allocation for partitioned floorplan"

We propose a multiple-Vddscheduling and allocation scheme for low-power that considers a partitioned floorplan. Multiple-Vdddesigns inevitably introduce an additional power mesh, thus consuming an additional metal layer. Considering voltage partition during scheduling, we may place the resources of same voltage in one partition; thereby reducing the additional power meshes. Such a schedule can also reduce the interfaces between different

voltage partitions. Therefore, the logic level-converters and the interconnects can be reduced. To accomplish this, we first generate a multiple-Vddschedule using force-directed scheduling. Given resource and time constraints, the multiple-Vddscheduler determines the voltage assignment of each node with resource constraints. Next, voltage partitioning is performed. Based on pair-wise and multiple-way graph partitioning, the voltage partitioning algorithm iteratively improves the schedule and the allocation. The proposed scheme generates a multiple-Vddschedule for an improved voltage partitioned floorplan. Reduction of level-converter cost, interconnect cost, and the number of voltage clusters were achieved. Relative to the minimum single voltage design, the average energy savings of a multiple-Vddpartitioned design was 29.7%. Reductions of 33.1%, 28.3%, 51.3% were achieved for level-conversion energy, total bus length and interconnect energy, respectively. [C1742]

"Automatic data migration for reducing energy consumption in multi-bank memory systems"

An architectural solution to reducing memory energy consumption is to adopt a multi-bank memory system instead of a monolithic (single-bank) memory system. Some recent multi-bank memory architectures help reduce memory energy by allowing an unused bank to be placed into a low-power operating mode. This paper describes an automatic data migration strategy which dynamically places the arrays with temporal affinity into the same set of banks. This strategy increases the number of banks which can be put into low-power modes and allows the use of more aggressive energy-saving modes. Experiments using several array-dominated applications show the usefulness of data migration and indicate that large energy savings can be achieved with low overhead. [C1743]

"Solving raw material challenges [Ccement industry]"

A comprehensive understanding of the chemical and physical aspects of raw material transformation into clinker is an important foundation to increasing production, reducing costs, and improving quality at the cement plant. Clinker formation relies on numerous kiln feed properties and pyroprocessing conditions. Understanding the influential properties of the feed (chemistry, fineness, uniformity, and mineralogy) can lead to improvements in its burnability and therefore in the efficiency of plant operations. The paper discusses clinker formation, its relation to kiln feed properties, and the importance of optimizing burnability by careful mix control, good mix homogeneity, and tailoring the burning process to the raw mix. The burnability and kiln feed are discussed in relation to specific fuel consumption. When the raw materials available make it hard to achieve burnability goals, the use of fluxes and/or mineralizers may be helpful. Fluxes and mineralizers indirectly affect burnability by promoting clinker phase formation to occur earlier; their effect on clinker formation and cement quality is briefly described. Fluoride-containing compounds have proven to be the most effective mineralizers in cement clinkering reactions. However, an excessive amount of fluoride may delay cement setting time. Emphasis is placed on the effects of changes in raw material burnability and clinker formation on kiln operations, finish mill productivity, and the properties of the resulting cement [C1744]

"An energy saving strategy based on adaptive loop parallelization"

In this paper, we evaluate an adaptive loop parallelization strategy (i.e., a strategy that allows each loop nest to execute using a different number of processors, if doing so is beneficial) and measure the potential energy savings when unused processors, during execution of a nested loop in a multi-processor on-a-chip (MPoC), are shut down (i.e., placed into a power-down or sleep state). Our results show that shutting down unused processors can lead to as much as 67% energy savings with up to 17% performance loss in a set of array-intensive applications. We also discuss and evaluate a processor pre-activation strategy based on compile-time analysis of nested loops. Based on our experiments, we conclude that an adaptive loop parallelization strategy combined with idle processor shut-down and pre-activation can be very effective in reducing energy consumption without increasing execution time. [C1745]

"A low-voltage low-power fast-settling operational amplifier for use in high-speed high-resolution pipelined A/D converters"

The most power-hungry circuit in a high-speed high-resolution pipelined analog-to-digital converter is the first stage opamp. In this paper a 1.5 V two-stage opamp is proposed which uses the cascode compensation to achieve a bandwidth higher than the miller compensation and also a class-A/AB output stage to reduce the high current needed in the opamp second stage to satisfy the slew-rate performance. HSPICE simulations show that considerable power is saved merging these two techniques in a 0.25 μm CMOS process. [C1746]

"Evaluation on power reduction applying gated clock approaches"

In this paper the use of the gated clock approach to reduce power consumption is analyzed and compared. The

approach has been implemented following three different strategies that allow the approach to be efficiently used under different design conditions. To verify the strength of the approach it has been implemented during the design of a programmable interrupt controller (PIC). The results found show a 2Ч factor reduction in the average power consumption through the use of the three strategies. Moreover, the results have been also compared with those obtained through an automatic implementation of one of the gated clock strategies allowed by Synopsys's power compiler. In this second case only about 25% of power consumption is saved. It is worth noting that implementation of the three gated clock strategies leads also to a design with the smallest gate count. [C1747]

"Low-swing clock domino logic incorporating dual supply and dual threshold voltages"

High-speed domino logic is now prevailing in the performance critical block of chips. A Low Voltage Swing Clock (LVSC) domino logic family is developed for substantial dynamic power saving. To boost transition speed in the proposed circuitry, a well-established dual threshold voltage technique is exploited. A dual supply voltage technique in the LVSC domino logic is geared to reduce power consumption in the clock tree and logic gates effectively. A Delay Constrained Power Optimization (DCPO) algorithm allocates low supply voltage to logic gates such that the dynamic power consumed by logic gates is minimized. Delay time variations due to gate-to-source voltage change and and input signal arrival time difference are considered for accurate timing analysis in DCPO. [C1748]

"90% write power saving SRAM using sense-amplifying memory cell"

Summary form only given. A low power write scheme is proposed for an SRAM using seven-transistor sense-amplifying memory cells, which can save 90% of the power in write cycles when 4M SRAM is assumed. By reducing the bit line swing to 1/6 VDDand amplifying the voltage swing by a sense-amplifier structure in a memory cell, charging and discharging component of the power of the bit lines is reduced. A 64 Kbit test chip has been fabricated and operation has been verified. [C1749]

"Static pulsed bus for on-chip interconnects"

Summary form only given. Static Pulsed Bus (SPB) improves delay by 15%-25% or reduces energy by 12%-25% and peak current by 26%-34%, compared to the conventional static bus (SB) scheme, for 1500 µm to 4500 µm bus lengths in a 100 nm technology. Energy savings are maintained across all data activity factors. [C1750]

"Noise tolerant low power dynamic TSPCL D flip-flops"

The extensive use of a dynamic circuit techniques for higher performance has already been implemented in many circuits like microprocessors. With the scaling down to deep submicron technology and the move towards dynamic circuit techniques, noise immunity is becoming an important metric like power, speed, and area. This paper proposes a technique to achieve low energy consumption in TSPCL D flip-flops. The paper studies some published flip-flops and carries out a modification that reduces the switching activity of some internal nodes, causing a big saving in power consumption. The proposed flip-flop is characterized and compared with those published ones for reliability and energy efficiency. Comparison for speed, power consumption, and noise tolerance is also presented. The average noise threshold energy (ANTE) and the energy normalized ANTE metrics are used for quantifying the noise immunity and energy efficiency, respectively of flip-flops. Results using 0.18 µm CMOS technology and HSPICE for simulation, show that the proposed TSPCL D flip-flop achieves reduction in power dissipation ranging from 4.6% to 80% depending on the input pattern and the technology in use. The noise immunization curves show that the modified flip-flop is more susceptible to noise. Hence, one of the known noise immunization techniques should be applied [C1751]

"Energy estimation and optimization of embedded VLIW processors based on instruction clustering"

Aim of this paper is to propose a methodology for the definition of an instruction-level energy estimation framework for VLIW (very long instruction word) processors. The power modeling methodology is the key issue to define an effective energy-aware software optimisation strategy for state-of-the-art ILP (instruction level parallelism) processors. The methodology is based on an energy model for VLIW processors that exploits instruction clustering to achieve an efficient and fine grained energy estimation. The approach aims to reduce the complexity of the characterization problem for VLIW processors from exponential, with respect to the number of parallel operations in the same very long instruction, to quadratic, with respect to the number of instruction clusters. Furthermore, the paper proposes a spatial scheduling algorithm based on a low-power reordering of the parallel operations within the same long instruction. Experimental results have been carried out on the Lx processor, a 4-issue VLIW core jointly designed by HPLabs and STMicroelectronics. The results have shown an

average error of 1.9% between the cluster-based estimation model and the reference design, with a standard deviation of 5.8%. For the Lx architecture, the spatial instruction scheduling algorithm provides an average energy saving of 12%. [C1752]

"A new reduced clock-swing flip-flop: NAND-type keeper flip-flop (NDKFF)"

A new reduced clock-swing flip-flop, named NAND-type Keeper Flip-Flop (NDKFF) is proposed. Compared with other conventional reduced clock-swing flip-flops such as HSFF and RCSFF, NDKFF features a simple configuration, which does not have additional clock drivers or does not have additional nand/or p-wells. Compared with the hybrid-latch flip-flop, 52% of the flip-flop power and 64% of the clocking power are saved in the case of 0.25 μm CMOS technology. Moreover CLK-to-Q delay is comparable to that of conventional C2MOS-type master-slave flip-flop. [C1753]

"Input space adaptive embedded software synthesis"

This paper presents a novel technique, called input space adaptive software synthesis, for the energy and performance optimization of embedded software. The proposed technique is based on the fact that the computational complexities of programs or sub-programs are often highly dependent on the values assumed by input and intermediate program variables during execution. This observation is exploited in the proposed software synthesis technique by augmenting the program with optimized versions of one or more sub-programs that are specialized to, and executed under, specific input sub-spaces. We propose a methodology for input space adaptive software synthesis which consists of the following steps: control and value profiling of the input program, application of compiler transformations as a preprocessing step, identification of sub-programs and corresponding input sub-spaces that hold the highest potential for optimization, and transformation of the sub-programs to realize performance and energy savings. We have evaluated input space adaptive software synthesis by compiling the resulting optimized programs to two commercial embedded processors (Fujitsu SPARCliteTMand Intel StrongARMTM). Our experiments indicate that our techniques can reduce energy consumption of the whole program by up to 7.8Ч (an average of 3.1Ч for SPARClite and 2.6Ч for StrongARM) while simultaneously improving performance by up to 8.5Ч (an average of 3.1Ч for SPARClite and 2.7Ч for StrongARM), leading to an improvement in the energy-delay product by up to 66.7Ч (an average of 8.2Ч for SPARClite and 6.3Ч for StrongARM), at the cost of minimal code size overheads (an average of 5.9%) [C1754]

"Minimizing energy consumption for high-performance processing"

Power consumption is becoming an increasingly important constraint in the design of microprocessors. This paper examines the use of multiple constrained processors running at lowered voltage and frequency to perform a similar amount of work in less time and lower power than a uniprocessor The paper also studies the effect of reducing cache and Branch Target Buffer (BTB) sizes for further reducing power consumption while still providing adequate performance. The best configuration requiring four processors reduced energy by 56%. Reducing cache and BTB provided a further 16% savings in energy while still finishing the workload in the same amount of time as the uniprocessor [C1755]

"Hardware-assisted data compression for energy minimization in systems with embedded processors"

In this paper, we suggest hardware-assisted data compression as a tool for reducing energy consumption of core-based embedded systems. We propose a novel and efficient architecture for on-the-fly data compression and decompression whose field of operation is the cache-to-memory path. Uncompressed cache lines are compressed before they are written back to main memory, and decompressed when cache refills take place. We explore two classes of compression methods, profile-driven and differential, since they are characterized by compact HW implementations, and we compare their performance to those provided by some state-of-the-art compression methods (e.g., we have considered a few variants of the Lempel-Ziv encoder). We present experimental results about memory traffic and energy consumption in the cache-to-memory path of a core-based system running standard benchmark programs. The achieved average energy savings range from 4.2% to 35.2%, depending on the selected compression algorithm [C1756]

"Minimizing energy consumption of secure wireless session with QoS constraints"

We investigate techniques to minimize the energy consumed by a secure wireless session without compromising the security of the session. While we have shown elsewhere (see Karri, R. and Mishra, P., submitted to ACM MOBIHOC 2002; http://emme.poly.edu/Goodies/TEMP/MOBIHOC2002.pdf) that the energy consumed by a secure session is reduced by compressing the session negotiation messages, the protocol header and the data, we now show that it is important to match the block size of compression to the data cache size of the device.

We also investigate the choice of a bulk encryption algorithm (3DES vs. AES) and a key exchange protocol (Diffie-Hellman vs. RSA) based on the energy consumed by a secure wireless session. These techniques yield energy savings of 1.3Ч during data transmission and 1.2Ч during data reception beyond those obtained by techniques given in our cited paper. These techniques complement and supplement those proposed in that paper, and when combined, yield overall energy savings of 2.1Ч during data transmission and 4.35Ч during data reception. [C1757]

"Profile-based dynamic voltage scheduling using program checkpoints"

Dynamic voltage scaling (DVS) is a known effective mechanism for reducing CPU energy consumption without significant performance degradation. While a lot of work has been done on inter-task scheduling algorithms to implement DVS under operating system control, new research challenges exist in intra-task DVS techniques under software and compiler control. In this paper we introduce a novel intra-task DVS technique under compiler control using program checkpoints. Checkpoints are generated at compile time and indicate places in the code where the processor speed and voltage should be re-calculated. Checkpoints also carry user-defined time constraints. Our technique handles multiple intra-task performance deadlines and modulates power consumption according to a run-time power budget. We experimented with two heuristics for adjusting the clock frequency and voltage. For the particular benchmark studied, one heuristic yielded 63% more energy savings than the other. With the best of the heuristics we designed, our technique resulted in 82% energy savings over the execution of the program without employing DVS [C1758]

"Reducing energy consumption in a clustered MANET using the intra cluster data-dissemination protocol (Icdp)"

An efficient and reliable solution to data broadcasting is hard to obtain. Reliable energy-efficient data broadcasting is even harder to obtain when dealing with wireless networks where battery energy is a limited resource. We present a study which evaluates different power aware approaches to provide reliable broadcasting in a dynamic MANET. We present the intra-cluster data-dissemination protocol (Icdp). The Icdp is used to group nodes around a special one, called the cluster leader (CL). The CL centralizes the power management mechanism and acts as a proxy for data transfer between the cluster and the rest of the nodes in the region. When a cluster node enables the power management it goes into "sleep" mode, to minimize power consumption. The CL buffers data frames for power saving stations and delivers them on station request. We periodically distribute the cluster leader role among all the nodes inside the cluster to not overload a single node. We compare few different traffic broadcasting policies and evaluate their impact comparing Icdp to a classical IEEE 802.11 scheme. We show that in constant bit rate (CBR) and variable bit rate (VBR) cases, we can save up to 30% of NIC's energy, while preserving packet end-to-end delay and packet loss rate values [C1759]

"Pruning-based energy-optimal device scheduling for hard real-time systems"

Dynamic power management (DPM) provides a simple, elegant and flexible method for reducing energy consumption in embedded real-time systems. However, I/O-centric DPM techniques have been studied largely for non-real-time environments. We present an offline device scheduling technique for real-time systems that generates an energy-optimal device schedule for a given task set while guaranteeing that all real-time deadlines are met. Our method takes as inputs a task set and a device-usage list for each task, and it schedules the tasks such that the energy consumed by the set of I/O devices is minimized. We compare our algorithm to an exhaustive enumeration method and show that the proposed algorithm is very efficient in terms of memory usage and computation time. We also present case studies to show that I/O-centric DPM methods can result in significant energy savings [C1760]

"Dynamic voltage scaling algorithm for dynamic-priority hard real-time systems using slack time analysis"

Dynamic voltage scaling (DVS), which adjusts the clock speed and supply voltage dynamically, is an effective technique in reducing the energy consumption of embedded real-time systems. The energy efficiency of a DVS algorithm largely depends on the performance of the slack estimation method used in it. In this paper, we propose a novel DVS algorithm for periodic hard real-time tasks based on an improved slack estimation algorithm. Unlike the existing techniques, the proposed method takes full advantage of the periodic characteristics of the real-time tasks under priority-driven scheduling such as EDF. Experimental results show that the proposed algorithm reduces the energy consumption by 20 40 % over the existing DVS algorithm. The experiment results also show that our algorithm based on the improved slack estimation method gives comparable energy savings to the DVS algorithm based on the theoretically optimal (but impractical) slack estimation method. [C1761]

"Energy savings through compression in embedded Java environments"

Limited energy and memory resources are important constraints in the design of an embedded system. Compression is a useful and widely employed mechanism to reduce the memory requirements of the system. As the leakage energy of a memory system increases with its size and because of the increasing contribution of leakage to overall system energy, compression also has a significant effect on reducing energy consumption. However, storing compressed data / instructions has a performance and energy overhead associated with decompression at runtime. The underlying compression algorithm, the corresponding implementation of the decompression and the ability to reuse decompressed information critically impact this overhead. In this paper, we explore the influence of compression on overall memory energy using a commercial embedded Java virtual machine (JVM) and a customized compression algorithm. Our results show that compression is effective in reducing energy even when considering the runtime decompression overheads; for most applications [C1762]

"Minimum energy fixed-priority scheduling for variable voltage processors"

To fully exploit the benefit of variable voltage processors, voltage schedules must be designed in the context of work load requirement. In this paper, we present an approach to finding the least-energy voltage schedule for executing real-time jobs on such a processor according to a fixed priority, preemptive policy. The significance of our approach is that the theoretical limit in terms of energy saving for such systems is established, which can thus serve as the standard to evaluate the performance of various heuristic approaches. Two algorithms for deriving the optimal voltage schedule are provided. The first one explores fundamental properties of voltage schedules while the second one builds on the first one to further reduce the computational cost. Experimental results are shown to compare the results of this paper with previous ones [C1763]

"Potential benefits of implementing load control"

The design of wholesale electricity markets through deregulation has focused almost exclusively on the development of competitive supply (generation). The demand side of the market has been virtually ignored. Mostly, this is due to the assumption that electricity demand is almost completely inelastic. As a result, deregulated wholesale markets universally fail to pass price signals down to the end-users. This paper challenges the assumption of inelastic demand by exploring the potential benefits of implementing a simple load control scheme. This load control scheme allows consumers to shift demand from high priced hours to low priced hours during the day. The benefits to the individual consumer are explored through an example applied to residential air conditioning using price and demand data from California. This example shows that "smart" use of air conditioning can lead to great savings for residential consumers, without sacrificing comfort. The potential for multiple consumers implementing load control to reduce wholesale prices is also examined. [C1764]

"VLSI design and implementation of high-speed Viterbi decoder"

This paper presents a new architecture for high-speed Viterbi decoder with low power dissipation based on the modified T-algorithm and modified trace-back methods. The former algorithm is used to reduce the unnecessary operations in path metric computation, while the latter is adopted to reuse the already generated trace-back routes to reduce the times of trace-back operations, so the power consumption can be saved. High throughput and short decoding latency are achieved by parallel computation in the add-compare-select unit and pipeline structure in the survivor-memory-unit. The complexity of the (2,1,7) Viterbi decoder is about 50,000 gates with a decoding latency of 32 clock cycles, and an area of 3.88 mm2including IO pad with a throughput of 200 Mb/s using 0.25 μm technology. [C1765]

"VLSI implementation of a high-speed and low-power punctured Viterbi decoder"

This paper presents a new architecture of punctured Viterbi decoder with high-speed and low-power based on the modified T-algorithm and trace-back method. To gain high throughput and short decoding latency, parallel computations in ACSU and SMU are adopted. Furthermore, to save the power consumption, the unnecessary computations of path metric are omitted in the add-compare-select-unit (ACSU) and the already generated back-tracing routes are reused to reduce the times of trace-back operations in the survivor-memory-unit (SMU). The decoding latency of the (2,1,7) Viterbi decoder is only 34 clock cycles, the total average power is 185 mW with 200 Mb/s throughput using 0.25 μm CMOS technology. [C1766]

"Energy-conserving reception protocols for mobile ad hoc networks"

The importance of conserving the limited battery energy available in mobile tactical communication systems is well appreciated in their design. Radio transceivers are major energy consumers in such systems, however

fundamental advancements to increase battery capacity and/or reduce transceiver power requirements are not expected in the near future; therefore, energy-conserving techniques are the main avenue for extending system life. In this paper, we propose a suite of reception protocols that support episodic powering down of the radio receiver during periods of low communication activity. The suite covers a range of varying implementation complexion, control-traffic overhead, and energy-saving capability, thus an appropriate solution can be selected according to the particular tactical application. The protocols are considered in the framework of asynchronous (e.g. CSMA) channel access but can be easily adapted to synchronous channel access methods as well. We evaluate the performance of two protocols from the suite in the context of a proactive link-state routing protocol and show that they are capable of significantly reducing energy consumption with little additional complexity and acceptable performance penalties. [C1767]

"A data broadcast scheme based on prediction for the wireless environment"

Broadcasting is an essential paradigm to transport data and support scalability in the wireless environment. Traditional index-based broadcast schemes take advantage of tree structures for saving energy but they record too much index information to make the broadcast cycle short. On the other hand, the hash scheme may suffer from longer broadcast cycles and data collision problems, resulting in longer access and tuning time. In this paper we propose a novel broadcast scheme, named predictive indexing, which allows mobile clients to access data by predicting data locations in the broadcast cycle. The new scheme not only has very compact structure, but also is flexible enough to allow the server to adjust the index structure for saving energy or reducing access time. Experimental studies show that it outperforms the tree-based schemes 2.5 times in energy saving, while maintaining roughly the same access time. It also outperforms the flexible indexing 70% and the hash scheme 80% in energy consumption. [C1768]

"A study on the potential of corn cob engine-generator for electricity generation in Thailand"

This paper describes the potential of using corn cob as a primary energy source for electricity generation in Thailand. Due to increase in energy demands, fuel cost, and environmental issues, the reliance of fossil fuel has to be reduced. One of the alternatives is to utilize agricultural residues. This paper provides an overview of the availability of corn cob in Thailand and a description of a small-scaled biomass gasifier engine-generator. Based on literature research and estimation, over 1 GWh/year could be produced from this technique. This will provide substantial savings on fuel cost and reduction on environmental impacts. In addition to the generation of electricity, this also provides a safe means to dispose the waste residues. This is an initial phase of an ongoing project to be undertaken in Phitsanulok, Thailand. [C1769]

"A low power implementation for the motion estimation processor"

This paper presents a low power video motion estimation processor. The combination of motion fuzzy prediction and modified four-step search algorithm (4SS) gives faster and more correct searching results. With the analysis of the relationship between the consecutive search iterations, some of the searching operations are saved which enhance the computing efficiency and reduce power consumption. Experimental results demonstrate the higher performance in both PNSR and computation complexity compared to other systems. [C1770]

"Generating physical addresses directly for saving instruction TLB energy"

Power consumption and power density for the Translation Lookaside Buffer (TLB) are important considerations not only in its design, but can have a consequence on cache design as well. This paper embarks on a new philosophy for reducing the number of accesses to the instruction TLB (iTLB) for power and performance optimizations. The overall idea is to keep a translation currently being used in a register and avoid going to the iTLB as far as possible-until there is a page change. We propose four different approaches for achieving this, and experimentally demonstrate that one of these schemes that uses a combination of compiler and hardware enhancements can reduce iTLB dynamic power by over 85% in most cases. These mechanisms can work with different instruction-cache (iLl) lookup mechanisms and achieve significant iTLB power savings without compromising on performance. Their importance grows with higher iLl miss rates and larger page sizes. They can work very well with large iTLB structures, that can possibly consume more power and take longer to lookup, without the iTLB getting into the common case. Further, we also experimentally demonstrate that they can provide performance savings for virtually-indexed, virtually-tagged iLl caches, and can even make physically-indexed, physically-tagged iLl caches a possible choice for implementation. [C1771]

"Three-dimensional memory vectorization for high bandwidth media memory systems"

Vector processors have good performance, cost and adaptability when targeting multimedia applications. However, for a significant number of media programs, conventional memory configurations fail to deliver enough

memory references per cycle to feed the SIMD functional units. This paper addresses the problem of the memory bandwidth. We propose a novel mechanism suitable for 2-dimensional vector architectures and targeted at providing high effective bandwidth for SIMD memory instructions. The basis of this mechanism is the extension of the scope of vectorization at the memory level, so that 3-dimensional memory patterns can be fetched into a second-level register file. By fetching long blocks of data and by reusing 2-dimensional memory streams at this second-level register file, we obtain a significant increase in the effective memory bandwidth. As side benefits, the new 3-dimensional load instructions provide a high robustness to memory latency and a significant reduction of the cache activity, thus reducing power and energy requirements. At the investment of a 50% more area than a regular SIMD register file, we have measured and average speed-up of 13% and the potential for power savings in the L2 cache of a 30%. [C1772]

"Frame-based dynamic voltage and frequency scaling for a MPEG decoder"

This paper describes a dynamic voltage and frequency scaling (DVFS) technique for MPEG decoding to reduce the energy consumption while maintaining a quality of service (QoS) constraint. The computational workload for an incoming frame is predicted using a frame-based history so that the processor voltage and frequency can be scaled to provide: the exact amount of computing power needed to decode the frame. More precisely, the required decoding time for each frame is separated into two parts: a frame-dependent (FD) part and a frame-independent (FI) part. The FD part varies greatly according to the type the incoming frame whereas the FI part remains constant regardless of the frame type. In the DVFS scheme presented in this paper the FI part is used to compensate for the prediction error that may occur during the FD part such that a significant amount of energy can be saved while meeting the frame rate requirement. The proposed DVFS algorithm has been implemented on a StrongArm-1110 based evaluation board. Measurement results demonstrate a higher than 50% CPU energy saving as a result of DVFS. [C1773]

"RISE: reducing interference and saving energy through multicasting in ad hoc wireless networks"

We develop an approach that makes use of directional antennas to improve the performance of multicasting in ad hoc wireless networks. We first assume that multicast trees are known for all the active sessions. The antenna beamwidth at the network nodes is determined in such a way that both the nodes' transmit power and the interference among simultaneous transmissions are reduced, while the signal power at the intended receivers remains unchanged. We propose a model to study the performance improvement that results solely from interference reduction by using directional antennas. The proposed approach is then applied to a simple distributed algorithm for multicast tree construction and the performance is evaluated. [C1774]

"Development of load control and management system"

This paper presents the conservation of electrical energy in building with the technique to develop load control and management system in order to adjust load factor of system. Using the limiting and controlling the maximum demand, we can acquire the prediction and compare it to the maximum demand set point. This system consists of a computer which works as controller, processor and database unit and works with digital power meter informing of multidrop network by serial communication via RS-485. The control system use PLC to control load via serial communication RS-485. The data of measurement such as voltage, current, power, power factor, energy, etc., can be saved as a database and analysed. The load factor adjustment by limiting and controlling maximum demand can reduce the cost of electric consumption and energy generation. [C1775]

"Power protocol: reducing power dissipation on off-chip data buses"

Power consumption is becoming increasingly important for both embedded and high-performance systems. Off-chip data buses can be a major power consumer. In this paper we present a strategy called "power protocol" that tries to reduce the dynamic power dissipation on off-chip data buses. To accomplish this, our strategy reduces the number of bus lines that need to be activated for data transfer by employing a small cache (called "value cache") at each side of the off-chip data bus. These value caches keep track of the data values that have recently been transmitted over the bus. The entries in these caches are constructed in such a way that the contents of both the value caches are the same all the time. When a data value needs to be transmitted over the bus, we first check whether it is in the value cache of the sender. If it is, we transmit only the index of the data (i.e., its value cache address) instead of the actual data value and, the other side (receiver) can determine the data value by using this index and its value cache. Our experimental results using a set of fifteen benchmark codes from embedded systems domain show that power protocol is very effective in practice, and reduces the bit switching activity on the data bus by as much as 70.7% (with a value cache of 128 entries). We also present results from an implementation that combines our strategy with 1-to-2 encoding, a popular bus encoding strategy for low power. Our results indicate that this combined optimization strategy reduces bit switching activity by

67.8% on the average (across all benchmarks). These reductions in bit switching activity lead to more than 7% reduction on overall system energy on the average for a value cache of 256 entries. We also study the sensitivity of our savings to the value cache capacity and data cache capacity. [C1776]

"System level power-performance trade-offs in embedded systems using voltage and frequency scaling of off-chip buses and memory"

In embedded systems, off-chip buses and memory (i.e., L2 memory as opposed to the L1 memory which is usually on-chip cache) consume significant power often more than the processor itself. In this paper for the case of an embedded system with one processor chip and one memory chip, we propose frequency and voltage scaling of the off-chip buses and the memory chip and use a known micro-architectural enhancement called a store buffer to reduce the resulting impact on execution time. Our benchmarks show a system (processor + off-chip bus + off-chip memory) power savings of 28% to 36%, an energy savings of 13% to 35%, all while increasing the execution time in the range of 1% to 29%. Previous work in power-aware computing has focused on frequency and voltage scaling of the processors or selective power-down of sub-sets of off-chip memory chips. This paper quantitatively explores voltage/frequency scaling of off-chip buses and memory as a means of trading off performance for power/energy at the system level in embedded systems. [C1777]

"Strategies of energy saving in a wafer fab"

Energy saving on a semiconductor fab is a big issue from the cost reduction point of view. This paper summarizes some effective actions carried out in our fab. We found that lowering the temperature setting in the make-up air unit (MAU) outlet can save as much as NT$ 5.6 million per year. Adjusting the amount of exhaust of processing equipment to a reasonable level can also reduce large amounts of the running cost. Furthermore, adding heat recovery coils into a traditional MAU can reduce both cooling load and heating load. All the energy-saving actions can serve as valuable references to other semiconductor fabs. [C1778]

"Dynamic operand modification for reduced power multiplication"

We present and analyze a methodology to reduce power dissipation in binary multiplication. Our methodology is based on the observation that any n by n bit multiplication of two operands A and B can be expressed by a variety of products like e.g. A·B, B·A, (-A)·(-B), -((-A)·B), and so on, all specifying the same value, each of which being associated with a different energy consumption of the underlying multiplier computation. Given a first operand A and a second operand B, all modified operands of the product choices from the above have in common that they can easily be generated from A and B by conditional switching and complementation and that they can serve as inputs for a conventional binary multiplier with almost unchanged internal structure. We propose selection among the modified operand choices targeting reduced power dissipation within the multiplier. For the proposed operand selection schemes, the potential power savings is analyzed depending on the operand bit width n. [C1779]

"Scalable pipeline analog-to-digital converter for UTRA-TDD mobile station receiver"

A new reconfigurable pipeline ADC has been proposed for a mobile terminal receiver that can drastically reduce power dissipation dependent on adjacent channel interference. The proposed design automatically scales the word length by monitoring the in-band and out-of-band powers. The new ADC performance was evaluated in a simulation UTRA-TDD environment because of the large near far problem caused by adjacent channel interference from adjacent mobiles and base stations. Results show that the reconfigurable architecture (ADC) can save up to of 75% power dissipation when compared to a fixed word length ADC of 16 bits. This will prolong talk and standby time in a mobile terminal. [C1780]

"Energy impact of secure computation on a handheld device"

Computation offloading is an important approach to save the energy consumption while improving performance for wireless networked handheld devices. With such an approach, computational tasks are offloaded from the handheld device to a server, depending on the tradeoff between the communication cost and the computation cost. Adding security to the wireless network changes the relative cost of computation and communication. In this paper, we measure the energy consumption characteristics of multimedia applications on a handheld device, supported by computation offloading though a wireless LAN which is secured with IPsec. The measurement indicates that despite the overhead of the security mechanism, offloading remains quite effective as a method to reduce program execution time and energy consumption. [C1781]

"Reducing energy consumption by dynamic copying of instructions onto onchip memory"

The number of mobile embedded systems is increasing and all of them are limited in their uptime by their battery capacity. Several hardware changes have been introduced during the last years, but the steadily growing functionality still requires further energy reductions, e.g. through software optimizations. A significant amount of energy can be saved in the memory hierarchy where most of the energy is consumed. In this paper, a new software technique is presented which supports the use of an onchip scratchpad memory by dynamically copying program parts into it. The set of selected program parts are determined with an optimal algorithm using integer linear programming. Experimental results show a reduction of the energy consumption by nearly 30%, a performance increase by 25% against a common cache system and energy improvements against a static approach of up to 38%. [C1782]

"An optimal variable voltage scheduling"

With the development of mobile and portable devices, there is a strong need for reducing the energy in integrated circuit chips. Dynamic voltage scaling (DVS) techniques reduce energy consumption by changing the operating speed and voltage in real-time, based on the workload of the operation. In this paper, we address the optimal variable voltage scheduling problem for different workloads to save the maximum energy. Both static DVS and real-time DVS methods are investigated. [C1783]

"An adaptive low power texture mapping architecture"

The texture mapping stage is one of the most power consuming stages of the modern 3D graphics pipeline, due to its extensive computation and off-chip memory accesses. In this work, an adaptive texture mapping architecture is proposed, which achieves low-power by facilitating two types of data pattern sensitive transformations that reduce complexity of the computations. These transformations have been shown to achieve power savings in the range of 30% to 53% from the interpolation unit, the main power consumer of the texture mapping system. Systems with ability to obtain low power by tuning their supply voltages to the throughput requirements are gaining increasing prominence. Two more techniques namely adaptive datapath partitioning and dynamic voltage scaling based on the algorithm selected for texture mapping have been proposed for achieving significant power savings in these scenarios. These techniques can facilitate up to 79.5% and 59% power savings from the interpolation unit and the entire texture mapping system respectively. [C1784]

"A low-power reconfigurable digital pulse-shaping filter for an UTRA-TDD mobile terminal receiver"

A novel reconfigurable digital pulse-shaping filter has been proposed for a mobile terminal receiver that can drastically reduce power dissipation dependant on adjacent channel interference. It automatically scales the number of filter coefficients by monitoring the in-band and out-of-band powers. This new filter performance was evaluated in a simulation UTRA-TDD (UMTS terrestrial radio access-time division duplex) environment because of the large near far problem caused by adjacent channel interference from adjacent mobiles and base stations. The UTRA-TDD downlink mode was examined statistically and results show that this reconfigurable filter can save an average of 75% power dissipation when compared to a fixed filter length of 41. This will prolong talk and standby time in a mobile terminal. [C1785]

"Tracking and exploiting correlations in dense sensor networks"

In this paper, we propose a novel method for reducing energy consumption in a sensor network. It is important in a sensor network to minimize the energy usage of each sensor, because the nodes typically have finite battery life and if a node dies, this can lead to a loss of data or a network partition. As a result, several researchers have proposed various methods of routing and communication between nodes to reduce energy consumption. We propose an orthogonal approach to previous methods. In particular, we propose to exploit the inherent correlations that exist between sensor nodes by devising a novel algorithm that enables sensor nodes to compress their readings without knowing the exact measurements of the other nodes. Our simulations show that our algorithm used is promising as it leads to significant energy saving for various types of sensor nodes. [C1786]

"A mobility management scheme for reducing power consumption in IP-based wireless networks"

For data communication services gradually dominating in future wireless networks, one crucial problem is to save battery power of data terminals usually requiring much power. A mobility management scheme in IP-based wireless networks is proposed to reduce battery power consumption of mobile hosts. The proposed scheme manages six states: communicating, attention/cell-connected, attention/PA-connected, idle, off/attached, and detached states for efficient management of battery power, radio resources, and network load. Steady state probabilities for mobile host (MH) state transitions are derived using a semi-Markov process approach, and the power-saving effect of the proposed scheme is analyzed. The effects of various input parameters on the steady

state probabilities and power consumption are also investigated. The proposed mobility management scheme yields significant power saving in comparison with the current mobility management schemes for Mobile IP-based wireless networks. [C1787]

"Variable-rate pipelined multiplier design for reconfigurable DSP applications"

This paper presents a VLSI design and implementation of a variable-rate multiply-and-accumulate (MAC) block for DSP applications. The pipeline depth of the multiplier is dynamically controlled given the throughput requirement of the application. The depth of pipeline varies at the hardware level which controls the rate of execution to save power consumption. The MAC is targeted for a coarse grain FPGA design to support a wide range of digital signal processing applications. The power consumption is lowered by reducing the unnecessary register switching. The technique is applied to carry-save and Booth recoded multipliers. The MAC circuit is designed in 0.35-μm CMOS processing technology and evaluated for current DSP applications. [C1788]

"Combined dynamic voltage scaling and adaptive body biasing for lower power microprocessors under dynamic workloads"

Dynamic voltage scaling (DVS) reduces the power consumption of processors when peak performance is unnecessary. However, the achievable power saving by DVS alone is becoming limited as leakage power increases. In this paper, we show how the simultaneous use of adaptive body biasing (ABB) and DVS can be used to reduce power in high-performance processors. Analytical models of the leakage current, dynamic power, and frequency as functions of supply voltage and body bias are derived and verified with SPICE simulation. We then show how to determine the correct trade-off between supply voltage and body bias for a given clock frequency and duration of operation. The usefulness of our approach is evaluated on real workloads obtained using real-time monitoring of processor utilization for four applications. The results demonstrate that application of simultaneous DVS and ABB results in an average energy reduction of 48% over DVS alone. [C1789]

"Infrastructured ad hoc networks"

In traditional ad hoc networks, all nodes are considered equal and take equal part in the routing and forwarding of packets. We believe that this may not always be desirable. Rather, some nodes may be equipped with virtually unlimited power supplies, while others have to rely on battery power Thus, we propose the creation of "infrastructured" ad hoc networks by the deployment of pseudo base-stations (PBSs), which are nodes that have constant power supply (e.g., through a power outlet or a car battery), do not move, and are present just to act as routers and forward packets for other nodes, thus allowing the mobile nodes to save power The paper also presents ISAIAH, an ad hoc routing protocol based on the ad-hoc on-demand distance vector (AODV) routing protocol, which tries to select routes that go through PBSs instead of through mobile nodes to reduce the amount of power spent by these mobile nodes. Furthermore, it allows nodes to enter a power-saving mode, significantly reducing the power consumption compared to AODV. [C1790]

"STEM: Topology management for energy efficient sensor networks"

In wireless sensor networks, where energy efficiency is the key design challenge, the energy consumption is typically dominated by the node's communication subsystem. It can only be reduced significantly by transitioning the embedded radio to a sleep state, at which point the node essentially retracts from the network topology. Existing topology management schemes have focused on cleverly selecting which nodes can turn off their radio, without sacrificing the capacity of the network. We propose a new technique, called sparse topology and energy management (STEM), that dramatically improves the network lifetime by exploiting the fact that most of the time, the network is only sensing its environment waiting for an event to happen. By alleviating the restriction of network capacity preservation, we can trade off extensive energy savings for an increased latency to set up a multi-hop path. We will also show how STEM integrates efficiently with existing topology management techniques. [C1791]

"Gigahertz FPGAs with new power saving techniques and decoding logic"

The availability of SiGe HBT devices has opened the door for Gigahertz FPGAs. Speeds over 5 GHz have been reported However, to make the idea practical, serious power management and new architectural features have to be included, so that they can be scaled up significantly. This paper elaborates new ideas in designing high-speed SiGe BiCMOS FPGAs. The paper explains new methods to cut down the number of current trees in the circuit. Selective tree shutdown has been used to reduce power consumption. A new decoding logic has been developed where the address and data lines are shared These ideas have improved the performance of SiGe FPGAs. The operating frequency of the new Configurable. Logic Block (CLB) is 6.8 GHz. [C1792]

"Zero-power design for Smart Dust networks"

This paper addresses the low-power design of distributed sensor networks for intelligent measurement. We present a method for system clock optimization based on behavioural requirements and a power-saving mode. Essentially, the suggested approach minimizes the power consumption and provides longer battery lifetimes. In addition, the method improves the electromagnetic compatibility which is crucial for cubic-millimeter nodes. The zero-power theme goes on with passive reflector communication systems. We discuss an approach for zero-power orientation of corner-cube retroreflectors. [C1793]

"Power consumption and throughput in mobile ad hoc networks using directional antennas"

We present medium access control (MAC) protocols for mobile ad hoc networks that utilize directional antennas. The use of directional antennas in place of traditional omnidirectional antennas reduces interference and thereby improves the throughput performance of the network. An additional advantage of using directional antennas is due to its higher gain from its directivity, which can be utilized to reduce the transmission power during a directional transmission. In order to maximally utilize the savings in the average power consumption in the network, we propose a power control scheme that maintains a minimum transmission power level for effective transmission of packets using directional antennas. We present simulation results showing the throughput advantage and the savings in the average consumed power in the network using the proposed protocol. We also present results showing the maximum possible savings in power consumption in the same network when an ideal power control scheme is applied. [C1794]

"Power aware scheduling for AND/OR graphs in multiprocessor real-time systems"

Power aware computing has become popular recently and many techniques have been proposed to manage the energy consumption for traditional real-time applications. We have previously proposed (2001) two greedy slack sharing scheduling algorithms for such applications on multi-processor systems. In this paper, we are concerned mainly with real-time applications that have different execution paths consisting of different number of tasks. The AND/OR graph model is used to represent the application data dependence and control flow. The contribution of this paper is twofold. First, we extend our greedy slack sharing algorithm for traditional applications to deal with applications represented by AND/OR graphs. Then, using the statistical information about the applications, we propose a few variations of speculative scheduling algorithms that intend to save energy by reducing the number of speed changes (and thus the overhead) while ensuring that the applications meet the timing constraints. The performance of the algorithms is analyzed with respect to energy savings. The results obtained show that the greedy scheme is better than some speculative schemes and that the greedy scheme is good enough when a reasonable minimal speed exists in the system. [C1795]

"A source coding and modulation method for power saving and interference reduction in DS-CDMA sensor network systems"

A source coding and modulation technique for reducing multiple access interference (MAI) as well as for reducing power consumption in DS-CDMA wireless sensor network systems is presented. Source symbols are represented by a special coding, termed minimum energy coding (ME coding), which exploits redundant bits for saving power when transmitted via RF links with on-off-keying. Since energy is consumed mostly when high bits are transmitted, the ME coding represents source symbols with the least number of high bits, given an extended word length. When each channel uses the ME coding combined with a spreading code and OOK, fewer high bits are transmitted. It is shown that signal-to-noise ratio is significantly increased and that the error probability is lowered as well. First, the communication system architecture of this low MAI DS-CDMA is described, followed by the principle of interference reduction. Second, a signal model is obtained for the new source coding and transmission process. Third, guidelines for designing the length of codeword, the number of communication channels, and power efficiency are obtained. A RF sensor network system is designed. [C1796]

"Impact of network density on data aggregation in wireless sensor networks"

In-network data aggregation is essential for wireless sensor networks where energy resources are limited. In a previously proposed data dissemination scheme (directed diffusion with opportunistic aggregation), data is opportunistically aggregated at intermediate nodes on a low-latency tree. In this paper, we explore and evaluate greedy aggregation, a novel approach that adjusts aggregation points to increase the amount of path sharing, reducing energy consumption. Our preliminary results suggest that, under investigated scenarios, greedy aggregation can achieve up to 45% energy savings over opportunistic aggregation in high-density networks without adversely impacting latency or robustness. [C1797]

"Delay constrained energy efficient transmission strategies for wireless devices"

In this paper, we address the problem of energy efficient packet scheduling in a wireless environment. We consider a wireless transmitter which is limited by its finite battery resource. Our objective is to design a transmission schedule that maximizes battery lifetime subject to some delay constraints. To achieve this, we exploit two previously unconnected ideas: (i) channel coding can be used to conserve energy by transmitting at reduced power levels over longer durations; (ii) electro-chemical mechanisms in batteries allow them to recover energy during idle periods. While the first idea favors extending transmission durations, the second idea requires the transmitter to be idle to allow for recovery. Therefore, a strategy which is based entirely on either one or the other idea is not optimal. We provide a framework to merge these two ideas. We consider two kinds of delay constraints, one a deadline constraint and the other an average delay constraint and show that energy aware scheduling strategies for both these scenarios can result in significant energy savings. [C1798]

"Energy-efficient hybrid wakeup logic"

The instruction window is a critical component and a major energy consumer in out-of-order superscalar processors. An important source of energy consumption in the instruction window is the instruction wakeup: a completing instruction broadcasts its result register tag and an associative comparison is performed with all the entries in the window. This paper shows that a very large fraction of the completing instructions have to wake up no more than a single instruction currently in the window. Consequently, we propose to save energy by using indexing to only enable the comparator at the single instruction to wake up. Only in the rare case when more than one instruction needs to wake up, our scheme reverts to enabling all the comparators or a subset of them. For this reason, we call our scheme Hybrid. Overall, our scheme is very effective: for a processor with a 96-entry window, the number of comparisons performed by the average completing instruction with a destination register is reduced to 0.8. The exact magnitude of the energy savings will depend on the specific instruction window implementation. Furthermore, the application suffers no performance penalty. [C1799]

"Saving energy with just in time instruction delivery"

Just-In-Time instruction delivery is a general method for saving energy in a microprocessor by dynamically limiting the number of in-flight instructions. The goal is to save energy by (1) fetching valid instructions no sooner than necessary, avoiding cycles stalled in the pipeline-especially the issue queue, and (2) reducing the number of fetches and subsequent processing of mis-speculated instructions. A simple algorithm monitors performance and adjusts the maximum number of in-flight instructions at fairly long intervals, 100 K instructions in this study. The proposed JIT instruction delivery scheme provides the combined benefits of more targeted schemes proposed previously. With only a 3% performance degradation, energy savings in the fetch, decode pipe, and issue queue are 10%, 12%, and 40%, respectively. [C1800]

"A history-based I-cache for low-energy multimedia applications"

This paper proposes a history-based tag-comparison scheme for reducing energy consumption of direct-mapped instruction caches. The proposed cache efficiently exploits program-execution footprints recorded in the branch target buffer (BTB), and attempts to detect; and eliminate unnecessary tag checks at run time. Simulation results show that our approach can eliminate up to 95% of tag checks, saving the cache energy by 17%, while affecting the processor performance by only 0.2%. [C1801]

"Low power logical element for FPGA fabric"

Logical Element (LE) is the basic building block of FPGA fabric or any re-configurable computing machines. Logical Element basically consists of look-up tables according to A.B. Smith et al. (2000). This paper shows a low power LE. The low power is achieved by taking advantage of the commutative property of operations. This property will allow the data to be reorganized such that there will be separate paths for logic state 0 and logic state 1. The approach is targeted to reduce switching activity when possible. This paper shows 28% increase in power savings. [C1802]

"Power reduction via an MTCMOS implementation of MOS current mode logic"

In this paper, MOS current mode logic (MCML) is implemented in a multi-threshold CMOS technology. The design scheme allows the reduction of the minimum operational supply voltage, as well as the elimination of level shifters used. A high-speed 1:8 2.5 Gbit/s demultiplexer is used as a test vehicle. A 37% power saving is achieved. Furthermore, the impact of using the MTCMOS implementation over circuit parameters such as output impedance, current-matching-ratio, common-mode-rejection-ratio, gain, threshold voltage fluctuations and frequency response is investigated. This work is important for industry since the MTCMOS technique opens a

new alley for reducing power in MCML high-speed implementations while attaining the required data rates. [C1803]

"Predictive precharging for bitline leakage energy reduction [Cmicroprocessor caches]"

As technology scales down into deep-submicron, leakage energy is becoming a dominant source of energy consumption. Leakage energy is generally proportional to the area of a circuit, and caches constitute a large portion of the processor die area. Therefore, there has been much effort to reduce leakage energy in caches. Most techniques have been targeted at cell leakage energy optimization. Bitline leakage energy also is critical. Thus, we propose a predictive precharging scheme to reduce bitline leakage energy. Results show that energy savings are significant with little performance degradation. Also, our predictive precharging is more beneficial in more aggressively scaled technologies. [C1804]

"Synthesis of customized loop caches for core-based embedded systems"

Embedded system programs tend to spend much time in small loops. Introducing a very small loop cache into the instruction memory hierarchy has thus been shown to substantially reduce instruction fetch energy. However, loop caches come in many sizes and variations-using the configuration best on the average may actually result in worsened energy for a specific program. We therefore introduce a loop cache exploration tool that analyzes a particular program's profile, rapidly explores the possible configurations, and generates the configuration with the greatest power savings. We introduce a simulation-based approach and show the good energy savings that a customized loop cache yields. We also introduce a fast estimation-based approach that obtains nearly the same results in seconds rather than tens of minutes or hours. [C1805]

"Power conservation strategies for MEMS-based storage devices"

Power dissipation by storage systems in mobile computers accounts for a large percentage of the power consumed by the entire system. Reducing the power used by the storage device is crucial for reducing overall power consumption. A new class of secondary storage devices based on microelectromechanical systems (MEMS) promises to consume an order of magnitude less power with 10-20 times shorter latency and 10 times greater storage densities. We describe three strategies to reduce power consumption: aggressive spin-down; sequential request merging; sub-sector accesses. We show that aggressive spin-down can save up to 50% of the total energy consumed by the device at the cost of increased response time. Merging of sequential requests can save up to 18% of the servicing energy and reduce response time by about 20%. Transferring less data for small requests such as those for metadata can save 40% of the servicing energy. Finally, we show that by applying all three power management strategies simultaneously the total power consumption of MEMS-based storage devices can be reduced by about 54% with no impact on I/O performance. [C1806]

"Reducing the switching activity of modified SAFF flip-flop for low power applications"

The design and analysis of flip-flops is a critical issue in the design of high-performance and low power systems. In this paper, we propose a low power and a high-speed flip-flop (LP-SAFF) based on the Sense Amplifier Flip-Flop (SAFF). The saving in power consumption was achieved by reducing the switching activity at major internal nodes of the original SAFF. Our simulations show that this new flip-flop achieves major reduction in power consumption (25%-80%) and increases its performance by 5%-16%. [C1807]

"Using on-chip configurable logic to reduce embedded system software energy"

We examine the energy savings possible by re-mapping critical software loops from a microprocessor to configurable logic appearing on the same-chip in commodity chips now commercially available. That logic is typically intended to implement peripherals and coprocessors without increasing chip count-but we show that reduced software energy is an additional benefit, making such chips even more useful. We find critical software loops and re-implement them in the configurable logic such that a repeating software task completes sooner, allowing us to put the system in a low-power state for longer periods, thus reducing energy. We use simulations and estimations for a hypothetical device having a 32-bit MIPS processor plus configurable logic, yielding energy savings of 25%, increasing to 39% assuming voltage scaling. We physically measured several examples running on two commercial single-chip devices having an 8-bit 8051 microprocessor plus configurable logic and a 32-bit ARM microprocessor with configurable logic, with energy savings of 71% and 53% respectively, increasing to an estimated 89% and 75% assuming voltage scaling. [C1808]

"Integrating adaptive on-chip storage structures for reduced dynamic power"

Energy efficiency in microarchitectures has become a necessity. Significant dynamic energy savings can be

realized for adaptive storage structures such as caches, issue queues, and register files by disabling unnecessary storage resources. Prior studies have analyzed individual structures and their control. A common theme to these studies is exploration of the configuration space and use of system IPC as feedback to guide reconfiguration. However when multiple structures adapt in concert, the number of possible configurations increases dramatically, and assigning causal effects to IPC change becomes problematic. To overcome this issue, we introduce designs that are reconfigured solely on local behavior. We introduce a novel cache design that permits direct calculation of efficient configurations. For buffer and queue structures, limited histogramming permits precise resizing control. When applying these techniques we show energy savings of up to 70% on the individual structures, and savings averaging 30% overall for the portion of energy attributed to these structures with an average of 2.1% performance degradation. [C1809]

"Effective MAC state transition for the mobile station power saving in 3G mobile communication systems"

The control hold mode from cdma2000 1x systems has been adapted to the 1xEV-DV (evolution data and voice) systems because it has a lot of benefits such as power saving, reducing of overload and channel interferences, etc. However d1xEV-DV system does not fully capture the benefits from control hold mode, because the MS has to do continuous monitoring the F-PDCCH indicating whether the BS sends packet data or not. That is, the MS has to do monitoring the F-PDCCH (forward packet data control channel) continuously to capture the MAC ID while in control hold mode like as an operation in active mode. This continuous monitoring of the F-PDCCH causes higher power consumption and gives an overload to the decoder block at the MS side. In this paper to resolve these problems, we propose a new channel, F-WUCH (forward wake-up channel), to maximize the power saving of the MS, to minimize the interferences and to reduce the overhead from the continuous monitoring of the F-PDCCH in the control hold mode. [C1810]

"Design for low-power, low-cost, and high-reliability precomputation-based content-addressable memory"

This paper presents a novel VLSI architecture for a fully parallel precomputation-based content addressable memory (PB-CAM) with low-power, low-cost, low-voltage, and high-reliability features. This design is based on a precomputation skill that saves not only power consumption of the PB-CAM system, but also reduces transistor count and operating voltage of the PB-CAM cell. In addition, the proposed CAM word structure adopts a static pseudo nMOS circuit design to improve system reliability. The whole design was fabricated with the TSMC 0.35 μm SPQM CMOS process parameters under 3.3 V supply voltage. With a 128 words by 30 bits CAM size, the measurement results indicate that the proposed circuit works up to 100 MHz with a power consumption of less than 33 mW. Furthermore, the low voltage measurement results show that the proposed circuit works up to 30 MHz under 1.5 V supply voltage. [C1811]

"Multiplier energy reduction through bypassing of partial products"

The design of portable battery operated multimedia devices requires energy-efficient multiplication circuits. This paper presents a novel approach to reduce power consumption of digital multiplier based on dynamic bypassing of partial products. The bypassing elements incorporated into the multiplier hardware eliminate redundant signal transitions, which appear within the carry-save adders when the partial product is zero. Simulations on the real-life DCT data show that the proposed approach can improve power saving of related methods by 12%, while jointly with them, it reduces the power consumption of a 16Ч16 digital CMOS multiplier by 31%, with 25% area overhead and less than 4% performance degradation in the worst case. The circuit implementation is outlined. [C1812]

"Combining dual-supply, dual-threshold and transistor sizing for power reduction"

Multiple supply voltages, multiple transistor thresholds and transistor sizing could be used to reduce the power dissipation of digital blocks. This paper presents a framework for evaluating the effectiveness of each of these approaches independently and in conjunction with each other. Results show the advantages of multiple supply, transistor sizing, and multiple threshold can be compounded to maximize power reduction. The order of application of these techniques determines the final savings in active and leakage power. [C1813]

"Exact and heuristic algorithms for low-energy code compression in performance and memory constrained embedded systems"

Code compression has proved to be a viable solution to the problem of minimizing energy in core-based embedded systems. Normally, energy reduction is achieved by limiting the dynamic size of the program being

executed. However, an increase of static code size is often observed as a result of compression, and this effect may not be acceptable in memory-constrained systems. Furthermore, nonnegligible hardware overhead may be needed to implement compression schemes that guarantee high dynamic size reduction, thus introducing potential performance penalties (on-the-fly instruction decompression during program execution may be slow). In this paper, we present exact and heuristic compression algorithms that reduce energy consumption under tight code size and decompressor complexity constraints. The proposed solutions are basic block oriented; they guarantee that static code size never increases with respect to the original, uncompressed code, and allow us to finely trade energy reduction for decompressor complexity. The achieved energy savings, evaluated on a number of benchmarks, range from 48% to 54%, depending on the technology used for code memory realization (on-chip ROM vs. off-chip flash) [C1814]

"Reduced precision redundancy for low-power digital filtering"

We propose a low-power digital filtering technique based on voltage overscaling (VOS) and a novel algorithmic noise-tolerant (ANT) technique referred to as reduced precision redundancy (RPR). VOS implies scaling of the supply voltage beyond the critical voltage required for correct operation. RPR involves having a reduced precision replica whose output can be employed as the final output in case the original filter computes erroneously. In addition, an LSB estimator is also employed to compensate for information loss in the LSBs. For frequency selective filtering, it is shown that the proposed technique provides 30% energy savings over an optimally scaled (i.e., the supply voltage equals the critical voltage) present day system. Energy savings of up to 65% can be achieved if a SNR loss of 1.5 dB is tolerated [C1815]

"Sign extension reduction by propagated-carry selection"

To reduce the area and power consumption in constant coefficient multiplications, the coefficient can be encoded using the canonic signed digit (CSD) representation. When the partial product terms are added depending on the nonzero bit positions in the CSD-encoded multiplier, all sign bits are properly extended before the addition takes place. In this paper, to reduce the overhead due to sign extension, a new method is proposed based on the fact that carry propagation in the sign-extension part can be controlled such that a desired input bit can be propagated as a carry. Also, a fixed-width multiplier design method suitable for CSD multiplications is proposed. By combining these two methods, it is shown that significant hardware saving can be achieved [C1816]

"Procedure call duplication: minimization of energy consumption with constrained error detection latency"

This paper presents a new software technique for detecting transient hardware errors. The objective is to guarantee data integrity in the presence of transient errors and to minimize energy consumption at the same time. Basically, we duplicate computations and compare their results to detect errors. There are three choices for duplicate computations: (1) duplicating every statement in the program and comparing their results, (2) re-executing procedures with duplicated procedure calls and comparing the results, (3) re-executing the whole program and comparing the final results. Our technique is the combination of (1) and (2): Given a program, our technique analyzes procedure call behavior of the program and determines which procedures should have duplicated statements (choice (1)) and which procedure calls should be duplicated (choice (2)) to minimize energy consumption while controlling error detection latency constraints. Then, our technique transforms the original program into the program that is able to detect errors with reduced energy consumption by re-executing the statements or procedures. In benchmark program simulation, we found that our technique saves over 25% of the required energy on average compared to previous techniques that do not take energy consumption into consideration [C1817]

"Improving memory energy using access pattern classification"

In this paper, we propose a data-driven strategy to optimize the memory energy consumption in a banked memory system. Our compiler-based strategy modifies the original execution order of loop iterations in array-dominated applications to increase the length of the time period(s) in which memory banks axe idle (i.e., not accessed by any loop iteration). To achieve this it first classifies loop iterations according to their bank access patterns and then, with the help of a polyhedral tool, tries to bring the iterations with similar bank access patterns close together. Increasing the idle periods of memory banks brings two major benefits; first, it allows us to place more memory banks into low-power operating modes, and second, it enables us to use a more aggressive (i.e., more energy saving) operating mode for a given bank. Our strategy has been evaluated using seven array-dominated applications on both a cacheless system and a system with cache memory. Our results indicate that the strategy is very successful in reducing the memory system energy, and improves the memory energy by as much as 34% on the average [C1818]

"Decrease power consumption using a programmable logic device"

This paper describes system design techniques using a low power CoolRunnerTMCPLD to reduce overall system power consumption. Utilizing a CoolRunner CPLD to off-load operations from the system microprocessor keeps the processor in a power saving mode longer and contributes to significant power savings [C1819]

"On signal-gating schemes for low-power adders"

Signal gating schemes for low-power adder design are studied in this paper. Signal gating dynamically deactivates portions of an adder according to the actual precision of two operands. Based on program analysis, signal gating is developed for two different adders: symmetric adders and asymmetric adders. The effect of signal gating is investigated by incorporating several gating schemes into a RISC pipeline. Experimental results indicate more power saving compared to previous work [C1820]

"Cool-cache for hot multimedia"

We claim that the unique characteristics of multimedia applications dictate media-sensitive architectural and compiler approaches to reduce the power consumption of the data cache. Our motivation is exploring energy savings for real-time multimedia workloads without sacrificing performance. In this paper, we present two complementary media-sensitive energy-saving techniques that leverage static information. While our first technique is applicable to existing architectures, in our second technique we adopt a more radical approach and propose a new caching architecture by re-evaluating the architecture-compiler interface. Our experiments show that substantial energy savings are possible in the data cache. Across a wide range of cache and architectural configurations we obtain up to 77% energy savings, while the performance varies from 14% improvement to 4% degradation depending on the application. [C1821]

"Reducing environmental problems caused by domestic water consumption"

TOTO developed "Cefiontect Technology: the technology of preventing the dirt suitable for the toilet bowl etc.", and "HYDOROTECT Technology: the technology of preventing the dirt adapting the photocatalyst reaction." By using such technology, the number of times of cleaning is reduced,, detergent is cut down, and it can reduce the water consumption for cleaning. Furthermore, the air can also be purified. Here, the outline and effect of each technology are reported. Moreover, TOTO offers an impressive line-up of water-saving and power-saving type equipment. Great water saving can be performed by combining water-saving type equipment. Simultaneously, discharge of carbon dioxide is greatly reducible. Here, the environmental-preservation effect and economical effect of using a water-saving instrument in a residence are reported [C1822]

"Development of environmentally friendly energy-efficient copier"

Offering the ease of operation that enables instantaneous copier use, while at the same time reducing sleep energy consumption, is a major research topic. In 1998, the IEA proposed the IEA/DSM "Copier of the Future" program to attain this goal. The specifications of this program were exceedingly strict: sleep power consumption was to be reduced to at most 1/10 that of current copiers of the same class. Ricoh joined this program, and in 1999 became the first in the world to pass the program specifications. Ricoh then began sales of the imagio Neo 350 (overseas model: Aficio1035), incorporating this energy-saving technology, in February 2001. The imagio Neo 350, a mid-high speed copier capable of 35 copies per minute, consumes no more than 7W in sleep mode, and recovers from sleep mode within 10 seconds. This technology consists of the following three basic technologies, all developed by Ricoh: (1) an energy-efficient fusing unit; (2) control of fusing temperature using twin heater; (3) low-temperature fusing toner. This allowed Ricoh to offer a revolutionary environmentally friendly digital multi-functional copier with four times the energy efficiency of its predecessors [C1823]

"Saving energy with architectural and frequency adaptations for multimedia applications"

General-purpose processors are expected to be increasingly employed for multimedia workloads on systems where reducing energy consumption is an important goal. Researchers have proposed the use of two forms of hardware adaptation-architectural adaptation and dynamic voltage (and frequency) scaling or DVS-to reduce energy. This paper develops and evaluates an integrated algorithm to control both architectural adaptation and DVS targeted to multimedia applications. It also examines the interaction between the two forms of adaptation, identifying when each will perform better in isolation and when the addition of architectural adaptation will benefit DVS. Our adaptation control algorithm is effective in saving energy and exploits most of the available potential. For the applications and systems studied, DVS is consistently better than architectural adaptation in isolation. The addition of architectural adaptation to DVS benefits some applications, but not all. Finally, in a seemingly counter-intuitive result, we find that while less aggressive architectures reduce energy for fixed frequency

hardware, with DVS, more aggressive architectures are often more energy efficient. [C1824]

"Scheduling with dynamic voltage/speed adjustment using slack reclamation in multi-processor real-time systems"

The power consumption of modern high-performance processors is becoming a major concern because it leads to increased heat dissipation and decreased reliability. While many techniques have been proposed to reduce power consumption for uni-processors, there has been considerably less work on multi-processor systems. In this paper we focus on power-aware scheduling for multi-processor real-time systems. Based on the idea of slack sharing among processors, we propose two novel scheduling algorithms for task sets with and without precedence constraints. These scheduling techniques reclaim the time unused by a task to reduce the execution speed of future tasks, and thus reduce the total energy consumption of the system. Simulation results indicate that our algorithms achieve up to 60% energy savings on multi-processor systems with variable voltage processors. [C1825]

"Memory energy characterization and optimization for the SPEC2000 benchmarks"

With an increasing focus on low power computing devices such as PDA's, energy has become an important criterion for optimization. Power mode control of memory devices has the potential to significantly reduce energy consumption, for a moderate increase in execution time. Prior studies have explored the benefits of many schemes for DRAM power mode control. In this work, we present a framework for estimating the optimal energy savings that can be obtained under various constraints. We also analyze the memory energy consumption patterns of a set of benchmarks drawn from the SPEC2000 suite and establish that energy consumed during power mode transitions is a significant component of DRAM energy. We characterize the memory access behavior of these benchmarks by studying their inter access times. Based on our analysis, we revisit existing mode control schemes and fine tune their performance. In particular we propose a history based mode control policy, which performs better than the existing schemes in most cases. [C1826]

"Direct addressed caches for reduced power consumption"

A direct addressed cache is a hardware-software design for an energy-efficient microprocessor data cache. Direct addressing allows software to access cache data without a hardware cache tag check. These tag-unchecked loads and stores save the energy of a tag check when the compiler can guarantee an access will be to the same line as an earlier access. We have added support for tag-unchecked loads and stores to C and Java compilers. For Mediabench C programs, the compiler eliminates 16-76% of data cache tag accesses, with half of the benchmarks avoiding over 40% of the data tag checks. For SPECjvm98 Java programs, the compiler eliminates 18-63% of data cache tag checks. These tag check reductions translate into data cache energy savings of 9-40%, and overall processor and cache energy savings of 2-8%. [C1827]

"A novel architecture for low-power design of parallel multipliers"

In this paper, a new architecture for low-power design of parallel multipliers is proposed. Reduction of power consumption is achieved by reducing the circuit activity at the architecture level by dividing the multiplication circuit into clusters of smaller multipliers. By applying clock gating techniques and preprocessing operations on the input pattern using simple logic functions, some of these clusters that are producing a zero result can be disabled and hence saving the switching power component that could be consumed by these clusters. The amount of power savings is dependent on the nature of the input pattern, which varies according to the application. Analysis of the input pattern is performed. For testing purposes, A 8-bit multiplier prototype is constructed in 0.35 micron double metal CMOS technology using Cadence development tools. For the average case when all the input combinations have an equal probability of occurrence, HSPICE simulation results at 3.3 V and 500 MHz frequency show that the proposed architecture results in 13.4% power savings [C1828]

"Test scheduling for minimal energy consumption under power constraints"

Power consumption has become a crucial concern in built-in self-test (BIST) due to the increased switching activity in the circuit under test. In this paper we present a method for scheduling tests which aims at minimizing total energy consumption and test application time under peak power constraints. In contrast to previous approaches, our method takes into account switching activity which occurs in overlapping regions of the subcircuits under test. The key part is a hierarchical approach to power estimation which makes it possible to quickly evaluate the power consumption of partial schedules. Experimental results show that the energy savings range between 54% and 97% in comparison with conventional methods. Test application time can be reduced to the same extent [C1829]

"Candidate scheme for MP-MLQ search in G723.1"

For the purpose of low cost or low power consumption, a cost-effective solution with good trade-off between quality and complexity must be estimated for a small mobile device. We propose a condensed MP-MLQ algorithm to reduce the search computation required for G723.1. Simulation results show that the proposed method can reduce about 50~82% the computational load for stochastic codebook search with perceptually intangible degradation. This reduction would be helpful to save power consumption and relax the CPU load for a mobile device in wireless communication, e.g., PALM, PDA [C1830]

"A high-performance low-power static differential double edge-triggered flip-flop"

A new static differential double edge-triggered flip-flop is proposed. In order to ensure the double edge triggering operation, a narrow pulse is generated after each clocking edge, by means of clock racing. Compared to existing double edge-triggered flip-flops, the presented circuit configuration presents improved delay characteristics, reduced power consumption, while keeps the total transistor count low. Further power and transistor savings can be achieved by applying the narrow pulse to more than one similar adjacent DET flip-flops [C1831]

"A low-power reduced swing single clock flip-flop"

A reduced swing single clock flip-flop (RS2CFF) is developed to reduce power consumption significantly compared to conventional FFs. RS2CFF avoids unnecessary internal node transition and reduce fighting currents. The overall power saving in flip-flop operation is estimated to be 33% with additional 64% power savings in clock network [C1832]

"Energy locality: processing/communication/interface tradeoffs to optimize energy in mobile systems"

Summary form only given, as follows. As computers continue to shrink, research and commercial interest in mobile/wearable computing is rapidly growing. Unlike traditional desktop computing in which the user is required to come to the computer, mobile computing brings the computer to the user. Mobile/wearable computers represent the next evolutionary step in the trend toward more people-centric computing. One of the key problems with mobile/wearable computing is energy consumption. Battery weight for mobile/wearable computers often exceeds the weight of all other components combined. In order to make mobile/wearable computing widely applicable, major advances in reducing power consumption and battery weight are needed. While a “Moore's Law” exists for power consumption of microprocessors with mW/MIPS decreasing by a factor of ten every five year, there is no such similar trend in wireless communications. This suggests that future wearable computers will be communications bound. In fact, we estimate that nearly 80% of the power consumed by wearable computers can be due to communications. Trading off energy expensive communication for energy cheap computation through effective partitioning of control and data can result in significant energy savings. Examples and measurements will illustrate how the use of proxies can reduce power consumption due to communications by several orders of magnitude. In addition, the interface design must be carefully matched with user tasks and balanced against energy consumption. Many complex and interrelated issues determine the balance between ease-of-use and power consumption. Simply trading off ease-of-use for lower per operation power consumption may result in higher task energy consumption due to the increase in the number of operations needed to traverse a less intuitive interface. The effect of user interface on energy consumption can be evaluated by developing several different interfaces and measuring and comparing the ease-of-use and energy consumption. In conclusion, an architecture that supports these studies will be introduced. The Spot wearable computer includes a dozen power monitors that can be read under software control to determine which subsystems are active and their power consumption during an application [C1833]

"A low-swing clock double-edge triggered flip-flop"

A low-swing clock double-edge triggered flip-flop (LSDBF) is developed to reduce power consumption significantly compared to conventional FFs. LSDFF avoids unnecessary internal node transition and reduces conflicting currents. The overall power saving in flip-flop operation is estimated to be 30.2 to 50.8% with additional 78% power savings in a clock network [C1834]

"Environment friendly revolution in home appliances"

In home appliances, electrical energy is optimally controlled by using power electronics technology, creating a comfortable environment in terms of energy saving, low sound generation, and reduced time consumption. At present, this technology has been expanding the range of its applications and leading environment friendly revolution in home appliances. This paper describes an ultra low-noise washing machine with direct drive motor,

an energy saving inverter refrigerator with twin-evaporator, a high efficiency microwave oven, a high output power induction heating rice cooker, and a twin-burner induction heating range [C1835]

"Dynamic voltage scaling on MPEG decoding"

A number of research efforts have been devoted to reduce energy consumption of a processor without impacting the performance through the use of dynamic voltage scaling (DVS). The paper presents two DVS algorithms on MPEG decoding. One is DVS with delay and drop rate minimizing algorithm (DVS-DM) where voltage is determined based on previous workload only. Another algorithm scales the supply voltage according to the predicted MPEG decoding time and previous workload (DVS with predicted decoding time or DVS-PD). Simulation results show that DVS-PD improves energy efficiency as much as 56% compared to the conventional shutdown algorithm. We also found that the amount of energy saving with DVS-PD is not affected by the fluctuation of the movie stream, but is related to the error rate of the predictor, which implies that if decoding time is predicted more accurately, the DVS algorithm can be more efficient [C1836]

"Power efficient inter-module communication for digit-serial DSP architectures in deep-submicron technology"

This paper investigates the use of quaternary current mode signaling to minimize the power dissipation associated with inter-module communication. We formulate a condition specifying when the insertion of the encode-decoder pair between the two modules results in a reduction of the overall power consumption of the system. An algorithm LIBCOM is developed which utilizes this condition to insert the encoder-decoder pair between the two modules only if it is advantageous. The HSPICE results obtained for 0.35 μm CMOS process show that LIBCOM can reduce the power consumption by 15%. As technology scales down, the power saved by our algorithm can be several orders of magnitude higher [C1837]

"Influence of array allocation mechanisms on memory system energy"

Portability and energy consumption have become increasingly important in mobile computing. Consequently, there is a clear need for energy-aware portable software design. This paper brings these two design considerations together by examining and optimizing the energy consumption of array allocation mechanisms in Java. Specifically, using a set of array-dominated benchmarks and a partitioned memory architecture with multiple low-power operating modes, we study two data optimization techniques: memory layout modification and array-interleaving. Our results show that these optimizations increase the effectiveness of energy savings due to power control of partitioned memory architectures across different memory configurations. It is observed that the memory energy can be significantly reduced using these techniques [C1838]

"Efficient data dissemination to mobile clients in e-commerce applications"

Mobile commerce is the next growing area in electronic commerce and mobile computing. These are sophisticated, data-intensive mobile applications whose success depends strongly on the efficiency by which data are disseminated to a large number of mobile users. Different techniques have been put forward, of which the most promising are the push-based techniques that explore the asymmetry in wireless communications and the reduced energy consumption of the receiving mode on mobile devices. This paper proposes a new broadcast indexing scheme, termed “constant-size I-node distributed indexing” (CI), that offers more energy savings in practical applications. Our detailed simulation results indicate that CI, which is a variant of the currently best-performing distributed indexing scheme, outperforms the latter for broadcast sizes of 12,000 or fewer data items, reducing the access time by up to 25% and the tuning time by up to 15% [C1839]

"Direct control of residential water heater loads to reduce power system distribution losses"

This paper presents a new method to reduce the real power losses and increase the associated dollar savings in electric power distribution systems. The method is based on the direct control and management of the power and energy consumption of residential water heaters. The objective function includes, among others, the cost of real power losses, the cost of the annual energy losses, and the cost associated with purchasing and installing additional water heating storage capacity at customer locations. Using a number of constraints, the objective function is solved and the optimal number and location of water heaters on a distribution feeder are determined. Through this procedure, the total system costs are minimized and the dollar savings are maximized. Details of the optimization procedure and some practical results are presented [C1840]

"Low power order based DCT processing algorithm"

This paper presents an algorithm and an associated architecture for the low power implementation of the

Discrete Cosine Transform. The algorithm reduces power by manipulating bit-correlation between successive cosine coefficients applied to the input of the Multiply-Accumulate section such that the effective switched capacitance is reduced. This reduces the switching activity in the Discrete Cosine Transform processor. The paper describes the algorithm and the proposed architecture. The evaluation procedure is also presented including the results from a number of example images illustrating up-to 29%, power savings [C1841]

"Signal activity and power consumption reduction using the logarithmic number system"

In this paper, the logarithmic number system (LNS) is exploited to save power. The equivalence of an LNS to a linear fixed-point system is initially explored and a related theorem is introduced. Then, activity is studied for both uniform, and Gaussian correlated input distributions. LNS is shown to reduce the average bit assertion probability by more than 60%, in certain cases, over an equivalent linear representation. The impact of LNS to power dissipation through architecture simplification is also discussed [C1842]

"A low power SOI adder using reduced-swing charge recycling circuits"

Power reduction is a critical requirement in modern VLSI design due to increasing operating frequencies and circuit densities, and the emergence of portable applications. Decreasing the supply voltage, VDD, is the easiest way to reduce power consumption in CMOS circuits because switching power is proportional to VDD2 for rail-to-rail logic swing. However, reducing VDDdegrades circuit speed due to the super-linear reduction of transistor current. Lowering transistor threshold voltage, Vth, helps to recover this speed degradation; however sub-threshold leakage current increases exponentially with decreasing Vth, resulting in battery-draining quiescent power consumption with Vthless than about 300 mV. Circuit techniques are needed to achieve lower power consumption without speed degradation. The low-power CMOS SOI circuit configuration reported here, low-swing charge recycling (LSCR), uses differential pass-transistor logic, a low voltage swing, and charge recycling to save power [C1843]

"Reducing cache energy through dual voltage supply"

Due to a large capacitance and enormous access rate, caches dissipate about a third of the total energy consumed by today's processors. In this paper we present a new architectural technique to reduce energy consumption in caches. Unlike previous approaches, which have focused on lowering cache capacitance and the number of accesses, our method exploits a new freedom in cache design, namely the voltage per access. Since in modern caches, the loading capacitance operated on cache-hit is much less than the capacitance operated on cache-miss, the given clock cycle time is inefficiently exploited during the hit. We propose to trade-off this unused time with the supply voltage, lowering the voltage level on the hit and increasing it during the miss. Experiments shows that the approach can save up to 60% of cache energy without large performance and area overhead [C1844]

"Memory hierarchy optimization of multimedia applications on programmable embedded cores"

Data memory hierarchy optimization and partitioning for a widely used multimedia application kernel known as the hierarchical motion estimation algorithm is undertaken, with the use of global loop and data-reuse transformations for three different embedded processor architecture models. Exhaustive exploration of the obtained results clarifies the effect of the transformations on power, area, and performance and also indicates a relation between the complexity of the application and the power savings obtained by this strategy. Furthermore, the significant contribution of the instruction memory even after the application of performance optimizations to the total power budget becomes evident and a methodology is introduced in order to reduce this component [C1845]

"An improved time-recursive lattice structure for low-latency IFFT architecture in DMT transmitter"

In this paper, we propose an improved parallel lattice structure to implement IFFT module in the transmitter of Discrete Multitone (DMT) system. By exploiting the symmetric/anti-symmetric properties of the input symbols, we add a new pre-processing scheme to previous work. By doing so, the iteration number can be halved from 2N to N (N is 256 in DMT). As a result, the clock rate of the IFFT lattice module can be lowered under the same input symbol rate. In addition, the internal registers are also reduced from 4N-4 to 2N-2, and multiplexers in post-processing circuits are all eliminated compared with the previous design. Hence, the proposed method can save more power consumption and further reduce the hardware complexity of the IFFT module. The proposed architecture is regular, modular, and free of global routing. Thus, it is very suitable for VLSI implementation [C1846]

"Enhanced low power motion estimation VLSI architectures for video compression"

Power consumption is very critical for portable video applications. During compression, the largest portion of power is consumed in the Motion Estimation part, which requires a huge amount of computation. This paper presents an architectural enhancement to reduce the power consumption during full-search block-matching (FSBM) motion estimation without sacrificing throughput or optimality. The proposed approach achieves these power savings by disabling portions of the architecture that perform unnecessary computations. A comparison between our enhancement and others is presented based on simulation and analytical analysis. Different benchmarks are used to test and compare the discussed architectures. Analytical and simulation results show the effectiveness of the enhancements [C1847]

"A low power charge-recycling ROM architecture"

A new low power charge recycling ROM (CR-ROM) architecture is proposed. The CR-ROM uses charge-recycling method in bit lines of ROM to save the power consumption. About 90% of the total power used in the ROM is consumed in bit lines. With the proposed method, power consumption in ROM bit lines can be reduced asymptotically to zero if the number of bit lines is infinite and the sense amplifiers detect infinitely small voltage difference. However, the real sense amplifiers cannot sense very small voltage difference. Therefore, reduction of power consumption is limited. The simulation results show that the CR-ROM only consumes 13%~78% of the conventional low power contact programming mask ROM [C1848]

"Arithmetic transformations for increased maximal sample rate of bit-parallel bireciprocal lattice wave digital filters"

In this paper we propose an arithmetic transformation of first-order allpass lattice wave digital filter sections implemented with bit-parallel, carry-save arithmetic which increases the maximum sample rate. Such filter sections are the critical component of bireciprocal lattice wave digital filters which are efficient filter structures for sample rate conversion with factors of two. The proposed transformation reduces the sample period bound by up to 33% for CSDC coefficients. This is obtained with a coefficient with four nonzero bits, and, dependent on the value of the adaptor coefficient, at the expense of up to 28% more carry-save adders. An example is presented where an adaptor with a coefficient with two nonzero bits is implemented. This results in a reduction of the sample period bound with 25% with a 14% increase of the number of carry-save adders needed [C1849]

"Minimizing gate capacitances with transistor sizing"

In this paper a method for choosing appropriate transistor topology for use with transistor sizing is presented. In combinatorial blocks of static CMOS circuits transistor sizing can be applied for delay balancing in order to guarantee synchronously arriving signal slopes at the input of logic gates. Since the delay of a logic gate depends directly on transistor sizes, the variation of channel-widths and -lengths (W and L) allows one to equalize different path delays without influencing the total propagation delay of the circuit. Thus, glitching can be avoided. To achieve optimal results, transistor lengths have to be increased, which results in both increased gate capacitances and area. Splitting the long transistors counteracts this negative influence and reduces the power dissipated. A program, GliMATS, for automated circuit optimization has been implemented. Experimental results show that significant power savings can be achieved with this method [C1850]

"A low power survivor memory unit for sequential Viterbi-Decoders"

This paper introduces an innovative, low-power algorithm for survivor memory units (SMU) in Sequential Viterbi-Decoders (VD), called “Path-Metric Controlled Decision Save” (PCDS). Based on the fact that theoretically only the decisions of the survivor states are necessary for decoding, one can neglect all the other decisions from non-survivor states, i.e. we do not have to save them in the survivor memory and hence reduce power consumption significantly. The only problem is to derive a criterion which distinguishes between the essential and negligible decisions. It will be investigated and proven that the performance loss introduced by the PCDS algorithm is confidently negligible for all SNR and that the PCDS algorithm is self-adaptive in terms of performance. Furthermore, it will be illustrated that, for state of the art VD. e.g. HDSL2 or SDSL, the power reduction exceeds 90% whereas the area-overhead for this algorithm is a comparator and hence negligible [C1851]

"An optimal power saving scheme for mobile handsets"

Power saving is an important issue for mobile handsets since they must rely on their batteries. To reduce the battery consumption of mobile handsets, we propose a fractional threshold-based wake-up mechanism, which switches the system into the sleep mode when the packet-receiving queue is empty, and switches the system

on when the number of packets in the queue “reaches” a fractional threshold value. A fractional threshold value can be any real number, instead of just a natural number. In fact, the fractional threshold value indicates the mean threshold value. Our study indicates that the fractional threshold scheme with probability 1 provides an optimal power saving solution. The optimization objective is to minimize switch-on rate while satisfying the quality of service requirement, which is an upper bound of the packet dropping probability [C1852]

"Compiler-directed dynamic voltage/frequency scheduling for energy reduction in microprocessors"

Dynamic voltage and frequency scaling of the CPU has been identified as one of the most effective ways to reduce energy consumption of a program. This paper discusses a compilation strategy that identifies scaling opportunities without significant overall performance penalty. Simulation results show CPU energy savings of 3.97%-23.75% for the SPECfp95 benchmark suite with a performance penalty of at most 2.53% [C1853]

"Reducing routing table size using ternary-CAM"

Ternary Content Addressable Memory (TCAM) has increasingly been used in high speed routers to perform routing lookup function. They allow simultaneous comparison of the key with every index at the same time so that the longest matched prefix could be selected within one memory access, much faster than software based search algorithms. We propose two techniques to compact routing table stored in TCAM. The techniques allow a smaller TCAM to be used to reduce cost, power consumption and thermal dissipation. They could also help routers to scale to larger routing table. Our simulation shows up to 48% size reduction. Fast incremental update algorithm is presented to maintain space saving without recomputing the compacted table after each routing update [C1854]

"Design of an adjustable-way set-associative cache"

The trade-off between direct-mapped caches and set-associative caches is an important issue in the research on the performance of caches. The conventional set-associative caches with higher associativity provide lower miss rate, however, they suffer from longer hit access time and larger energy consumption. Based on the consideration of different program localities, the different programs should select the caches with the appropriate associativity. In this paper, we propose a set-associative cache that can provide the flexibility to adjust its associativity according to the different program behaviors, which means that the proposed cache scheme can be adjusted from n-way set-associative cache to direct-mapped cache. By this cache architecture, the power consumption will be saved when an n-way set-associative cache configures as the cache with lower associativity (less than n) due to only enabling the fewer subarrays of the tag memory and the data memory. However, the performance is also maintained as the conventional set-associative cache or the direct-mapped cache. In the future, the adjustable-way set-associative cache can be applied to the multiprocessor system to reduce the average energy consumption of the overall system [C1855]

"Energy-efficient load and store reuse"

A load and store reuse mechanism can be used for filtering memory references to reduce memory activity including on-chip cache activity. The challenging aspect of this task is to ensure that energy savings achieved in memory are not offset by energy used by the reuse hardware. In this paper we present the design of a reuse mechanism which has been carefully tuned to achieve net energy savings. In contrast to traditional filter cache designs which trade-off energy reductions with higher execution times, our approach reduces both energy and execution time [C1856]

"Compiler support for block buffering"

On-chip caches consume a significant fraction of energy in current microprocessors. Hence, hardware techniques such as block buffering have been developed and shown to be effective in reducing on-chip cache energy consumption. We are not aware of any software solutions to exploit block buffering. This paper presents a compiler-based approach that modifies both code and variable layout to effectively exploit block buffering, and is aimed at the class of embedded codes that make heavy use of scalar variables. Unlike previous work that uses only storage pattern optimization, our solution integrates both code restructuring and storage pattern optimization. Experimental results on a set of complete programs demonstrate that our solution leads to significant energy savings [C1857]

"Selectively clocked skewed logic (SCSL): a robust low-power logic style for high-performance applications"

In very high performance designs, dynamic circuits, such as domino logic, are used because of their high speed.

Skewed logic circuits can be used to achieve designs having performance comparable to that of domino but with better scalability. Moreover, a selective clocking scheme may be applied to enhance the power savings for skewed logic circuits. This paper proposes Selectively Clocked Skewed Logic (SCSL), a new circuit style based on skewed logic aiming for low clock power consumption. The results on ISCAS benchmark circuits implemented with this circuit design style show that the total power consumption can be reduced by 52.05% when compared to that of domino circuit with comparable performance [C1858]

"Power quality issues in a hybrid power system"

We analyzed a power system network, which consisted of two types of power generation: wind turbine generation and diesel generation. The power quality and the interaction of diesel generation, the wind turbine, and the local load were the subjects of investigation. From an energy-production point of view, it is desirable to have as much wind energy production as possible in order to save fuel consumption of the diesel engines and to reduce the level of pollution. From the customer point of view, it is desirable to have good power quality at the receiving end. The purpose of this paper is to show the impact of wind power plant in the entire system. Also, we discuss how the startup of the wind turbine and the transient condition during load changes affects the voltage and frequency in the system [C1859]

"A fact-finding survey on the heat generation from processing equipment at a semiconductor fab under operation"

The energy balance in vertical oxidation furnaces in a semiconductor fab under full scale operation was measured for the heat loads for cooling water, exhaust air and clean room air, which have not yet fully been reported. The results showed that the heat generated from the furnaces was removed with ratio of 64% by cooling water, 14% by exhausting air and 22% by clean room air, indicating very similar values measured in a laboratory scale operation reported by the authors at ISSM'99. Based on these results, the amount of energy saving was estimated by applying the energy saving methods proposed at ISSM'99. More than 35% of energy consumption can be reduced, which corresponds to more than 50% reduction of CO2release or 50% operation cost reduction compared to the current system [C1860]

"Cooperative modulation techniques for long haul relay in sensor networks"

Cooperative modulation techniques can reduce the energy requirements for the long haul transmission of data from localized sensor networks. This saving is vital in extending the battery life of power limited sensor nodes communicating over a time-limited channel. Several transmission methods, including a novel scheme that conveys information via node selection, are analyzed. The energy cost in local communications needed to support the cooperative long haul link is determined and used to make comparisons between the techniques [C1861]

"A middleware framework coordinating processor/power resource management for multimedia applications"

It is challenging to reduce the processor power consumption while meeting the processor resource requirement of distributed multimedia applications in portable computers. This paper presents a middleware framework coordinating the processor/power resource management (PPRM) in a mobile computing environment. Our framework has four major contributions: (1) providing a power-aware resource reservation mechanism, where admission control is based on the processor utilization and power availability; (2) adjusting the speed and corresponding power consumption of the processor depending upon events and triggered by the change of the system workload or power availability; (3) updating reservation contracts of multimedia applications to maintain their resource requirements while adjusting the processor speed; (4) notifying applications about the change of resource status to enable them to adapt their behavior and complete tasks before the power drains. Our experimental results show the effectiveness of the coordinating PPRM framework to save energy and maintain the resource requirements of multimedia applications [C1862]

"Implementation of bit-parallel lattice wave digital filters with increased maximal sample rate"

Arithmetic transformations for increased maximal sample rate of bit-parallel lattice wave digital filters implemented with carry-save arithmetic are proposed. The purpose is to increase the throughput in order to allow a reduction of the power consumption through supply voltage scaling. A lattice wave digital filter can be composed of first- and second-order allpass sections which are recursive structures. This sets a bound on the maximal sample rate. The proposed transformations reduce the latency of the critical loop by reordering of arithmetic operations. The resulting structure is numerically equivalent to the original structure. Hence, the

favourable properties of lattice wave digital filters, such as guaranteed stability, low coefficient sensitivity, and good dynamic range, are retained. An example of a filter implementation where the proposed transformations are applied is presented. The maximal sample rate for this example was improved by about 40% at the expense of a 10% increase of the area [C1863]

"Considering power variations of DVS processing elements for energy minimisation in distributed systems"

Dynamic voltage scaling (DVS) is a powerful technique to reduce power dissipation in embedded systems. In this paper we investigate the problem of considering DVS-processing element (DVS-PE) power variations dependent on the executed tasks, during the synthesis of distributed embedded systems, and its impact on the energy savings. Unlike previous approaches, which minimise the energy consumption by exploiting the available slack time without considering the PE power profiles, a new and fast heuristic for the voltage scaling problem is proposed, which improves the voltage selection for each task dependent on the individual power dissipation caused by that task. Experimental results show that energy reductions with up to 80.7% were achieved by integrating the proposed DVS algorithm, which considers the PE power profiles, into the co-synthesis of distributed systems. [C1864]

"Computer based photometric calculations provide savings for industrial lighting projects"

Third party lighting design programs offer many advantages to traditional calculations for fixture placement, foot-candle levels and spatial arrangement. The programs offer reduced design and estimating time, accurate foot-candle calculations, taking into consideration the contribution from adjacent lighting, and savings from reduced fixture requirements, fewer retrofits after start-up and energy savings by the client. The paper presents the basic design attributes of these programs and real world experience at the plant level [C1865]

"Energy efficient fixed-priority scheduling for real-time systems on variable voltage processors"

Energy consumption has become an increasingly important consideration in designing many real-time embedded systems. Variable voltage processors, if used properly, can dramatically reduce such system energy consumption. In this paper, we present a technique to determine voltage settings for a variable voltage processor that utilizes a fixed priority assignment to schedule jobs. Our approach also produces the minimum constant voltage needed to feasibly schedule the entire job set. Our algorithms lead to significant energy saving compared with previously presented approaches. [C1866]

"Power and energy reduction via pipeline balancing"

Minimizing power dissipation is an important design requirement for both portable and non-portable systems. In this work, we propose an architectural solution to the power problem that retains performance while reducing power. The technique, known as Pipeline Balancing (PLB), dynamically tunes the resources of a general purpose processor to the needs of the program by monitoring performance within each program. We analyze metrics for triggering PLB, and detail instruction queue design and energy savings based on an extension of the Alpha 21264 processor. Using a detailed simulator we present component and full chip power and energy savings for single and multi-threaded execution. Results show an issue queue and execution unit power reduction of up to 23% and 13%, respectively, with an average performance loss of 1% to 2% [C1867]

"Energy-effective issue logic"

The issue logic of a dynamically-scheduled superscalar processor is a complex mechanism devoted to start the execution of multiple instructions every cycle. Due to its complexity, it is responsible for a significant percentage of the energy consumed by a microprocessor. The energy consumption of the issue logic depends on several architectural parameters, the instruction issue queue size being one of the most important. In this paper we present a technique to reduce the energy consumption of the issue logic of a high-performance superscalar processor. The proposed technique is based on the observation that the conventional issue logic wastes a significant amount of energy for useless activity. In particular, the wake-up of empty entries and operands that are ready represents an important source of energy waste. Besides, we propose a mechanism to dynamically reduce the effective size of the instruction queue. We show that on average the effective instruction queue size can be reduced by a factor of 26% with minimal impact on performance. This reduction together with the energy saved for empty and ready entries result in about 90.7% reduction in the energy consumed by the wake-up logic, which represents 14.9% of the total energy of the assumed processor [C1868]

"Combining low-power scan testing and test data compression for system-on-a-chip"

We present a novel technique to reduce both test data volume and scan power dissipation using test data compression for system-on-a-chip testing. Power dissipation during test mode using ATPG-compacted test patterns is much higher than during functional mode. We show that Golomb coding of precomputed test sets leads to significant savings in peak and average power, without requiring either a slower scan clock or blocking logic in the scan cells. We also improve upon prior work on Golomb coding by showing that a separate cyclical scan register is not necessary for pattern decompression. Experimental results for the larger ISCAS 89 benchmarks show that reduced test data volume and low power scan testing can indeed be achieved in all cases. [C1869]

"Dynamic voltage scaling and power management for portable systems"

Portable systems require long battery lifetime while still delivering high performance. Dynamic voltage scaling (DVS) algorithms reduce energy consumption by changing processor speed and voltage at run time depending on the needs of the applications running. Dynamic power management (DPM) policies trade off the performance for the power consumption by selectively placing components into low-power states. In this work we extend the DPM model with a DVS algorithm, thus enabling larger power savings. We test our approach on MPEG video and MP3 audio algorithms running on the SmartBadge portable device. Our results show savings of a factor of three in energy consumption for combined DVS and DPM approaches. [C1870]

"Coupling-driven bus design for low-power application-specific systems"

In modern embedded systems including communication and multimedia applications, a large fraction of power is consumed during memory access and data transfer. Thus, buses should be designed and optimized to consume reasonable power while delivering sufficient performance. In this paper, we address a bus ordering problem for low-power application-specific systems. A heuristic algorithm is proposed to determine the order in a way that effective lateral component of capacitance is reduced, thereby reducing the power consumed by buses. Experimental results for various examples indicate that an average power saving from 30% to 46.7%, depending on capacitance components, can be obtained without any circuit overhead. [C1871]

"Analytical exploration of power efficient data-reuse transformations on multimedia applications"

Power savings that can be achieved by data-reuse decisions targeting at a custom memory hierarchy for multimedia applications executing on embedded cores are examined in this paper. Exploiting the temporal locality of memory accesses in data-intensive applications a set of data-reuse transformations on a typical motion estimation algorithm is determined. The aim is to reduce data related power consumption by moving background memory accesses to smaller foreground memories, which are less power costly. The impact of these transformations on power, performance and area is evaluated both for application specific circuits and general purpose processors. The number of data and instruction memory accesses is analytically calculated, enabling a fast exploration of the design space by varying algorithmic parameters [C1872]

"Micro-operation cache: a power aware frontend for variable instruction length ISA"

Introduces the micro-operation cache (Uop Cache-UC) designed to reduce the processor's frontend power and energy consumption without performance degradation. The UC caches basic blocks of instructions pre-decoded into micro-operations (uops). The UC fetches a single basic-block worth of uops per cycle. Fetching complete pre-decoded basic-blocks eliminates the need to repeatedly decode variable length instructions and simplifies the process of predicting, fetching, rotating and aligning fetched instructions. The UC design enables even a small structure to be quite effective. Results: a moderate-sized UC eliminates about 75% instruction decodes across a broad range of benchmarks and over 90% in multimedia applications and high-power tests. For existing Intel P6 family processors, the eliminated work may save about 10% of the full-chip power consumption with no performance degradation [C1873]

"Energy reduction in queues and stacks by adaptive bitwidth compression"

A new micro-architectural technique to reduce energy dissipated by queues and stacks is proposed. Similarly to related research which targets the transition activity in bit-lines, the technique is based on bitwidth compression. However unlike them, it utilizes the fixed accessing order embodied in queues and stacks to exploit input data correlation. The technique dynamically adjusts the required bitwidth to the number of bits which changed in comparison to the last access. It is neither restricted to specific bit-patterns such as zero-byte or precharging value and works efficiently on read and write without large area, timing or power overhead. Simulations show that using this technique, we can save the energy of instruction queue by up to 30% and the energy of video data queue by 20% [C1874]

"Novel recursive-DCT implementations: a comparative study"

Reports on a new recursive discrete cosine transform (DCT) architecture that is more efficient in terms of area and power in comparison with recently published recursive DCT architectures. Our approach employs A-, B- and C-type Goertzel filters. These three different realizations of Goertzel filters, together with a multiplier-less implementation of loop multiplications, are used so as to reduce the area, the multiplier delay and undesirable transitions, and hence the power consumption. The newly proposed DCT structure has been compared with conventional recursive implementations at different transform lengths, to observe that there are potential savings both in area and power [C1875]

"The scope for energy saving in the EU through the use of energy-efficient electricity distribution transformers"

The scope for saving energy in the EU through the use of energy-efficient distribution transformers, has been estimated at 22 TWh/year, worth 942 million Euros at 1999 prices. Despite the efficiency of individual units, up to 2% of total electricity generated is estimated to be lost in distribution transformers, nearly one-third of the overall losses from the transmission and distribution system. This is comparable in scope with the energy savings potential estimated for electric motors and classes of domestic appliances. It is equivalent to the annual energy consumption of 6 million homes, or the electricity produced by three nuclear power stations in Europe. Because of the long life span of distribution transformers, ultimate market penetration will only be achieved gradually. Despite this, the authors estimate that energy-efficient units could contribute 7 TWh of savings by 2010, representing 1% of the European commitment to reducing carbon emissions [C1876]

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