Reconfigurable Digital Receiver for Polarimetric Radar with Dual-Orthogonal Signals

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***Abstract*— This paper outlines the work on the design of a reconfigurable receiver for the PARSAX radar. The FPGA based digital receiver samples incoming signals at intermediate frequency (IF) and processes signals digitally instead of using more conventional analog approaches. In this way it offers more robust system stability and avoids unnecessary multi-channel calibrations of analog circuits. The processing algorithms implemented in the FPGA chips can be reconfigured adaptively regarding to different transmitted waveforms, and without changing of hardware. The successful development of reconfigurable receiver has been verified by experiment and yields maximum flexibility for the whole radar system.**

I. INTRODUCTION

Polarimetric radars transmit and receive both horizontal and vertical polarization signals. The full polarimetric nature of electromagnetic wave information can so be obtained by measuring the scattering matrix from a target. In most existing radars with polarimetric capabilities, pulse-to-pulse based switching of the transmitted and/or received polarization is used to decouple the elements of the scattering matrix. This introduces temporal, frequency and phase unambiguities in the polarimetric results [1 - 3].

The PARSAX (Polarimetric Agile Radar for S- and X-bands) radar, which implements the concept of dual-orthogonal sounding signals for simultaneous measurements of all elements of the polarization scattering matrix, is currently under development in IRCTR, TU Delft [1]. It simultaneously transmits and receives signals with dual-orthogonality both in polarimetric and in time–frequency spaces. Such type of sounding signals provide the unique possibility to split all elements of the scattering matrix and to measure all of them simultaneously during one pulse or single sweep time [4]. The four complex elements of the scattering matrix can be retrieved on reception by processing the received signals on each polarization channel with different reference signals. Many types of sophisticated signals taking the feature of orthogonality in time–frequency spaces have been investigated [4, 5].

When utilising dual-orthogonal signals in polarimetric radar for simultaneous scattering matrix measurements, the digital processor as part of the receiver must meet a series of requirements. Firstly, the processor should be capable of performing all required receiver functions such as filtering and pulse compression, regarding to different types of transmitted signals. Secondly, due to the volume of raw data produced by such radar can not be efficiently stored, real-time processing is a must and the processor should therefore possess high performance front-end signal processing capacity. In addition, since polarimetric radar with dual-orthogonal signals should have four processing channels at the receiver to extract all scattering matrix elements, this multi-channel feature requires that all receiver channels must be synchronised and have the same characteristics in amplitude and phase.

Current high-end field programmable gate array (FPGA) devices have been specifically designed to perform high speed digital signal processing [6, 7], and are thus ideally suited to be the processor of reconfigurable fully digital receiver for polarimetric radar. An FPGA based multi-channel reconfigurable digital receiver has been developed for the PARSAX radar. Taking advantages of state-of-art electronic techniques, the new receiver brings the analog-to-digital converter (ADC) closer to the radar antenna elements, samples incoming signals at intermediate frequency (IF) and processes signals digitally instead of using more conventional analog approaches; it takes the features of broadband coverage, multi-waveform adaptation and high performance real-time processing capacity. The processing algorithm and parameters can be reconfigured according to the user's requirement, which yields the maximum flexibility for the whole radar system.

The structure of the paper is the following. Section 2 gives an overview of the PARSAX radar and the hardware platform used for the reconfigurable digital receiver. Section 3 introduces two kinds of signals used in the current stage together with related processing algorithms. Section 4 shows the FPGA implementation with feasibility study results for different processing algorithms. Section 5 includes conclusions and future plans.

II. PARSAX RADAR AND RECONFIGURABLE PROCESSOR

A. PARSAX Radar Architecture

Fig. 1 depicts the simplified block diagram of the PARSAX radar. The system operates as follows. A pair of selected orthogonal signals $e_H(t)$, $e_V(t)$ are generated at IF from the Arbitrary Waveform Generator (AWG). These signals are calculated in advance and can be changed at software level. These two signals are instantaneously transmitted from two radio frequency (RF) channels with orthogonal polarization,