

# A Modular 24 GHz Radar Sensor for Digital Beamforming on Transmit and Receive

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**Abstract**—A compact modular 24 GHz imaging radar sensor for digital beamforming is presented. Besides digital beamforming on receive, the advantage of multiple switched transmitters is used for increasing the angular resolution, which requires less hardware effort. The presented FMCW radar sensor provides up to eight switchable transmitters and eight receiver channels for parallel receiving, allowing digital beamforming on transmit and receive. A new switching technique via switchable amplifiers is proposed. Within the scope of this paper an overview of the whole radar sensor's architecture, design and realization is given. The performance of the sensor is successfully demonstrated and evaluated by measurements.

## I. INTRODUCTION

Besides range and velocity, digital beamforming radars provide angular information of targets by exploiting multiple individually digitized channels. A good angular resolution with a large field of view are the main requirements for digital beamforming radars. The angular resolution is mainly dependent on the number of channels used. For radar systems with digital beamforming on receive-only, as presented in [1] [2], several coherent receiving paths are required. Increasing the number of receiver channels can be very unattractive in hardware costs and size. By using several distributed transmitters as shown in [3], digital beamforming on transmit can be performed by sequentially switching of transmitters. Whereas the performance of transmitter multiplexing is highly dependent on the scenario. Changes in the scenario during one transmit cycle can result into phase errors due to non coherent transmit signals.

For a better angular resolution several high resolution processing techniques as for example two-dimensional MUSIC [4] and Capon beamforming [5] can be applied, which have been investigated in other works, e.g. [1].

In this paper a 24 GHz frequency modulated continuous wave (FMCW) radar sensor, which uses a combination of eight transmitter and eight receiver channels is presented. This radar sensor allows digital beamforming on receive and transmit. A new switching technique via switchable amplifiers is proposed. The focus in this paper is set on the overall sensor system design including hardware and basic signal processing. In the

following section the components of the main system will be described. Basic signal processing issues are treated in section III and measurement results are presented in the final section.

## II. RADAR SENSOR ARCHITECTURE

In this section an overview is given on all functional blocks of the radar sensor. As shown in the block diagram in Fig. 1, the radar sensor consists of five modules realized each on a single printed circuit board (PCB) and stacked on each other:

- Frequency synthesizer module
- Transmitter module (Tx-module)
- Receiver module (Rx-module)
- Control and processing module with a field programmable gate array (FPGA)
- Antenna Array

This compact modular assembly allows a maximum flexibility and quick evaluation of different antenna types as well as different Tx and Rx modules.

### A. Frequency Synthesizer Module

The transmit signal as well as the local oscillator signals for the receivers are generated from the output signal of a voltage controlled oscillator (VCO). Thereby the VCO is controlled by a frequency synthesizer providing a FMCW signal with digitally programmable sweep frequencies and slopes. As shown in Fig. 2, the frequency synthesizer comprises a crystal oscillator (RCO), a direct digital synthesizer (DDS), a phase locked loop (PLL) including an internal frequency divider, a phase detector, a charge pump and an external loop filter. The DDS is clocked by a 200 MHz crystal oscillator ensuring high clock stability. By generating a signal at a low frequency, the DDS provides a reference frequency for the PLL. In order to control and stabilize the VCO's output frequency, the output frequency is fed back through a frequency divider to the input of the PLL, producing a closed loop configuration. This synthesizer architecture allows quick changes of the sweep parameters and provides linear and low phase noise signal generation. For the currently deployed frequency synthesizer